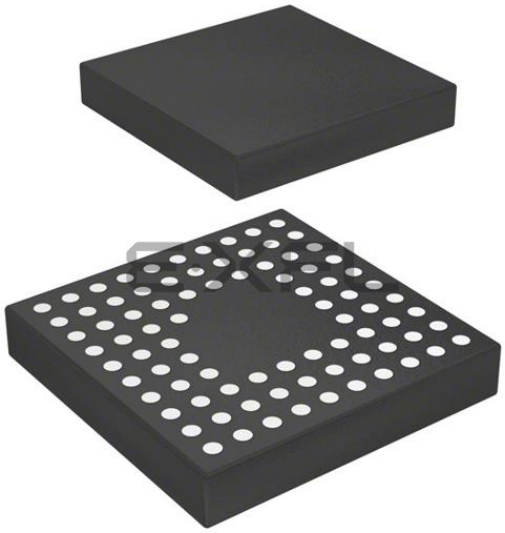
Renesas Electronics America Inc - M30280FAWG#U7B Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	M16C/60
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, IEBus, SIO, UART/USART
Peripherals	DMA, POR, PWM, Voltage Detect, WDT
Number of I/O	71
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	85-TFLGA
Supplier Device Package	85-TFLGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30280fawg-u7b

REJ03B0201-0050
Rev.0.50
2006.09.15

1. Overview

The M16C/28 Group (M16C/28 and M16C/28B) MCU are single-chip control MCU, fabricated using high-performance silicon gate CMOS technology with the M16C/60 series CPU core. The M16C/28 Group (M16C/28 and M16C/28B) are housed in 64-pin and 80-pin plastic molded LQFP packages and also in 85-pin plastic molded TFLGA (Thin Fine Pitch Land Grid Array) package. With a 1-Mbyte address space, this MCU combines advanced instruction manipulation capabilities to process complex instructions by less bytes and execute instructions at higher speed. It includes a multiplier and DMAC adequate for office automation, communication devices and other high-speed processing applications.

The M16C/28 has Normal-ver., T-ver., and V-ver.. The M16C/28B has Normal-ver. only.

This hardware manual describes the Normal-ver. only. Please contact Renesas Technology Corp. for T-ver./V-ver. information.

1.1 Applications

Audio, cameras, office equipment, communication equipment, portable equipment, home appliances (in-verter solution), motor control, industrial equipment, etc.

1.3 Block Diagram

Figure 1.1 is a block diagram of the M16C/28 Group (M16C/28, M16C/28B), 80-pin and 85-pin package.
Figure 1.2 is a block diagram of the M16C/28 Group (M16C/28, M16C/28B), 64-pin package.

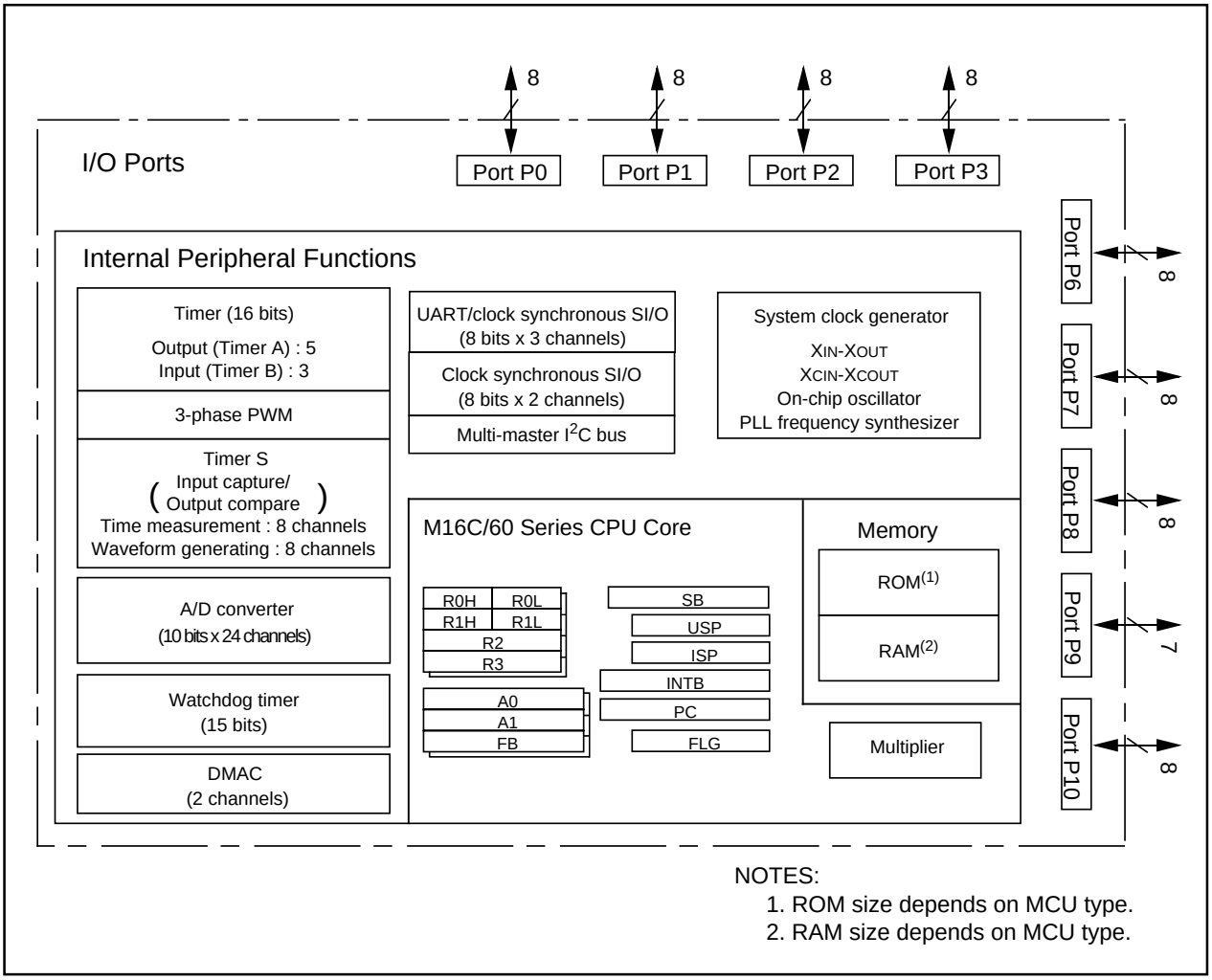


Figure 1.1 M16C/28 Group (M16C/28, M16C/28B), 80-Pin/85-Pin Block Diagram

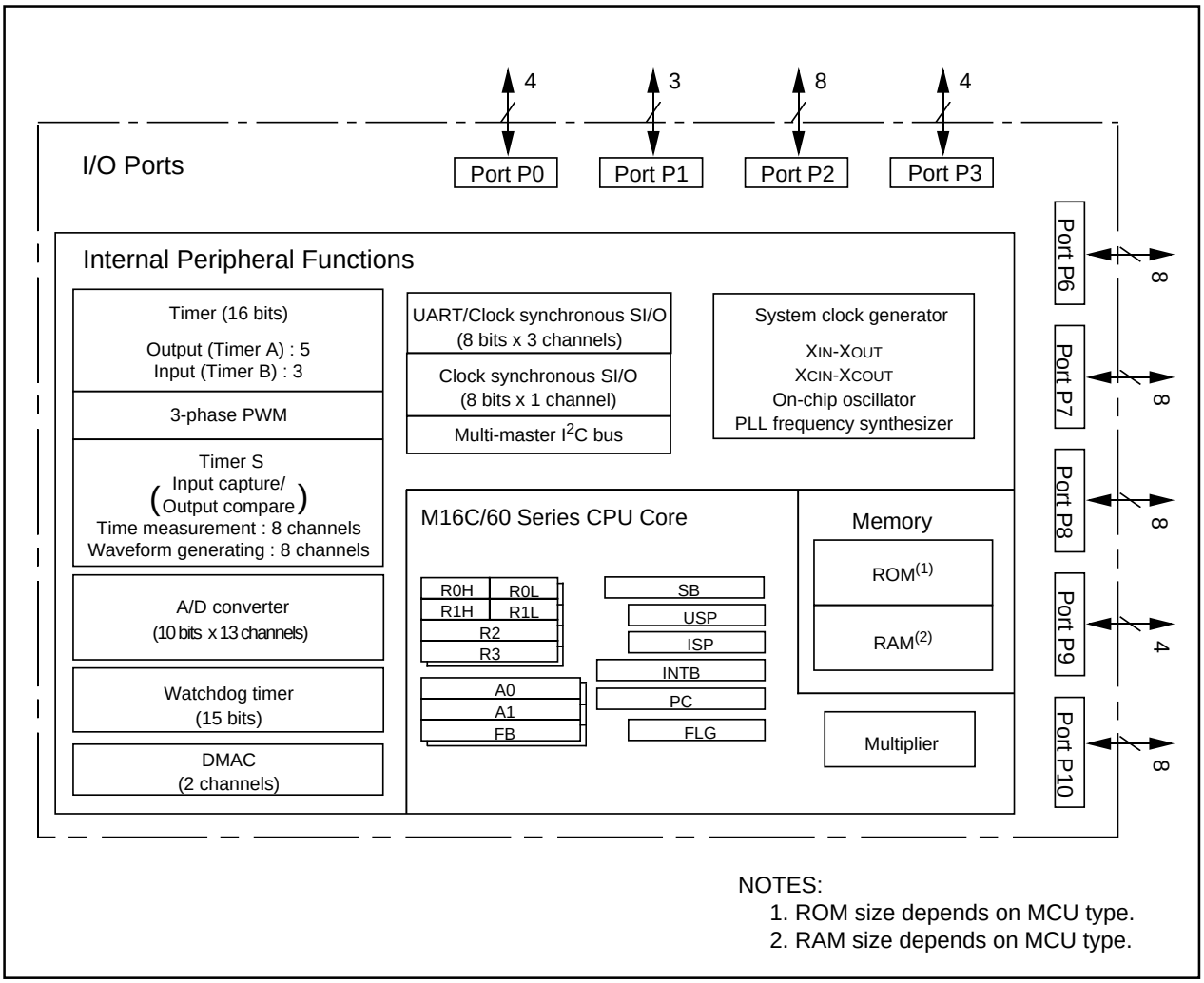


Figure 1.2 M16C/28 Group (M16C/28, M16C/28B), 64-Pin Block Diagram

1.4 Product Information

Tables 1.3 and **1.4** list the M16C/28 Group product information and **Figure 1.3** shows the product numbering system. The specifications are partially different between normal-ver.and T/ V-ver..

Table 1.3 M16C/28 Product List -Normal-ver. **As of September, 2006**

Type Number	ROM Capacity	RAM Capacity	Package Type	Remarks	Product Code
M30280F6WG (N)	48 K + 4 K	4 K	PTLG0085JB-A (85F0G)	Flash Memory	U3, U5, U7, U9
M30280F8WG (N)	64 K + 4 K	4 K			
M30280FAWG (N)	96 K + 4 K	8 K			
M30280F6HP (N)	48 K + 4 K	4 K	PLQP0080KB-A (80P6Q-A)		
M30280F8HP (N)	64 K + 4 K	4 K			
M30280FAHP (N)	96 K + 4 K	8 K			
M30280FCHP (N)	128 K + 4 K	12 K			
M30281F6HP (N)	48 K + 4 K	4 K	PLQP0064KB-A (64P6Q-A)		
M30281F8HP (N)	64 K + 4 K	4 K			
M30281FAHP (N)	96 K + 4 K	8 K			
M30281FCHP (N)	128 K + 4 K	12 K			
M30280M8-XXXHP (N)	64 K	4 K	PLQP0080KB-A (80P6Q-A)	Mask ROM	U3, U5
M30280MA-XXXHP (N)	96 K	8 K			
M30280MC-XXXHP (N)	128 K	12 K			
M30281M8-XXXHP (N)	64 K	4 K	PLQP0064KB-A (64P6Q-A)		
M30281MA-XXXHP (N)	96 K	8 K			
M30281MC-XXXHP (N)	128 K	12 K			

(N): New

Table 1.4 M16C/28B Product List -Normal-ver. **As of September, 2006**

Type Number	ROM Capacity	RAM Capacity	Package Type	Remarks	Product Code
M30280FCBHP (D)	128 K + 4 K	12 K	PLQP0080KB-A (80P6Q-A)	Flash memory	U7
M30281FCBHP (D)	128 K + 4 K	12 K	PLQP0064KB-A (64P6Q-A)		

(D): Under development

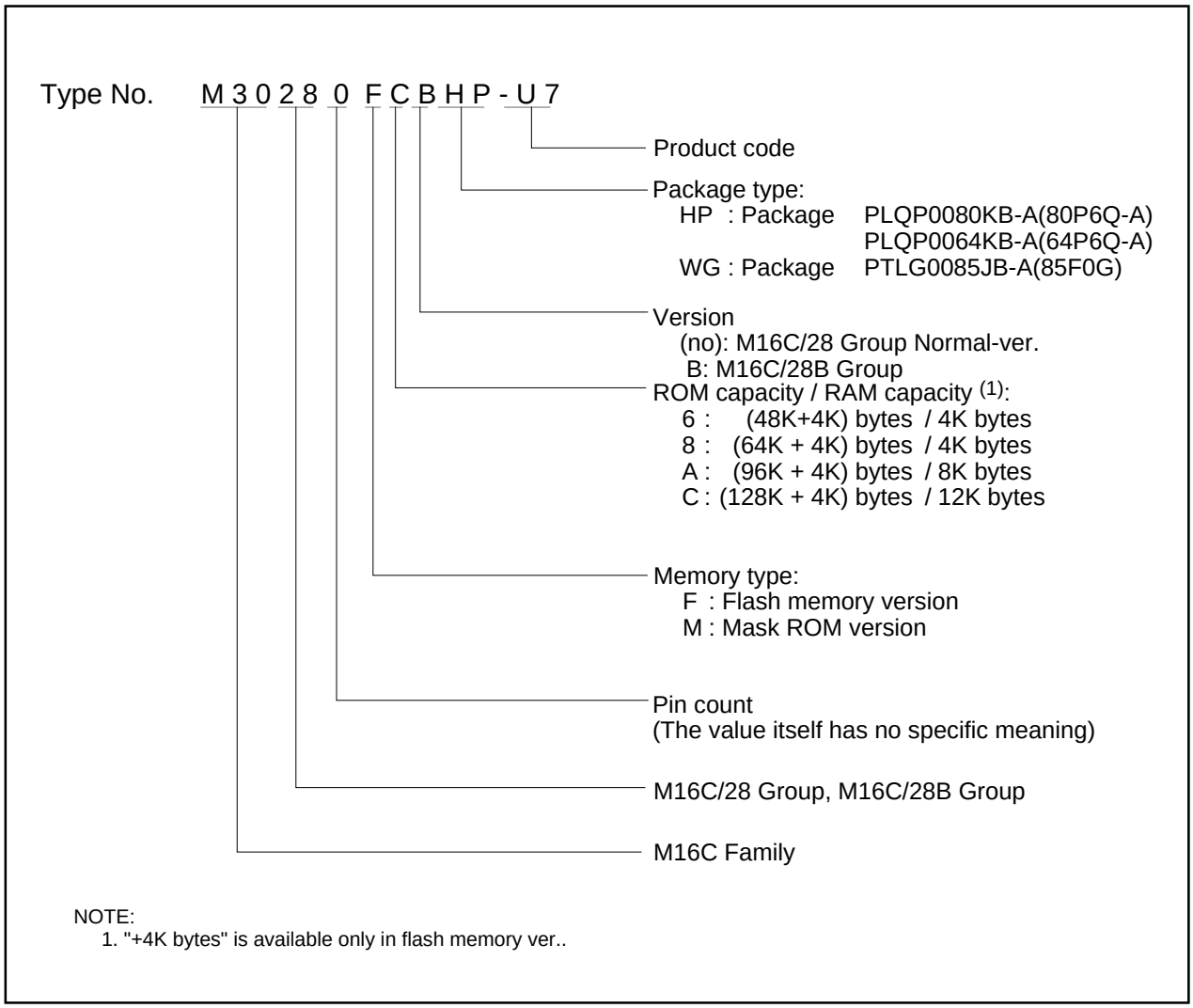
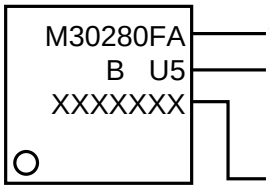


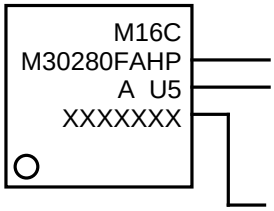
Figure 1.3 Product Numbering System

(1) Flash Memory Version, PTLG0085JB-A (85F0G), Normal-ver.



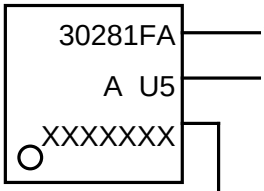
Type No. M30280FAWG
Chip version and product code
B : Chip version.
The first edition is shown to be blank and continues with A, B, and C.
U5 : Product code. (See **Table 1.5**)
Date code seven digits
Manufacturing management code

(2) Flash Memory Version, PLQP0080KB-A (80P6Q-A), Normal-ver.



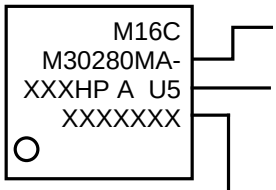
Type No. M30280FAHP
Chip version and product code
A : Chip version and product code(1)
The first edition is shown to be blank and continues with A, B and C.
U5 : Product code. (**Table 1.4**)
Date code seven digits
Manufacturing management code

(3) Flash Memory Version, PLQP0064KB-A (64P6Q-A), Normal-ver.



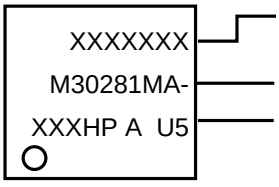
Type No. M30281FAHP
Chip version and product code
A : Chip version and product code(1)
The first edition is shown to be blank and continues with A, B and C.
U5 : Product code. (**Table 1.4**)
Date code seven digits
Manufacturing management code

(4) Mask ROM Version, PLQP0080KB-A (80P6Q-A), Normal-ver.



Type No. M30280MAHP
Chip version and product code
XXX : ROM No.
A : Chip version and product code(1)
The first edition is shown to be blank and continues with A, B and C.
U5 : Product code. (**Table 1.6**)
Date code seven digits
Manufacturing management code

(5) Mask ROM Version, PLQP0064-KB-A (64P6Q-A), Normal-ver.



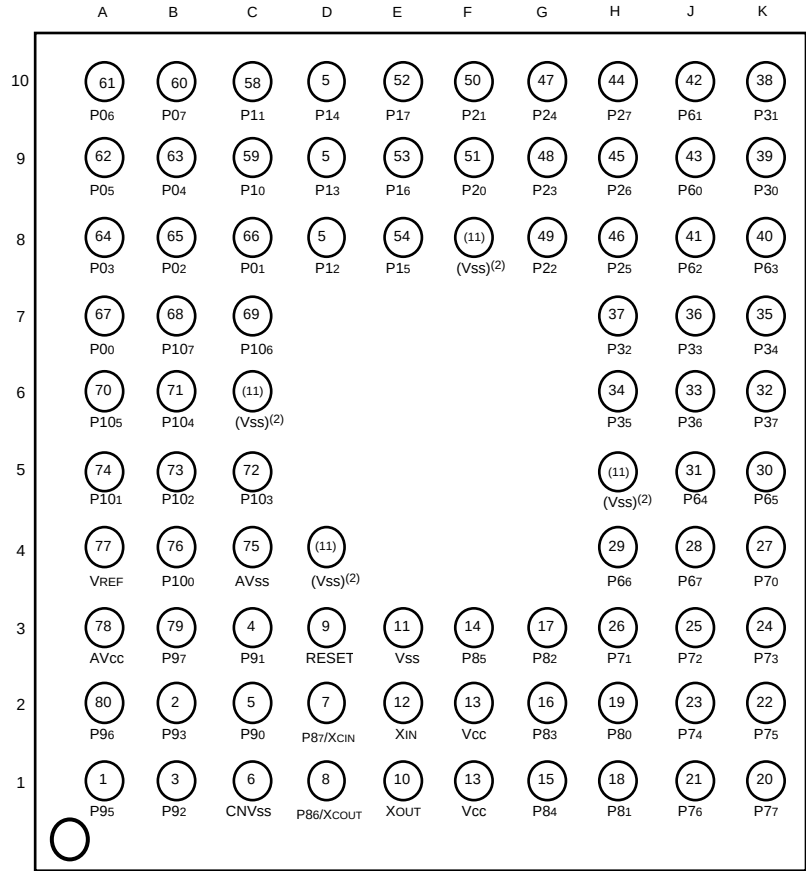
Date code seven digits
Manufacturing management code
Type No. M30281MAHP
Chip version and product code
XXX: ROM No.
A : Chip version and product code(1)
The first edition is shown to be blank and continues with A, B and C.
U5 : Product code. (**Table 1.6**)

NOTES:
1. The following functinos are not available in the first version and version A products.
-Delay trigger mode 0 of A/D conversion
-Delay trigger mode 1 of A/D conversion

Figure 1.4 Marking Diagram-M16C/28 Normal-ver.

1.5 Pin Assignment

Figures 1.5 to 1.7 show the pin Assignments (top view).



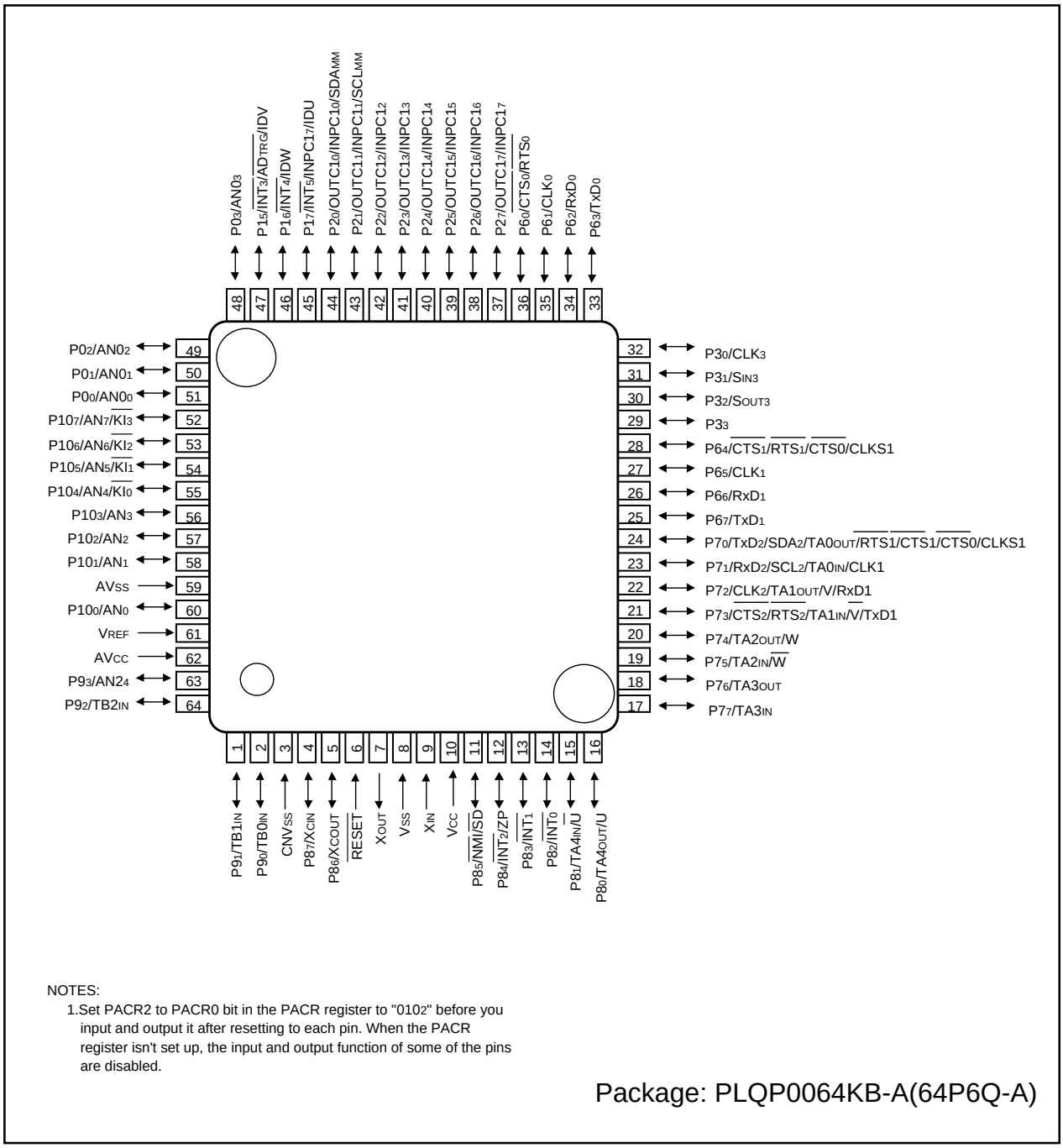
NOTES :
1. The numbers in each grid (circle) show the pin numbers of the M30280FAHP (80P6Q-A package)
2. Connect grids written as (Vss) to Vss(GND) or leave them open.
3. Set PACR2 to PACR0 bits in the PACR register to "0112" before you input and output it after resetting to each pin. When the PACR register is not set, the input and output function of some pins are disabled.

Package: PTLG0085JB-A(85F0G)

Figure 1.5 Pin Assignment (Top View) of 85-pin Package

Table 1.8 Pin Characteristics for 85-pin Package

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	Timer S Pin	UART Pin	Multi-master I^2C bus Pin	Analog Pin	PLQP0080KB-A Pin Number
A1		P9$_5$				CLK$_4$		AN2$_5$	1
A2		P9$_6$				SOUT$_4$		AN2$_6$	80
A3	AVcc								78
A4	VREF								77
A5		P10$_1$						AN$_1$	74
A6		P10$_5$	$\overline{KI}_1$					AN$_5$	70
A7		P0$_0$						AN0$_0$	67
A8		P0$_3$						AN0$_3$	64
A9		P0$_5$						AN0$_5$	62
A10		P0$_6$						AN0$_6$	61
B1		P9$_2$		TB2IN					3
B2		P9$_3$						AN2$_4$	2
B3		P9$_7$				SIN$_4$		AN2$_7$	79
B4		P10$_0$						AN$_0$	76
B5		P10$_2$						AN$_2$	73
B6		P10$_4$	$\overline{KI}_0$					AN$_4$	71
B7		P10$_7$	$\overline{KI}_3$					AN$_7$	68
B8		P0$_2$						AN0$_2$	65
B9		P0$_4$						AN0$_4$	63
B10		P0$_7$						AN0$_7$	60
C1	CNVss								6
C2		P9$_0$		TB0IN					5
C3		P9$_1$		TB1IN					4
C4	AVss								75
C5		P10$_3$						AN$_3$	72
C6	Vss(1)								(11)
C7		P10$_6$	$\overline{KI}_2$					AN$_6$	69
C8		P0$_1$						AN0$_1$	66
C9		P1$_0$						AN2$_0$	59
C10		P1$_1$						AN2$_1$	58
D1	XCOUT	P8$_6$							8
D2	XCIN	P8$_7$							7
D3	$\overline{RESET}$								9
D4	Vss(1)								(11)
D8		P1$_2$						AN2$_2$	57
D9		P1$_3$						AN2$_3$	56
D10		P1$_4$							55
E1	XOUT								10
E2	XIN								12
E3	Vss								11



NOTES:
1. Set PACR2 to PACR0 bit in the PACR register to "010₂" before you input and output it after resetting to each pin. When the PACR register isn't set up, the input and output function of some of the pins are disabled.

Package: PLQP0064KB-A(64P6Q-A)

Figure 1.6 Pin Assignment (Top View) of 64-Pin Package

Table 1.10 Pin Characteristics for 64-Pin Package

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	Timer S Pin	UART Pin	Mult-master I^2C bus Pin	Analog Pin
1		$P9_1$		TA_{1IN}				
2		$P9_0$		TB_{0IN}				
3	CNVss							
4	X_{CIN}	$P8_7$						
5	X_{COUT}	$P8_6$						
6	$\overline{RESET}$							
7	X_{OUT}							
8	Vss							
9	X_{IN}							
10	Vcc							
11		$P8_5$	$\overline{NMI}$	$\overline{SD}$				
12		$P8_4$	$\overline{INT_2}$	ZP				
13		$P8_3$	$\overline{INT_1}$					
14		$P8_2$	$\overline{INT_0}$					
15		$P8_1$		TA_{4IN} / $\overline{U}$				
16		$P8_0$		TA_{4OUT} / U				
17		$P7_7$		TA_{3IN}				
18		$P7_6$		TA_{3OUT}				
19		$P7_5$		TA_{2IN} / $\overline{W}$				
20		$P7_4$		TA_{2OUT} / W				
21		$P7_3$		TA_{1IN} / $\overline{V}$		$\overline{CTS_2}$ / $\overline{RTS_2}$ / TxD_1		
22		$P7_2$		TA_{1OUT} / V		CLK_2 / RxD_1		
23		$P7_1$		TA_{0IN}		RxD_2 / SCL_2 / CLK_1		
24		$P7_0$		TA_{0OUT}		TxD_2 / SDA_2 / $\overline{RTS_1}$ / $\overline{CTS_1}$ / $\overline{CTS_0}$ / $CLKS_1$		
25		$P6_7$				TxD_1		
26		$P6_6$				RxD_1		
27		$P6_5$				CLK_1		
28		$P6_4$				$\overline{RTS_1}$ / $\overline{CTS_1}$/ $\overline{CTS_0}$ / $CLKS_1$		
29		$P3_3$						
30		$P3_2$				$SOUT_3$		
31		$P3_1$				SIN_3		
32		$P3_0$				CLK_3		
33		$P6_3$				TxD_0		
34		$P6_2$				RxD_0		
35		$P6_1$				CLK_0		
36		$P6_0$				$\overline{RTS_0}$ / $\overline{CTS_0}$		
37		$P2_7$			$OUTC1_7$ / $INPC1_7$			
38		$P2_6$			$OUTC1_6$ / $INPC1_6$			
39		$P2_5$			$OUTC1_5$ / $INPC1_5$			
40		$P2_4$			$OUTC1_4$ / $INPC1_4$			

Table 10 Pin Characteristics for 64-Pin Package (Continued)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	Timer S Pin	UART Pin	Multi-master I^2C bus Pin	Analog Pin
41		$P2_3$			$OUTC1_3$ / $INPC1_3$			
42		$P2_2$			$OUTC1_2$ / $INPC1_2$			
43		$P2_1$			$OUTC1_1$ / $INPC1_1$		SCL_{MM}	
44		$P2_0$			$OUTC1_0$ / $INPC1_0$		SDA_{MM}	
45		$P1_7$	$\overline{INT}_5$	IDU	$INPC1_7$			
46		$P1_6$	$\overline{INT}_4$	IDW				
47		$P1_5$	$\overline{INT}_3$	IDV				$\overline{AD_{TRG}}$
48		$P0_3$						$AN0_3$
49		$P0_2$						$AN0_2$
50		$P0_1$						$AN0_1$
51		$P0_0$						$AN0_0$
52		$P10_7$	$\overline{KI}_3$					AN_7
53		$P10_6$	$\overline{KI}_2$					AN_6
54		$P10_5$	$\overline{KI}_1$					AN_5
55		$P10_4$	$\overline{KI}_0$					AN_4
56		$P10_3$						AN_3
57		$P10_2$						AN_2
58		$P10_1$						AN_1
59	AVss							
60		$P10_0$						AN_0
61	V_{REF}							
62	AVcc							
63		$P9_3$						$AN2_4$
64		$P9_2$		TB_{2IN}				

Table 1.10 Pin Description (64-Pin, 80-Pin and 85-Pin Packages) (Continued)

Classification	Symbol	I/O Type	Function
Timer S	$INPC1_0$ to $INPC1_7$	I	Input pins for the time measurement function
	$OUTC1_0$ to $OUTC1_7$	O	Output pins for the waveform generating function
I/O Ports	$P0_0$ to $P0_3$ $P1_5$ to $P1_7$ $P2_0$ to $P2_7$ $P3_0$ to $P3_3$ $P6_0$ to $P6_7$ $P7_0$ to $P7_7$ $P8_0$ to $P8_7$ $P10_0$ to $P10_7$	I/O	I/O ports for CMOS. Each port can be programmed for input or output under the control of the direction register. An input port can be set, by program, for a pull-up resistor available or for no pull-up resister available in 4-bit units
	$P9_0$ to $P9_3$	I/O	I/O ports having equivalent functions to P0

I : Input O : Output I/O : Input and output

Table 1.10 Pin Description (80-Pin and 85-Pin Packages only) (Continued)

Classification	Symbol	I/O Type	Function
Serial I/O	CLK4	I/O	Inputs and outputs the transfer clock
	SIN4	I	Inputs serial data
	SOUT4	O	Outputs serial data
A/D Converter	AN04 to AN07 AN20 to AN23 AN25 to AN27	I	Analog input pins for the A/D converter
I/O Ports	P04 to P07 P10 to P14 P34 to P37	I/O	I/O ports for CMOS. Each port can be programmed for input or output under the control of the direction register. An input port can be set, by program, for a pull-up resistor available or for no pull-up resister available in 4-bit units
	P95 to P97	I/O	I/O ports having equivalent functions to P0

I : Input O : Output I/O : Input and output

4. Special Function Register (SFR)

SFR (Special Function Register) is the control register of peripheral functions. **Tables 4.1** to **4.7** list the SFR information.

Table 4.1 SFR Information(1)[1]

Address	Register	Symbol	After Reset
0000₁₆			
0001₁₆			
0002₁₆			
0003₁₆			
0004₁₆	Processor mode register 0	PM0	00₁₆
0005₁₆	Processor mode register 1	PM1	00001000₂
0006₁₆	System clock control register 0	CM0	01001000₂
0007₁₆	System clock control register 1	CM1	00100000₂
0008₁₆			
0009₁₆	Address match interrupt enable register	AIER	XXXXXX00₂
000A₁₆	Protect register	PRCR	XX000000₂
000B₁₆			
000C₁₆	Oscillation stop detection register [2]	CM2	0X000010₂
000D₁₆			
000E₁₆	Watchdog timer start register	WDTS	XX₁₆
000F₁₆	Watchdog timer control register	WDC	00XXXXX₂
0010₁₆	Address match interrupt register 0	RMAD0	00₁₆
0011₁₆			00₁₆
0012₁₆			X0₁₆
0013₁₆			
0014₁₆	Address match interrupt register 1	RMAD1	00₁₆
0015₁₆			00₁₆
0016₁₆			X0₁₆
0017₁₆			
0018₁₆			
0019₁₆	Voltage detection register 1 [3]	VCR1	00001000₂
001A₁₆	Voltage detection register 2 [3]	VCR2	00₁₆
001B₁₆			
001C₁₆	PLL control register 0	PLC0	0001X010₂
001D₁₆			
001E₁₆	Processor mode register 2	PM2	XXX00000₂
001F₁₆	Low voltage detection interrupt register	D4INT	00₁₆
0020₁₆	DMA0 source pointer	SAR0	XX₁₆
0021₁₆			XX₁₆
0022₁₆			XX₁₆
0023₁₆			
0024₁₆	DMA0 destination pointer	DAR0	XX₁₆
0025₁₆			XX₁₆
0026₁₆			XX₁₆
0027₁₆			
0028₁₆	DMA0 transfer counter	TCR0	XX₁₆
0029₁₆			XX₁₆
002A₁₆			
002B₁₆			
002C₁₆	DMA0 control register	DM0CON	00000X00₂
002D₁₆			
002E₁₆			
002F₁₆			
0030₁₆	DMA1 source pointer	SAR1	XX₁₆
0031₁₆			XX₁₆
0032₁₆			XX₁₆
0033₁₆			
0034₁₆	DMA1 destination pointer	DAR1	XX₁₆
0035₁₆			XX₁₆
0036₁₆			XX₁₆
0037₁₆			
0038₁₆	DMA1 transfer counter	TCR1	XX₁₆
0039₁₆			XX₁₆
003A₁₆			
003B₁₆			
003C₁₆	DMA1 control register	DM1CON	00000X00₂
003D₁₆			
003E₁₆			
003F₁₆			

NOTES:
1. The blank spaces are reserved. No access is allowed.
2. The CM20, CM21, and CM27 bits do not change at oscillation stop detection reset.
3. This register does not change at software reset, watchdog timer reset and oscillation stop detection reset.

X : Undefined

Table 4.3 SFR Information(3)(1)

Address	Register	Symbol	After Reset
≈			≈
01B0₁₆			
01B1₁₆			
01B2₁₆			
01B3₁₆	Flash memory control register 4 (2)	FMR4	01000000₂
01B4₁₆			
01B5₁₆	Flash memory control register 1 (2)	FMR1	000XXX0X₂
01B6₁₆			
01B7₁₆	Flash memory control register 0 (2)	FMR0	00000001₂
01B8₁₆			
01B9₁₆			
≈			≈
0210₁₆	Low-power Consumption Control 0	LPCC0	X0000001₂
0211₁₆			
0212₁₆			
0213₁₆			
0214₁₆			
0215₁₆			
0216₁₆			
0217₁₆			
0218₁₆			
0219₁₆			
≈			≈
0250₁₆			
0251₁₆			
0252₁₆			
0253₁₆			
0254₁₆			
0255₁₆			
0256₁₆			
0257₁₆			
0258₁₆			
0259₁₆			
025A₁₆			
025B₁₆			
025C₁₆	On-chip oscillator control register	ROCR	X0000101₂
025D₁₆	Pin assignment control register	PACR	00₁₆
025E₁₆	Peripheral clock select register	PCLKR	00000011₂
025F₁₆	Low-power Consumption Control 1	LPCC1	00₁₆
≈			≈
02E0₁₆	I^2C0 data shift register	S00	XX₁₆
02E1₁₆			
02E2₁₆	I^2C0 address register	S0D0	00₁₆
02E3₁₆	I^2C0 control register 0	S1D0	00₁₆
02E4₁₆	I^2C0 clock control register	S20	00₁₆
02E5₁₆	I^2C0 start/stop condition control register	S2D0	00011010₂
02E6₁₆	I^2C0 control register 1	S3D0	00110000₂
02E7₁₆	I^2C0 control register 2	S4D0	00₁₆
02E8₁₆	I^2C0 status register	S10	0001000X₂
02E9₁₆			
02EA₁₆			
≈			≈
02FE₁₆			
02FF₁₆			

Note 1:The blank spaces are reserved. No access is allowed.
Note 2:This register is included in the flash memory version.

X : Undefined

Table 4.5 SFR Information(5)(1)

Address	Register	Symbol	After Reset
034016			
034116			
034216	Timer A1-1 register	TA11	XX16
034316			XX16
034416	Timer A2-1 register	TA21	XX16
034516			XX16
034616	Timer A4-1 register	TA41	XX16
034716			XX16
034816	Three-phase PWM control register 0	INVC0	0016
034916	Three-phase PWM control register 1	INVC1	0016
034A16	Three-phase output buffer register 0	IDB0	001111112
034B16	Three-phase output buffer register 1	IDB1	001111112
034C16	Dead time timer	DTT	XX16
034D16	Timer B2 interrupt occurrence frequency set counter	ICTB2	XX16
034E16	Position-data-retain function control register	PDRF	XXXX00002
034F16			
035016			
035116			
035216			
035316			
035416			
035516			
035616			
035716			
035816			
035916			
035A16			
035B16			
035C16			
035D16			
035E16	Interrupt request cause select register 2	IFSR2A	00XXXXX02(2)
035F16	Interrupt request cause select register	IFSR	0016
036016	SI/O3 transmit/receive register	S3TRR	XX16
036116			
036216	SI/O3 control register	S3C	010000002
036316	SI/O3 bit rate generator	S3BRG	XX16
036416	SI/O4 transmit/receive register	S4TRR	XX16
036516			
036616	SI/O4 control register	S4C	010000002
036716	SI/O4 bit rate generator	S4BRG	XX16
036816			
036916			
036A16			
036B16			
036C16			
036D16			
036E16			
036F16			
037016			
037116			
037216			
037316			
037416	UART2 special mode register 4	U2SMR4	0016
037516	UART2 special mode register 3	U2SMR3	000X0X0X2
037616	UART2 special mode register 2	U2SMR2	X0000000 2
037716	UART2 special mode register	U2SMR	X0000000 2
037816	UART2 transmit/receive mode register	U2MR	0016
037916	UART2 bit rate generator	U2BRG	XX16
037A16	UART2 transmit buffer register	U2TB	XX16
037B16			XX16
037C16	UART2 transmit/receive control register 0	U2C0	000010002
037D16	UART2 transmit/receive control register 1	U2C1	000000102
037E16	UART2 receive buffer register	U2RB	XX16
037F16			XX16

Note 1: The blank spaces are reserved. No access is allowed.
Note 2: Write 1 to bit 0 after reset.

X : Undefined

03C0$_{16}$
03C1$_{16}$
03C2$_{16}$
03C3$_{16}$
03C4$_{16}$
03C5$_{16}$
03C6$_{16}$
03C7$_{16}$
03C8$_{16}$
03C9$_{16}$
03CA$_{16}$
03CB$_{16}$
03CC$_{16}$
03CD$_{16}$