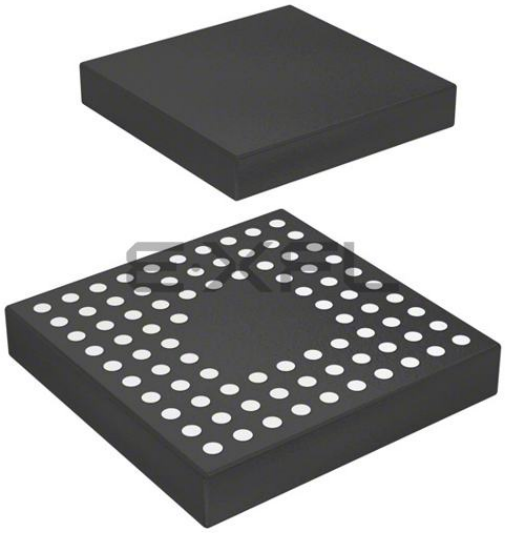
Renesas Electronics America Inc - M30280FAWG#U9B Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M16C/60
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, IEBus, SIO, UART/USART
Peripherals	DMA, POR, PWM, Voltage Detect, WDT
Number of I/O	71
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	85-TFLGA
Supplier Device Package	85-TFLGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30280fawg-u9b

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1.2 Performance Overview

Table 1.1 and **1.2** outline performance overview of the M16C/28 Group (M16C/28, M16C/28B).

Table 1.1 M16C/28 Group (M16C/28, M16C/28) Performance (80/85-Pin Package)

	Item	Performance
CPU	Number of basic instructions	91 instructions
	Minimum instruction excution time	41.7 ns (f(BCLK) = 24 MHz, Vcc = 4.2 V to 5.5 V) (M16C/28B) 50 ns (f(BCLK) = 20 MHz, Vcc = 3.0 V to 5.5 V) (M16C/28, M16C/28B) 100 ns (f(BCLK) = 10 MHz, Vcc= 2.7 V to 5.5 V) (M16C/28, M16C/28B)
	Operation mode	Single chip mode
	Address space	1M bytes
	Memory capacity	See **Table 1.3**
Peripheral Function	I/O port	Input/Output : 71 lines
	Multifunction timer	TimerA:16 bits x 5 channels, TimerB:16 bits x 3 channels Three-phase Motor Control Timer TimerS (Input Capture/Output Compare) : 16bit base timer x 1 channel (Input/Output x 8 channels)
	Serial I/O	2 channels (UART0, UART1) UART, clock synchronous 1 channel (UART2) UART, clock synchronous, I^2C bus(1), or IEbus(2) 2 channels (SI/O3, SI/O4) Clock synchronous 1 channel (Multi-Master I^2C bus(1))
	A/D converter	10 bits x 24 channels
	DMAC	2 channels
	Watchdog timer	15 bits x 1 (with prescaler)
	Interrupt	25 internal and 8 external sources, 4 software sources, 7 levels
	Clock generation circuit	4 circuits • Main clock (*) • Sub-clock (*) • On-chip oscillator • PLL frequency synthesizer (*) Equipped with a built-in feedback resistor
	Oscillation Stop Detect Function	Main clock oscillation stop, re-oscillation detect function
	Voltage detection circuit	Available
Electrical Characteristics	Power supply voltage	Vcc = 4.2 V to 5.5 V (f(BCLK) = 24 MHz) (M16C/28B) Vcc = 3.0 V to 5.5 V (f(BCLK) = 20 MHz) (M16C/28, M16C/28B) Vcc = 2.7 V to 5.5 V (f(BCLK) = 10 MHz) (M16C/28, M16C/28B)
	Power consumption	16 mA (Vcc = 5V, f(BCLK) = 20 MHz) 25 µA (f(XCIN) = 32 KHz on RAM) 3.0 µA (Vcc = 3V, f(XCIN) = 32 KHz, in wait mode) 0.7 µA (Vcc = 3V, in stop mode)
Flash Memory	Program/erase supply voltage	2.7 V to 5.5 V
	Program and erase endurance	100 times (all space) or 1,000 times (Blocks 0 to 5) /10,000 times (Block A, Block B(3))
Operating Ambient Temperature		-20 to 85°C/-40 to 85°C(3)
Package		80-pin plastic mold LQFP, 85-pin plastic mold TFLGA

NOTES:
1. I^2C bus is a trademark of Koninklijke Philips Electronics N. V.
2. IEBus is a trademark of NEC Electronics Corporation.
3. Refer to **Table 1.5** to **1.7** for number of program/erase.
4. Use PLL frequency synthesizer to use M16C/28B at f(BCLK) = 24 MHz.

1.3 Block Diagram

Figure 1.1 is a block diagram of the M16C/28 Group (M16C/28, M16C/28B), 80-pin and 85-pin package.
Figure 1.2 is a block diagram of the M16C/28 Group (M16C/28, M16C/28B), 64-pin package.

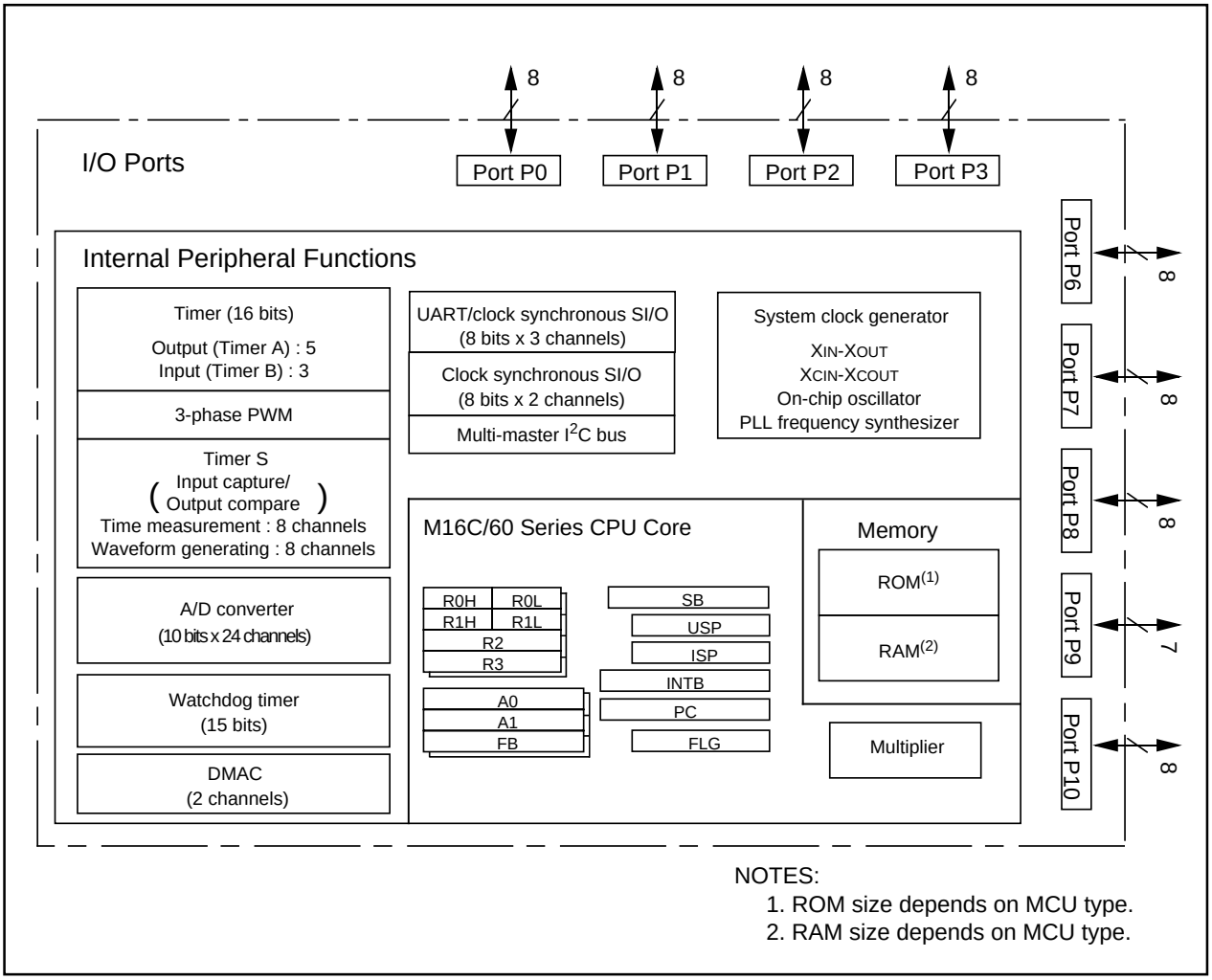


Figure 1.1 M16C/28 Group (M16C/28, M16C/28B), 80-Pin/85-Pin Block Diagram

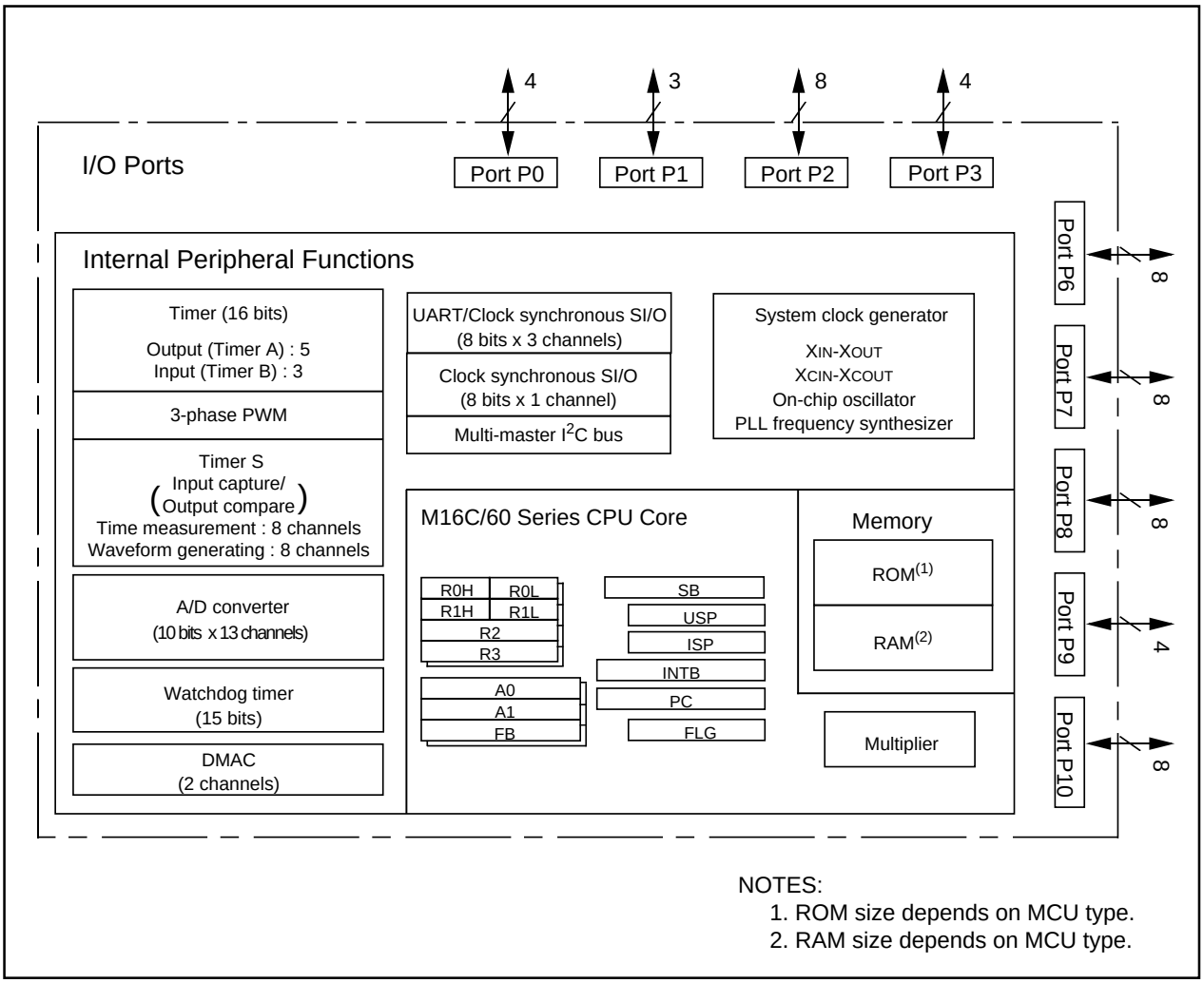


Figure 1.2 M16C/28 Group (M16C/28, M16C/28B), 64-Pin Block Diagram

1.4 Product Information

Tables 1.3 and **1.4** list the M16C/28 Group product information and **Figure 1.3** shows the product numbering system. The specifications are partially different between normal-ver.and T/ V-ver..

Table 1.3 M16C/28 Product List -Normal-ver. **As of September, 2006**

Type Number	ROM Capacity	RAM Capacity	Package Type	Remarks	Product Code
M30280F6WG (N)	48 K + 4 K	4 K	PTLG0085JB-A (85F0G)	Flash Memory	U3, U5, U7, U9
M30280F8WG (N)	64 K + 4 K	4 K			
M30280FAWG (N)	96 K + 4 K	8 K			
M30280F6HP (N)	48 K + 4 K	4 K	PLQP0080KB-A (80P6Q-A)		
M30280F8HP (N)	64 K + 4 K	4 K			
M30280FAHP (N)	96 K + 4 K	8 K			
M30280FCHP (N)	128 K + 4 K	12 K			
M30281F6HP (N)	48 K + 4 K	4 K	PLQP0064KB-A (64P6Q-A)		
M30281F8HP (N)	64 K + 4 K	4 K			
M30281FAHP (N)	96 K + 4 K	8 K			
M30281FCHP (N)	128 K + 4 K	12 K			
M30280M8-XXXHP (N)	64 K	4 K	PLQP0080KB-A (80P6Q-A)	Mask ROM	U3, U5
M30280MA-XXXHP (N)	96 K	8 K			
M30280MC-XXXHP (N)	128 K	12 K			
M30281M8-XXXHP (N)	64 K	4 K	PLQP0064KB-A (64P6Q-A)		
M30281MA-XXXHP (N)	96 K	8 K			
M30281MC-XXXHP (N)	128 K	12 K			

(N): New

Table 1.4 M16C/28B Product List -Normal-ver. **As of September, 2006**

Type Number	ROM Capacity	RAM Capacity	Package Type	Remarks	Product Code
M30280FCBHP (D)	128 K + 4 K	12 K	PLQP0080KB-A (80P6Q-A)	Flash memory	U7
M30281FCBHP (D)	128 K + 4 K	12 K	PLQP0064KB-A (64P6Q-A)		

(D): Under development

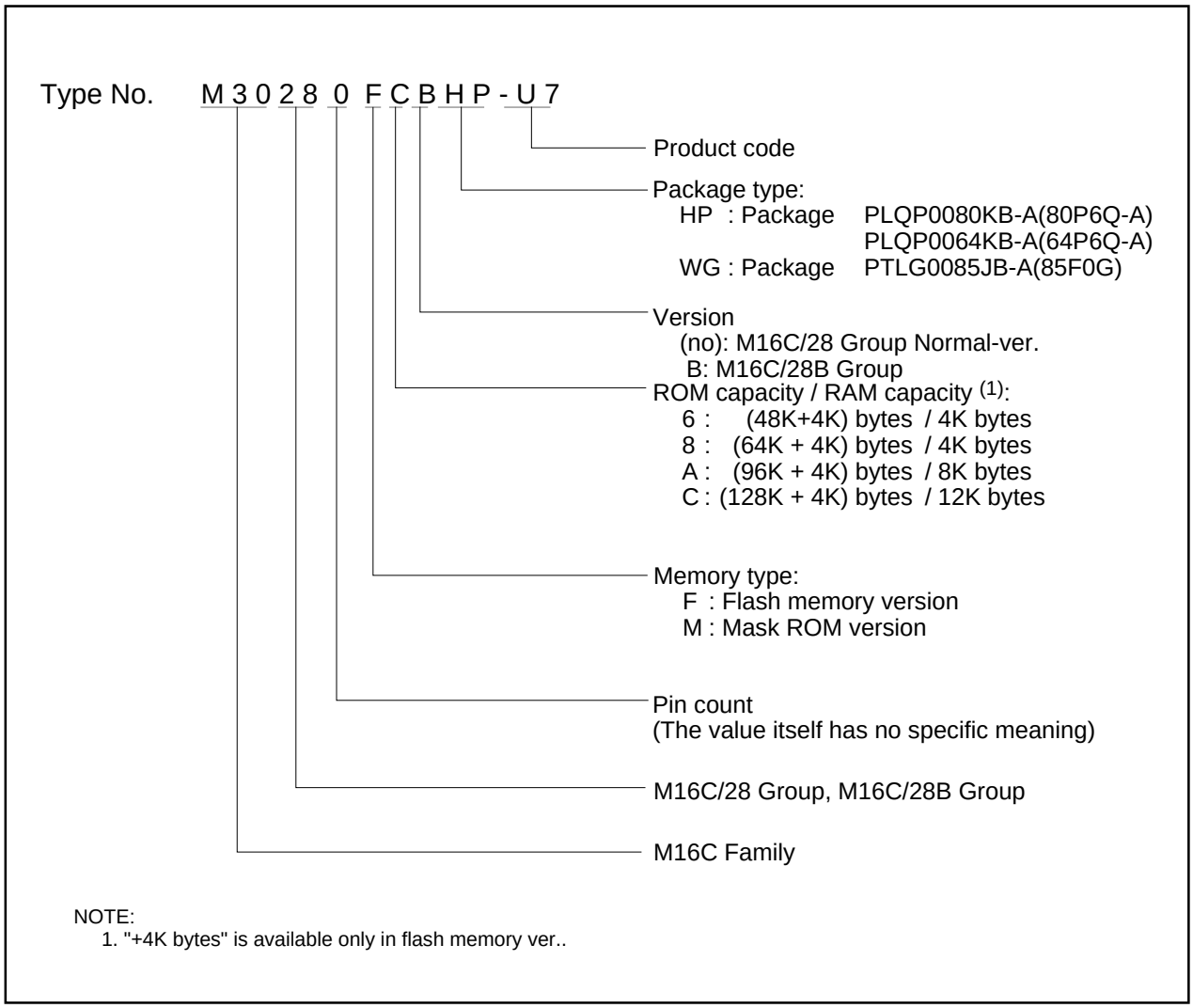
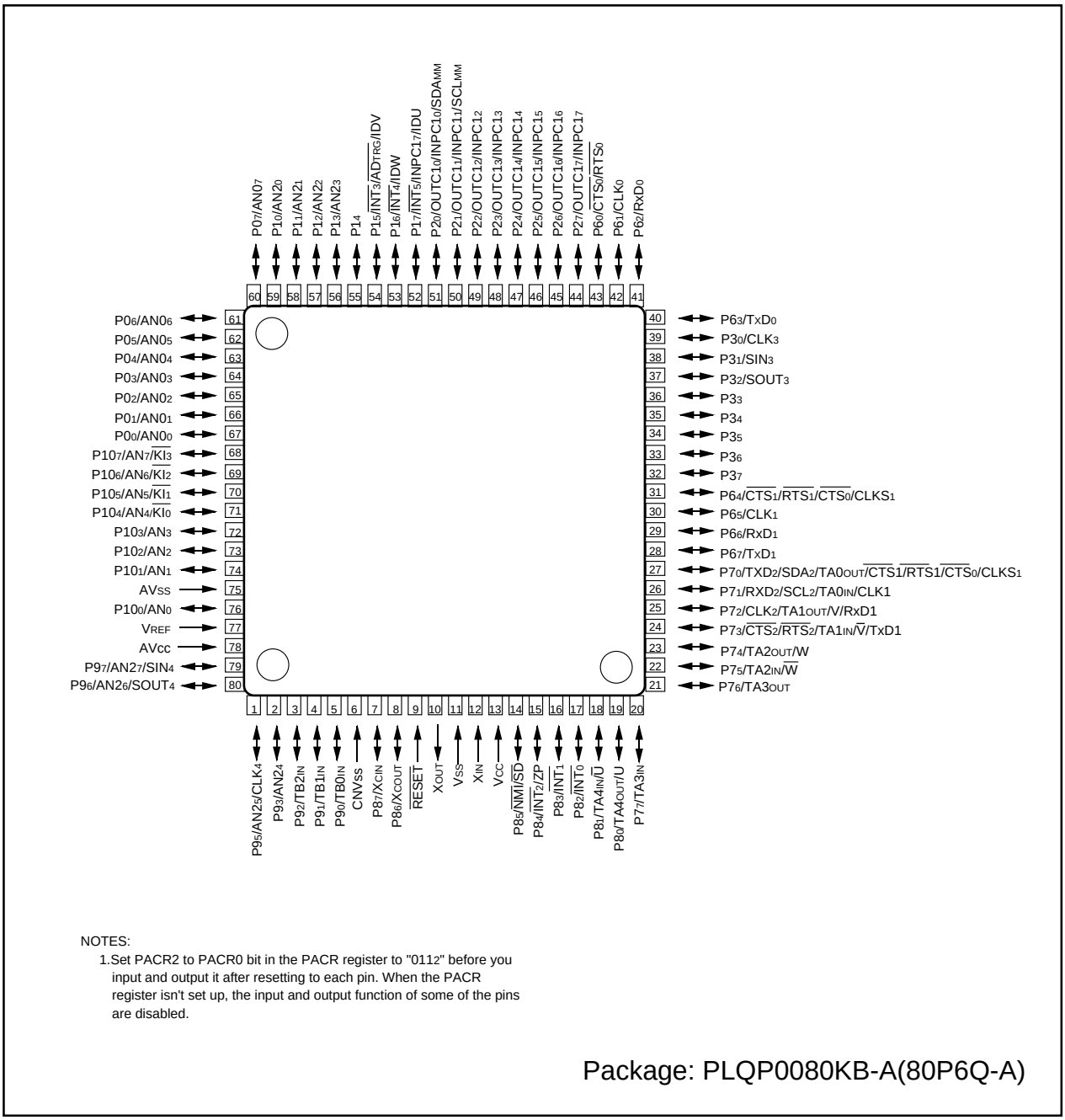


Figure 1.3 Product Numbering System

Table 1.8 Pin Characteristics for 85-pin Package (continued)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	Timer S Pin	UART Pin	Multi-master I²C bus Pin	Analog Pin	PLQP0080KB-A Pin Number
E8		P15	$\overline{INT_3}$	IDV				$\overline{ADTRG}$	54
E9		P16	$\overline{INT_4}$	IDW					53
E10		P17	$\overline{INT_5}$	IDU	INPC17				52
F1	Vcc								13
F2	Vcc								13
F3		P85	$\overline{NMI}$	$\overline{SD}$					14
F8	Vss(1)								(11)
F9		P20			OUTC10 / INPC10		SDAMM		51
F10		P21			OUTC11 / INPC11		SCLMM		50
G1		P84	$\overline{INT_2}$	ZP					15
G2		P83	$\overline{INT_1}$						16
G3		P82	$\overline{INT_0}$						17
G8		P22			OUTC12 / INPC12				49
G9		P23			OUTC13 / INPC13				48
G10		P24			OUTC14 / INPC14				47
H1		P81		TA4IN / $\overline{U}$					18
H2		P80		TA4OUT / U					19
H3		P71		TA0IN		RXD2 / SCL2 / CLK1			26
H4		P66				RXD1			29
H5	Vss(1)								(11)
H6		P35							34
H7		P32				SOUT3			37
H8		P25			OUTC15 / INPC15				46
H9		P26			OUTC16 / INPC16				45
H10		P27			OUTC17 / INPC17				44
J1		P76		TA3OUT					21
J2		P74		TA2OUT / W					23
J3		P72		TA1OUT / V		CLK2 / RXD1			25
J4		P67				TXD1			28
J5		P64				$\overline{RTS_1}$ / $\overline{CTS_1}$/ $\overline{CTS_0}$ / CLKS1			31
J6		P36							33
J7		P33							36
J8		P62				RXD0			41
J9		P60				$\overline{RTS_0}$ / $\overline{CTS_0}$			43
J10		P61				CLK0			42
K1		P77		TA3IN					20
K2		P75		TA2IN / $\overline{W}$					22
K3		P73		TA1IN / $\overline{V}$		$\overline{CTS_2}$ / $\overline{RTS_2}$ / $\overline{TXD_1}$			24
K4		P70		TA0OUT		TXD2 / SDA2 / $\overline{RTS_1}$ / $\overline{CTS_1}$ / $\overline{CTS_0}$ / $\overline{CLKS_1}$			27
K5		P65				CLK1			30
K6		P37							32
K7		P34							35
K8		P63				TXD0			40
K9		P30				CLK3			39
K10		P31				SIN3			38



NOTES:
1. Set PACR2 to PACR0 bit in the PACR register to "011₂" before you input and output it after resetting to each pin. When the PACR register isn't set up, the input and output function of some of the pins are disabled.

Package: PLQP0080KB-A(80P6Q-A)

Figure 1.5 Pin Assignment (Top View) of 80-Pin Package

Table 1.10 Pin Characteristics for 64-Pin Package

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	Timer S Pin	UART Pin	Mult-master I^2C bus Pin	Analog Pin
1		$P9_1$		TA_{1IN}				
2		$P9_0$		TB_{0IN}				
3	CNVss							
4	X_{CIN}	$P8_7$						
5	X_{COUT}	$P8_6$						
6	$\overline{RESET}$							
7	X_{OUT}							
8	Vss							
9	X_{IN}							
10	Vcc							
11		$P8_5$	$\overline{NMI}$	$\overline{SD}$				
12		$P8_4$	$\overline{INT_2}$	ZP				
13		$P8_3$	$\overline{INT_1}$					
14		$P8_2$	$\overline{INT_0}$					
15		$P8_1$		TA_{4IN} / $\overline{U}$				
16		$P8_0$		TA_{4OUT} / U				
17		$P7_7$		TA_{3IN}				
18		$P7_6$		TA_{3OUT}				
19		$P7_5$		TA_{2IN} / $\overline{W}$				
20		$P7_4$		TA_{2OUT} / W				
21		$P7_3$		TA_{1IN} / $\overline{V}$		$\overline{CTS_2}$ / $\overline{RTS_2}$ / TxD_1		
22		$P7_2$		TA_{1OUT} / V		CLK_2 / RxD_1		
23		$P7_1$		TA_{0IN}		RxD_2 / SCL_2 / CLK_1		
24		$P7_0$		TA_{0OUT}		TxD_2 / SDA_2 / $\overline{RTS_1}$ / $\overline{CTS_1}$ / $\overline{CTS_0}$ / $CLKS_1$		
25		$P6_7$				TxD_1		
26		$P6_6$				RxD_1		
27		$P6_5$				CLK_1		
28		$P6_4$				$\overline{RTS_1}$ / $\overline{CTS_1}$/ $\overline{CTS_0}$ / $CLKS_1$		
29		$P3_3$						
30		$P3_2$				$SOUT_3$		
31		$P3_1$				SIN_3		
32		$P3_0$				CLK_3		
33		$P6_3$				TxD_0		
34		$P6_2$				RxD_0		
35		$P6_1$				CLK_0		
36		$P6_0$				$\overline{RTS_0}$ / $\overline{CTS_0}$		
37		$P2_7$			$OUTC1_7$ / $INPC1_7$			
38		$P2_6$			$OUTC1_6$ / $INPC1_6$			
39		$P2_5$			$OUTC1_5$ / $INPC1_5$			
40		$P2_4$			$OUTC1_4$ / $INPC1_4$			

1.6 Pin Description

Table 1.10 Pin Description (64-Pin, 80-Pin and 85-Pin Packages)

Classification	Symbol	I/O Type	Function
Power Supply	VCC, VSS	I	Apply 2.7 to 5.5V to the Vcc pin. Apply 0V to the Vss pin.
Analog Power Supply	AVCC AVSS	I	Supplies power to the A/D converter. Connect the AVCC pin to VCC and the AVSS pin to VSS.
Reset Input	$\overline{\text{RESET}}$	I	The MCU is in a reset state when "L" is applied to the $\overline{\text{RESET}}$ pin
CNVSS	CNVSS	I	Connect the CNVSS pin to VSS.
Main Clock Input	XIN	I	I/O pins for the main clock oscillation circuit. Connect a ceramic resonator or crystal oscillator between XIN and XOUT. To apply external clock, apply it to XIN and leave XOUT open. If XIN is not used (for external oscillator or external clock) connect XIN pin to VCC and leave XOUT open.
Main Clock Output	XOUT	O	
Sub Clock Input	XCIN	I	I/O pins for the sub clock oscillation circuit. Connect a crystal oscillator between XCIN and XCOUT.
Sub Clock Output	XCOUT	O	
$\overline{\text{INT}}$ Interrupt Input	$\overline{\text{INT0}}$ to $\overline{\text{INT5}}$	I	Input pins for the $\overline{\text{INT}}$ interrupt. $\overline{\text{INT2}}$ can be used for Timer A Z-phase function.
$\overline{\text{NMI}}$ Interrupt Input	$\overline{\text{NMI}}$	I	Input pin for the $\overline{\text{NMI}}$ interrupt. $\overline{\text{NMI}}$ cannot be used as I/O port while the three-phase motor control is enabled. Apply a stable "H" to $\overline{\text{NMI}}$ after setting it's direction register to "0" when the three-phase motor control is enabled.
Key Input Interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	Input pins for the key input interrupt
Timer A	TA0OUT to TA4OUT	I/O	I/O pins for the timer A0 to A4
	TA0IN to TA4IN	I	Input pins for the timer A0 to A4
	ZP	I	Input pin for Z-phase
Timer B	TB0IN to TB2IN	I	Input pins for the timer B0 to B2
Three-phase Motor Control Timer Output	U, $\overline{\text{U}}$, V, $\overline{\text{V}}$, W, $\overline{\text{W}}$	O	Output pins for the three-phase motor control timer
	IDU, IDW, IDV, $\overline{\text{SD}}$	I/O	Input and output pins for the three-phase motor control timer
Serial I/O	$\overline{\text{CTS0}}$ to $\overline{\text{CTS2}}$	I	Input pins for data transmission control
	$\overline{\text{RTS0}}$ to $\overline{\text{RTS2}}$	O	Output pins for data reception control
	CLK0 to CLK3	I/O	Inputs and outputs the transfer clock
	RxD0 to RxD2	I	Inputs serial data
	TxD0 to TxD2	O	Outputs serial data
	CLKS1	O	Output pin for transfer clock
I^2C Mode	SDA2	I/O	Inputs and outputs serial data
	SCL2		Inputs and outputs the transfer clock
Multi-master I^2C bus	SDAMM	I/O	Inputs and outputs serial data
	SCLMM		Inputs and outputs the transfer clock
Reference Voltage Input	VREF	I	Applies reference voltage to the A/D converter
A/D Converter	AN0 to AN7 AN00 to AN03 AN24	I	Analog input pins for the A/D converter
	$\overline{\text{ADTRG}}$		Input pin for an external A/D trigger

I : Input O : Output I/O : Input and output

Table 1.10 Pin Description (64-Pin, 80-Pin and 85-Pin Packages) (Continued)

Classification	Symbol	I/O Type	Function
Timer S	INPC10 to INPC17	I	Input pins for the time measurement function
	OUTC10 to OUTC17	O	Output pins for the waveform generating function
I/O Ports	P00 to P03 P15 to P17 P20 to P27 P30 to P33 P60 to P67 P70 to P77 P80 to P87 P100 to P107	I/O	I/O ports for CMOS. Each port can be programmed for input or output under the control of the direction register. An input port can be set, by program, for a pull-up resistor available or for no pull-up resister available in 4-bit units
	P90 to P93	I/O	I/O ports having equivalent functions to P0

I : Input O : Output I/O : Input and output

Table 1.10 Pin Description (80-Pin and 85-Pin Packages only) (Continued)

Classification	Symbol	I/O Type	Function
Serial I/O	CLK4	I/O	Inputs and outputs the transfer clock
	SIN4	I	Inputs serial data
	SOUT4	O	Outputs serial data
A/D Converter	AN04 to AN07 AN20 to AN23 AN25 to AN27	I	Analog input pins for the A/D converter
I/O Ports	P04 to P07 P10 to P14 P34 to P37	I/O	I/O ports for CMOS. Each port can be programmed for input or output under the control of the direction register. An input port can be set, by program, for a pull-up resistor available or for no pull-up resister available in 4-bit units
	P95 to P97	I/O	I/O ports having equivalent functions to P0

I : Input O : Output I/O : Input and output

3. Memory

Figure 3.1 is a memory map of the M16C/28 Group (M16C/28, M16C/28B). M16C/28 Group provides 1-Mbyte address space from addresses 00000_{16} to $FFFFF_{16}$. The internal ROM is allocated lower addresses beginning with address $FFFFF_{16}$. For example, 64 Kbytes internal ROM is allocated addresses $F0000_{16}$ to $FFFFF_{16}$.

Two 2-Kbyte internal ROM areas, block A and block B, are available in the flash memory version. The blocks are allocated addresses $F000_{16}$ to $FFFF_{16}$.

The fixed interrupt vector tables are allocated addresses $FFFDC_{16}$ to $FFFFF_{16}$. It stores the starting address of each interrupt routine. See the section on interrupts for details.

The internal RAM is allocated higher addresses beginning with address 00400_{16}. For example, 4-Kbytes internal RAM is allocated addresses 00400_{16} to $013FF_{16}$. Besides storing data, it becomes stacks when the subroutine is called or an interrupt is acknowledged.

SFR, consisting of control registers for peripheral functions such as I/O port, A/D converter, serial I/O, timers is allocated addresses 00000_{16} to $003FF_{16}$. All blank spaces within SFR are reserved and cannot be accessed by users.

The special page vector table is allocated to the addresses $FFE00_{16}$ to $FFFDB_{16}$. This vector is used by the JMPS or JSRS instruction. For details, refer to the ***M16C/60 and M16C/20 Series Software Manual***.

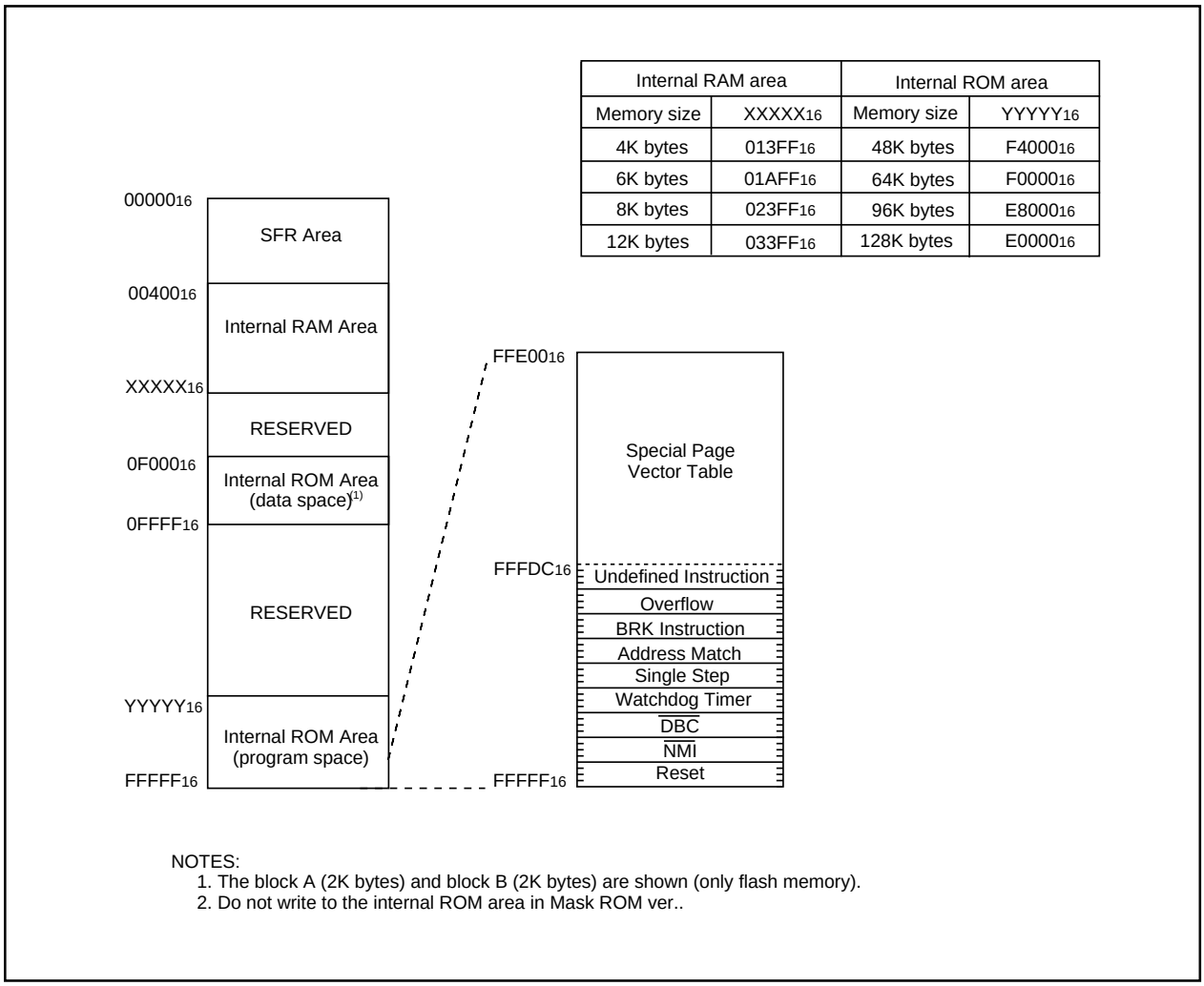


Figure 3.1 Memory Map

4. Special Function Register (SFR)

SFR (Special Function Register) is the control register of peripheral functions. **Tables 4.1** to **4.7** list the SFR information.

Table 4.1 SFR Information(1)[1]

Address	Register	Symbol	After Reset
0000₁₆			
0001₁₆			
0002₁₆			
0003₁₆			
0004₁₆	Processor mode register 0	PM0	00₁₆
0005₁₆	Processor mode register 1	PM1	00001000₂
0006₁₆	System clock control register 0	CM0	01001000₂
0007₁₆	System clock control register 1	CM1	00100000₂
0008₁₆			
0009₁₆	Address match interrupt enable register	AIER	XXXXXX00₂
000A₁₆	Protect register	PRCR	XX000000₂
000B₁₆			
000C₁₆	Oscillation stop detection register [2]	CM2	0X000010₂
000D₁₆			
000E₁₆	Watchdog timer start register	WDTS	XX₁₆
000F₁₆	Watchdog timer control register	WDC	00XXXXXX₂
0010₁₆	Address match interrupt register 0	RMAD0	00₁₆
0011₁₆			00₁₆
0012₁₆			X0₁₆
0013₁₆			
0014₁₆	Address match interrupt register 1	RMAD1	00₁₆
0015₁₆			00₁₆
0016₁₆			X0₁₆
0017₁₆			
0018₁₆			
0019₁₆	Voltage detection register 1 [3]	VCR1	00001000₂
001A₁₆	Voltage detection register 2 [3]	VCR2	00₁₆
001B₁₆			
001C₁₆	PLL control register 0	PLC0	0001X010₂
001D₁₆			
001E₁₆	Processor mode register 2	PM2	XXX00000₂
001F₁₆	Low voltage detection interrupt register	D4INT	00₁₆
0020₁₆	DMA0 source pointer	SAR0	XX₁₆
0021₁₆			XX₁₆
0022₁₆			XX₁₆
0023₁₆			
0024₁₆	DMA0 destination pointer	DAR0	XX₁₆
0025₁₆			XX₁₆
0026₁₆			XX₁₆
0027₁₆			
0028₁₆	DMA0 transfer counter	TCR0	XX₁₆
0029₁₆			XX₁₆
002A₁₆			
002B₁₆			
002C₁₆	DMA0 control register	DM0CON	00000X00₂
002D₁₆			
002E₁₆			
002F₁₆			
0030₁₆	DMA1 source pointer	SAR1	XX₁₆
0031₁₆			XX₁₆
0032₁₆			XX₁₆
0033₁₆			
0034₁₆	DMA1 destination pointer	DAR1	XX₁₆
0035₁₆			XX₁₆
0036₁₆			XX₁₆
0037₁₆			
0038₁₆	DMA1 transfer counter	TCR1	XX₁₆
0039₁₆			XX₁₆
003A₁₆			
003B₁₆			
003C₁₆	DMA1 control register	DM1CON	00000X00₂
003D₁₆			
003E₁₆			
003F₁₆			

NOTES:
1. The blank spaces are reserved. No access is allowed.
2. The CM20, CM21, and CM27 bits do not change at oscillation stop detection reset.
3. This register does not change at software reset, watchdog timer reset and oscillation stop detection reset.

X : Undefined

Table 4.3 SFR Information(3)(1)

Address	Register	Symbol	After Reset
≈			≈
01B016			
01B116			
01B216			
01B316	Flash memory control register 4 (2)	FMR4	010000002
01B416			
01B516	Flash memory control register 1 (2)	FMR1	000XXX0X2
01B616			
01B716	Flash memory control register 0 (2)	FMR0	000000012
01B816			
01B916			
≈			≈
021016	Low-power Consumption Control 0	LPCC0	X00000012
021116			
021216			
021316			
021416			
021516			
021616			
021716			
021816			
021916			
≈			≈
025016			
025116			
025216			
025316			
025416			
025516			
025616			
025716			
025816			
025916			
025A16			
025B16			
025C16	On-chip oscillator control register	ROCR	X00001012
025D16	Pin assignment control register	PACR	0016
025E16	Peripheral clock select register	PCLKR	000000112
025F16	Low-power Consumption Control 1	LPCC1	0016
≈			≈
02E016	I^2C0 data shift register	S00	XX16
02E116			
02E216	I^2C0 address register	S0D0	0016
02E316	I^2C0 control register 0	S1D0	0016
02E416	I^2C0 clock control register	S20	0016
02E516	I^2C0 start/stop condition control register	S2D0	000110102
02E616	I^2C0 control register 1	S3D0	001100002
02E716	I^2C0 control register 2	S4D0	0016
02E816	I^2C0 status register	S10	0001000X2
02E916			
02EA16			
≈			≈
02FE16			
02FF16			

Note 1:The blank spaces are reserved. No access is allowed.
Note 2:This register is included in the flash memory version.

X : Undefined

Table 4.4 SFR Information(4)(1)

Address	Register	Symbol	After Reset
0300₁₆ 0301₁₆	TM, WG register 0	G1TM0, G1PO0	XX16 XX16
0302₁₆ 0303₁₆	TM, WG register 1	G1TM1, G1PO1	XX16 XX16
0304₁₆ 0305₁₆	TM, WG register 2	G1TM2, G1PO2	XX16 XX16
0306₁₆ 0307₁₆	TM, WG register 3	G1TM3, G1PO3	XX16 XX16
0308₁₆ 0309₁₆	TM, WG register 4	G1TM4, G1PO4	XX16 XX16
030A₁₆ 030B₁₆	TM, WG register 5	G1TM5, G1PO5	XX16 XX16
030C₁₆ 030D₁₆	TM, WG register 6	G1TM6, G1PO6	XX16 XX16
030E₁₆ 030F₁₆	TM, WG register 7	G1TM7, G1PO7	XX16 XX16
0310₁₆	WG control register 0	G1POCR0	0X00XX002
0311₁₆	WG control register 1	G1POCR1	0X00XX002
0312₁₆	WG control register 2	G1POCR2	0X00XX002
0313₁₆	WG control register 3	G1POCR3	0X00XX002
0314₁₆	WG control register 4	G1POCR4	0X00XX002
0315₁₆	WG control register 5	G1POCR5	0X00XX002
0316₁₆	WG control register 6	G1POCR6	0X00XX002
0317₁₆	WG control register 7	G1POCR7	0X00XX002
0318₁₆	TM control register 0	G1TMCR0	0016
0319₁₆	TM control register 1	G1TMCR1	0016
031A₁₆	TM control register 2	G1TMCR2	0016
031B₁₆	TM control register 3	G1TMCR3	0016
031C₁₆	TM control register 4	G1TMCR4	0016
031D₁₆	TM control register 5	G1TMCR5	0016
031E₁₆	TM control register 6	G1TMCR6	0016
031F₁₆	TM control register 7	G1TMCR7	0016
0320₁₆ 0321₁₆	Base timer register	G1BT	XX16 XX16
0322₁₆	Base timer control register 0	G1BCR0	0016
0323₁₆	Base timer control register 1	G1BCR1	0016
0324₁₆	TM prescale register 6	G1TPR6	0016
0325₁₆	TM prescale register 7	G1TPR7	0016
0326₁₆	Function enable register	G1FE	0016
0327₁₆	Function select register	G1FS	0016
0328₁₆ 0329₁₆	Base timer reset register	G1BTRR	XX16 XX16
032A₁₆	Divider register	G1DV	0016
032B₁₆			
032C₁₆			
032D₁₆			
032E₁₆			
032F₁₆			
0330₁₆	Interrupt request register	G1IR	XX16
0331₁₆	Interrupt enable register 0	G1IE0	0016
0332₁₆	Interrupt enable register 1	G1IE1	0016
0333₁₆			
0334₁₆			
0335₁₆			
0336₁₆			
0337₁₆			
0338₁₆			
0339₁₆			
033A₁₆			
033B₁₆			
033C₁₆			
033D₁₆			
033E₁₆	NMI digital debounce register	NDDR	FF16
033F₁₆	P17 digital debounce register	P17DDR	FF16

Note 1:The blank spaces are reserved. No access is allowed.

X : Undefined

Table 4.6 SFR Information(6)(1)

Address	Register	Symbol	After Reset
038016	Count start flag	TABSR	0016
038116	Clock prescaler reset flag	CPSRF	0XXXXXXX2
038216	One-shot start flag	ONSF	0016
038316	Trigger select register	TRGSR	0016
038416	Up-down flag	UDF	0016
038516			
038616	Timer A0 register	TA0	XX16
038716			XX16
038816	Timer A1 register	TA1	XX16
038916			XX16
038A16	Timer A2 register	TA2	XX16
038B16			XX16
038C16	Timer A3 register	TA3	XX16
038D16			XX16
038E16	Timer A4 register	TA4	XX16
038F16			XX16
039016	Timer B0 register	TB0	XX16
039116			XX16
039216	Timer B1 register	TB1	XX16
039316			XX16
039416	Timer B2 register	TB2	XX16
039516			XX16
039616	Timer A0 mode register	TA0MR	0016
039716	Timer A1 mode register	TA1MR	0016
039816	Timer A2 mode register	TA2MR	0016
039916	Timer A3 mode register	TA3MR	0016
039A16	Timer A4 mode register	TA4MR	0016
039B16	Timer B0 mode register	TB0MR	00XX00002
039C16	Timer B1 mode register	TB1MR	00XX00002
039D16	Timer B2 mode register	TB2MR	00XX00002
039E16	Timer B2 special mode register	TB2SC	X00000002
039F16			
03A016	UART0 transmit/receive mode register	U0MR	0016
03A116	UART0 bit rate generator	U0BRG	XX16
03A216	UART0 transmit buffer register	U0TB	XX16
03A316			XX16
03A416	UART0 transmit/receive control register 0	U0C0	000010002
03A516	UART0 transmit/receive control register 1	U0C1	000000102
03A616	UART0 receive buffer register	U0RB	XX16
03A716			XX16
03A816	UART1 transmit/receive mode register	U1MR	0016
03A916	UART1 bit rate generator	U1BRG	XX16
03AA16	UART1 transmit buffer register	U1TB	XX16
03AB16			XX16
03AC16	UART1 transmit/receive control register 0	U1C0	000010002
03AD16	UART1 transmit/receive control register 1	U1C1	000000102
03AE16	UART1 receive buffer register	U1RB	XX16
03AF16			XX16
03B016	UART transmit/receive control register 2	UCON	X00000002
03B116			
03B216			
03B316			
03B416			
03B516			
03B616			
03B716			
03B816	DMA0 request cause select register	DM0SL	0016
03B916			
03BA16	DMA1 request cause select register	DM1SL	0016
03BB16			
03BC16			
03BD16			
03BE16			
03BF16			

Note 1:The blank spaces are reserved. No access is allowed.

X : Undefined

Table 4.7 SFR Information(7)(1)

Address	Register	Symbol	After Reset
03C0₁₆	A/D register 0	AD0	XX₁₆
03C1₁₆			XX₁₆
03C2₁₆	A/D register 1	AD1	XX₁₆
03C3₁₆			XX₁₆
03C4₁₆	A/D register 2	AD2	XX₁₆
03C5₁₆			XX₁₆
03C6₁₆	A/D register 3	AD3	XX₁₆
03C7₁₆			XX₁₆
03C8₁₆	A/D register 4	AD4	XX₁₆
03C9₁₆			XX₁₆
03CA₁₆	A/D register 5	AD5	XX₁₆
03CB₁₆			XX₁₆
03CC₁₆	A/D register 6	AD6	XX₁₆
03CD₁₆			XX₁₆
03CE₁₆	A/D register 7	AD7	XX₁₆
03CF₁₆			XX₁₆
03D0₁₆			
03D1₁₆			
03D2₁₆	A/D trigger control register	ADTRGCON	00₁₆
03D3₁₆	A/D convert status register 0	ADSTAT0	00000X00₂
03D4₁₆	A/D control register 2	ADCON2	00₁₆
03D5₁₆			
03D6₁₆	A/D control register 0	ADCON0	00000XXX₂
03D7₁₆	A/D control register 1	ADCON1	00₁₆
03D8₁₆			
03D9₁₆			
03DA₁₆			
03DB₁₆			
03DC₁₆			
03DD₁₆			
03DE₁₆			
03DF₁₆			
03E0₁₆	Port P0 register	P0	XX₁₆
03E1₁₆	Port P1 register	P1	XX₁₆
03E2₁₆	Port P0 direction register	PD0	00₁₆
03E3₁₆	Port P1 direction register	PD1	00₁₆
03E4₁₆	Port P2 register	P2	XX₁₆
03E5₁₆	Port P3 register	P3	XX₁₆
03E6₁₆	Port P2 direction register	PD2	00₁₆
03E7₁₆	Port P3 direction register	PD3	00₁₆
03E8₁₆			
03E9₁₆			
03EA₁₆			
03EB₁₆			
03EC₁₆	Port P6 register	P6	XX₁₆
03ED₁₆	Port P7 register	P7	XX₁₆
03EE₁₆	Port P6 direction register	PD6	00₁₆
03EF₁₆	Port P7 direction register	PD7	00₁₆
03F0₁₆	Port P8 register	P8	XX₁₆
03F1₁₆	Port P9 register	P9	XX₁₆
03F2₁₆	Port P8 direction register	PD8	00₁₆
03F3₁₆	Port P9 direction register	PD9	000X0000₂
03F4₁₆	Port P10 register	P10	XX₁₆
03F5₁₆			
03F6₁₆	Port P10 direction register	PD10	00₁₆
03F7₁₆			
03F8₁₆			
03F9₁₆			
03FA₁₆			
03FB₁₆			
03FC₁₆	Pull-up control register 0	PUR0	00₁₆
03FD₁₆	Pull-up control register 1	PUR1	00₁₆
03FE₁₆	Pull-up control register 2	PUR2	00₁₆
03FF₁₆	Port control register	PCR	00₁₆

Note 1:The blank spaces are reserved. No access is allowed.

X : Undefined

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