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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	M16C/60
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, IEBus, SIO, UART/USART
Peripherals	DMA, POR, PWM, Voltage Detect, WDT
Number of I/O	71
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30280fchp-u3b

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1. Overview

The M16C/28 Group (M16C/28 and M16C/28B) MCU are single-chip control MCU, fabricated using high-performance silicon gate CMOS technology with the M16C/60 series CPU core. The M16C/28 Group (M16C/28 and M16C/28B) are housed in 64-pin and 80-pin plastic molded LQFP packages and also in 85-pin plastic molded TFLGA (Thin Fine Pitch Land Grid Array) package. With a 1-Mbyte address space, this MCU combines advanced instruction manipulation capabilities to process complex instructions by less bytes and execute instructions at higher speed. It includes a multiplier and DMAC adequate for office automation, communication devices and other high-speed processing applications.

The M16C/28 has Normal-ver., T-ver., and V-ver.. The M16C/28B has Normal-ver. only.

This hardware manual describes the Normal-ver. only. Please contact Renesas Technology Corp. for T-ver./V-ver. information.

1.1 Applications

Audio, cameras, office equipment, communication equipment, portable equipment, home appliances (inverter solution), motor control, industrial equipment, etc.

1.2 Performance Overview

Table 1.1 and **1.2** outline performance overview of the M16C/28 Group (M16C/28, M16C/28B).

Table 1.1 M16C/28 Group (M16C/28, M16C/28) Performance (80/85-Pin Package)

	Item	Performance
CPU	Number of basic instructions	91 instructions
	Minimum instruction excution time	41.7 ns (f(BCLK) = 24 MHz, Vcc = 4.2 V to 5.5 V) (M16C/28B) 50 ns (f(BCLK) = 20 MHz, Vcc = 3.0 V to 5.5 V) (M16C/28, M16C/28B) 100 ns (f(BCLK) = 10 MHz, Vcc= 2.7 V to 5.5 V) (M16C/28, M16C/28B)
	Operation mode	Single chip mode
	Address space	1M bytes
	Memory capacity	See **Table 1.3**
Peripheral Function	I/O port	Input/Output : 71 lines
	Multifunction timer	TimerA:16 bits x 5 channels, TimerB:16 bits x 3 channels Three-phase Motor Control Timer TimerS (Input Capture/Output Compare) : 16bit base timer x 1 channel (Input/Output x 8 channels)
	Serial I/O	2 channels (UART0, UART1) UART, clock synchronous 1 channel (UART2) UART, clock synchronous, I^2C bus(1), or IEbus(2) 2 channels (SI/O3, SI/O4) Clock synchronous 1 channel (Multi-Master I^2C bus(1))
	A/D converter	10 bits x 24 channels
	DMAC	2 channels
	Watchdog timer	15 bits x 1 (with prescaler)
	Interrupt	25 internal and 8 external sources, 4 software sources, 7 levels
	Clock generation circuit	4 circuits • Main clock (*) • Sub-clock (*) • On-chip oscillator • PLL frequency synthesizer (*) Equipped with a built-in feedback resistor
	Oscillation Stop Detect Function	Main clock oscillation stop, re-oscillation detect function
	Voltage detection circuit	Available
Electrical Characteristics	Power supply voltage	Vcc = 4.2 V to 5.5 V (f(BCLK) = 24 MHz) (M16C/28B) Vcc = 3.0 V to 5.5 V (f(BCLK) = 20 MHz) (M16C/28, M16C/28B) Vcc = 2.7 V to 5.5 V (f(BCLK) = 10 MHz) (M16C/28, M16C/28B)
	Power consumption	16 mA (Vcc = 5V, f(BCLK) = 20 MHz) 25 µA (f(XCIN) = 32 KHz on RAM) 3.0 µA (Vcc = 3V, f(XCIN) = 32 KHz, in wait mode) 0.7 µA (Vcc = 3V, in stop mode)
Flash Memory	Program/erase supply voltage	2.7 V to 5.5 V
	Program and erase endurance	100 times (all space) or 1,000 times (Blocks 0 to 5) /10,000 times (Block A, Block B(3))
Operating Ambient Temperature		-20 to 85°C/-40 to 85°C(3)
Package		80-pin plastic mold LQFP, 85-pin plastic mold TFLGA

NOTES:
1. I^2C bus is a trademark of Koninklijke Philips Electronics N. V.
2. IEBus is a trademark of NEC Electronics Corporation.
3. Refer to **Table 1.5** to **1.7** for number of program/erase.
4. Use PLL frequency synthesizer to use M16C/28B at f(BCLK) = 24 MHz.

1.3 Block Diagram

Figure 1.1 is a block diagram of the M16C/28 Group (M16C/28, M16C/28B), 80-pin and 85-pin package.
Figure 1.2 is a block diagram of the M16C/28 Group (M16C/28, M16C/28B), 64-pin package.

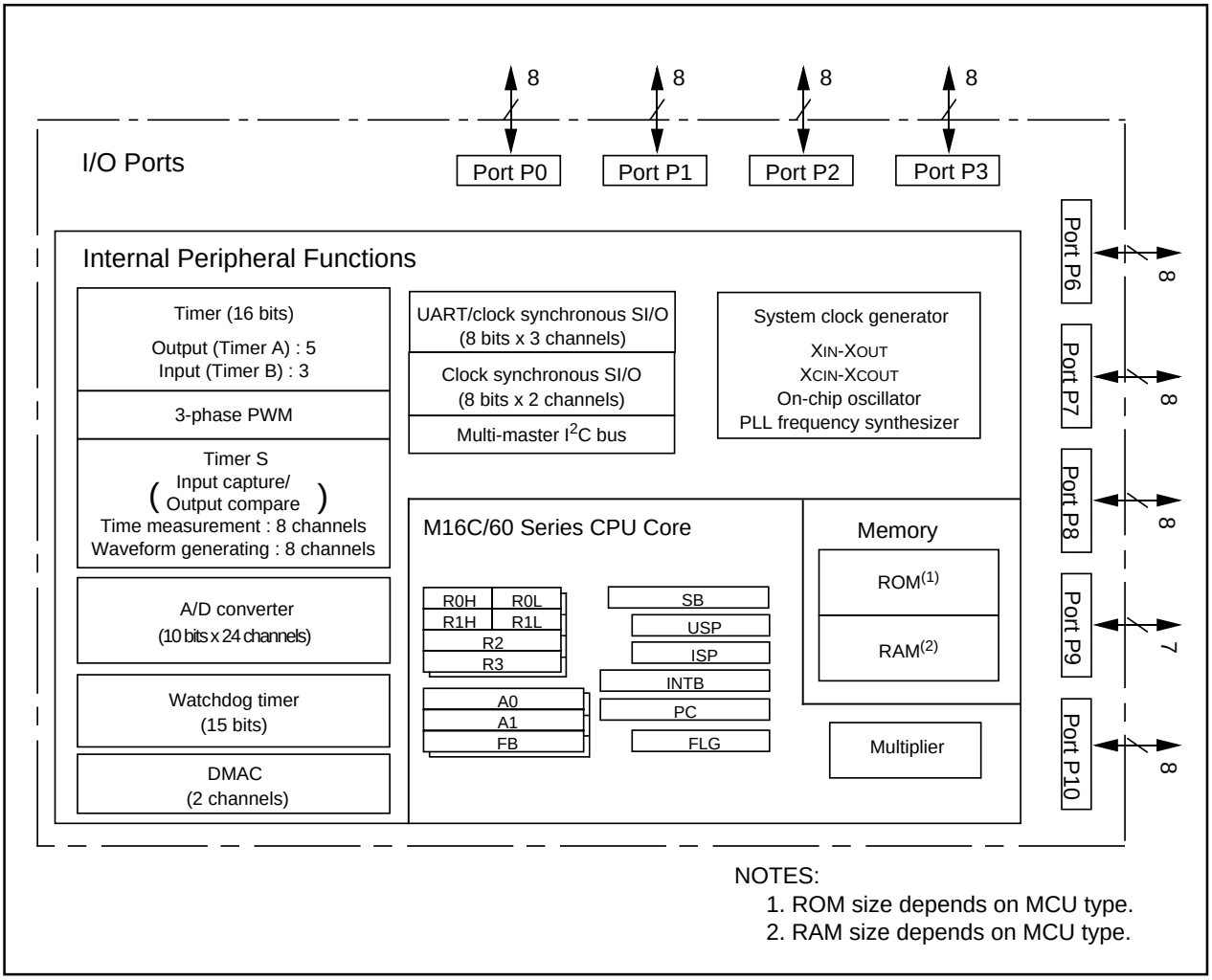


Figure 1.1 M16C/28 Group (M16C/28, M16C/28B), 80-Pin/85-Pin Block Diagram

1.4 Product Information

Tables 1.3 and **1.4** list the M16C/28 Group product information and **Figure 1.3** shows the product numbering system. The specifications are partially different between normal-ver.and T/ V-ver..

Table 1.3 M16C/28 Product List -Normal-ver. **As of September, 2006**

Type Number	ROM Capacity	RAM Capacity	Package Type	Remarks	Product Code
M30280F6WG (N)	48 K + 4 K	4 K	PTLG0085JB-A (85F0G)	Flash Memory	U3, U5, U7, U9
M30280F8WG (N)	64 K + 4 K	4 K			
M30280FAWG (N)	96 K + 4 K	8 K			
M30280F6HP (N)	48 K + 4 K	4 K	PLQP0080KB-A (80P6Q-A)		
M30280F8HP (N)	64 K + 4 K	4 K			
M30280FAHP (N)	96 K + 4 K	8 K			
M30280FCHP (N)	128 K + 4 K	12 K			
M30281F6HP (N)	48 K + 4 K	4 K	PLQP0064KB-A (64P6Q-A)		
M30281F8HP (N)	64 K + 4 K	4 K			
M30281FAHP (N)	96 K + 4 K	8 K			
M30281FCHP (N)	128 K + 4 K	12 K			
M30280M8-XXXHP (N)	64 K	4 K	PLQP0080KB-A (80P6Q-A)	Mask ROM	U3, U5
M30280MA-XXXHP (N)	96 K	8 K			
M30280MC-XXXHP (N)	128 K	12 K			
M30281M8-XXXHP (N)	64 K	4 K	PLQP0064KB-A (64P6Q-A)		
M30281MA-XXXHP (N)	96 K	8 K			
M30281MC-XXXHP (N)	128 K	12 K			

(N): New

Table 1.4 M16C/28B Product List -Normal-ver. **As of September, 2006**

Type Number	ROM Capacity	RAM Capacity	Package Type	Remarks	Product Code
M30280FCBHP (D)	128 K + 4 K	12 K	PLQP0080KB-A (80P6Q-A)	Flash memory	U7
M30281FCBHP (D)	128 K + 4 K	12 K	PLQP0064KB-A (64P6Q-A)		

(D): Under development

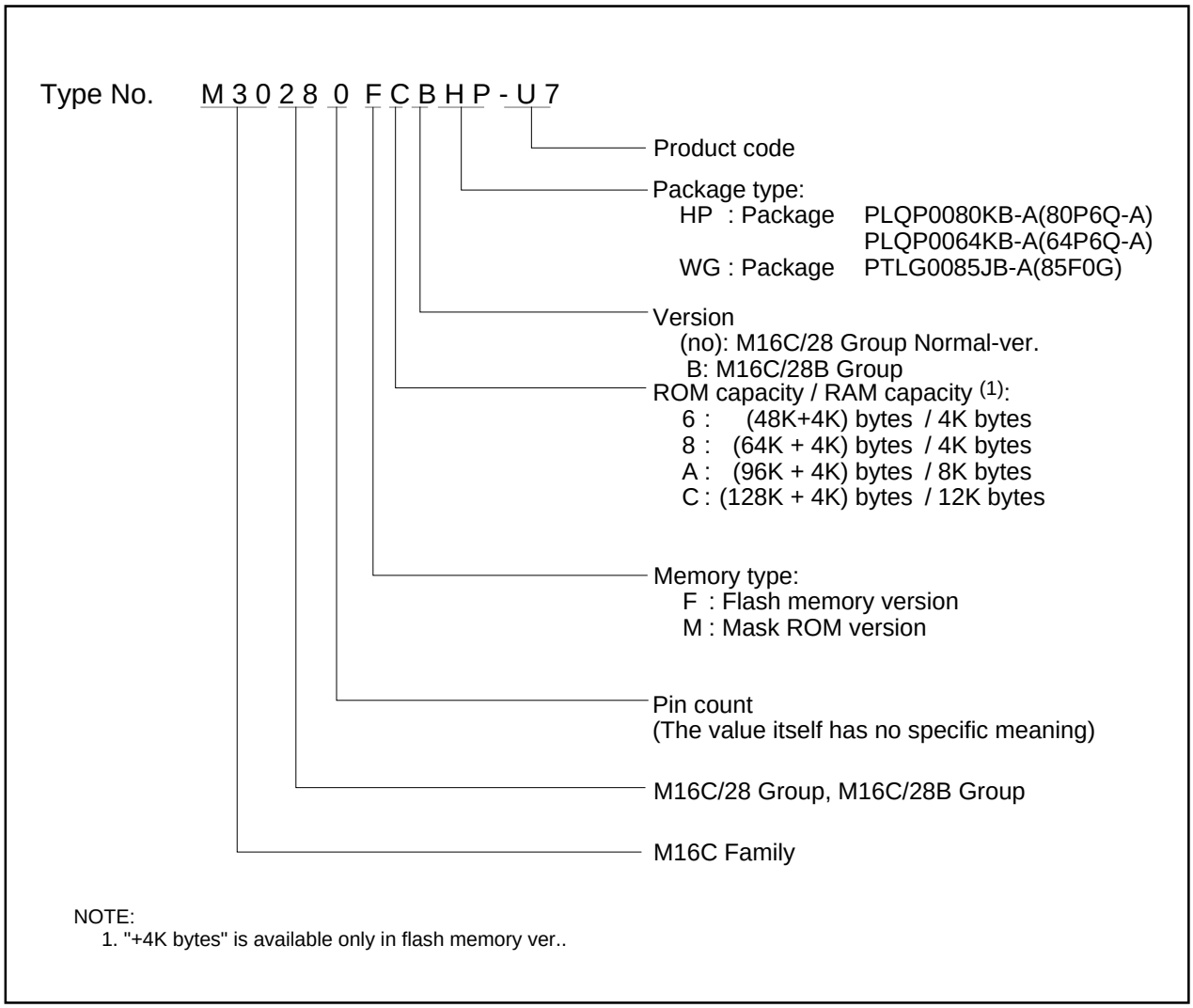
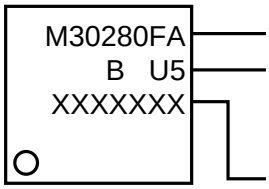


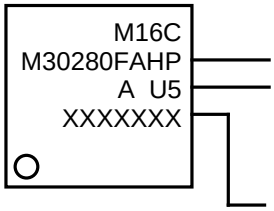
Figure 1.3 Product Numbering System

(1) Flash Memory Version, PTLG0085JB-A (85F0G), Normal-ver.



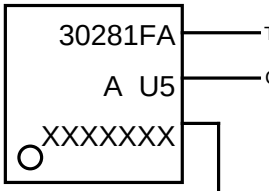
Type No. M30280FAWG
Chip version and product code
B : Chip version.
The first edition is shown to be blank and continues with A, B, and C.
U5 : Product code. (See **Table 1.5**)
Date code seven digits
Manufacturing management code

(2) Flash Memory Version, PLQP0080KB-A (80P6Q-A), Normal-ver.



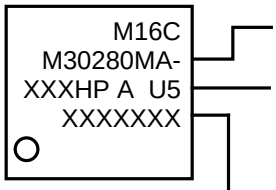
Type No. M30280FAHP
Chip version and product code
A : Chip version and product code(1)
The first edition is shown to be blank and continues with A, B and C.
U5 : Product code. (**Table 1.4**)
Date code seven digits
Manufacturing management code

(3) Flash Memory Version, PLQP0064KB-A (64P6Q-A), Normal-ver.



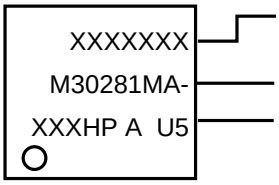
Type No. M30281FAHP
Chip version and product code
A : Chip version and product code(1)
The first edition is shown to be blank and continues with A, B and C.
U5 : Product code. (**Table 1.4**)
Date code seven digits
Manufacturing management code

(4) Mask ROM Version, PLQP0080KB-A (80P6Q-A), Normal-ver.



Type No. M30280MAHP
Chip version and product code
XXX : ROM No.
A : Chip version and product code(1)
The first edition is shown to be blank and continues with A, B and C.
U5 : Product code. (**Table 1.6**)
Date code seven digits
Manufacturing management code

(5) Mask ROM Version, PLQP0064-KB-A (64P6Q-A), Normal-ver.



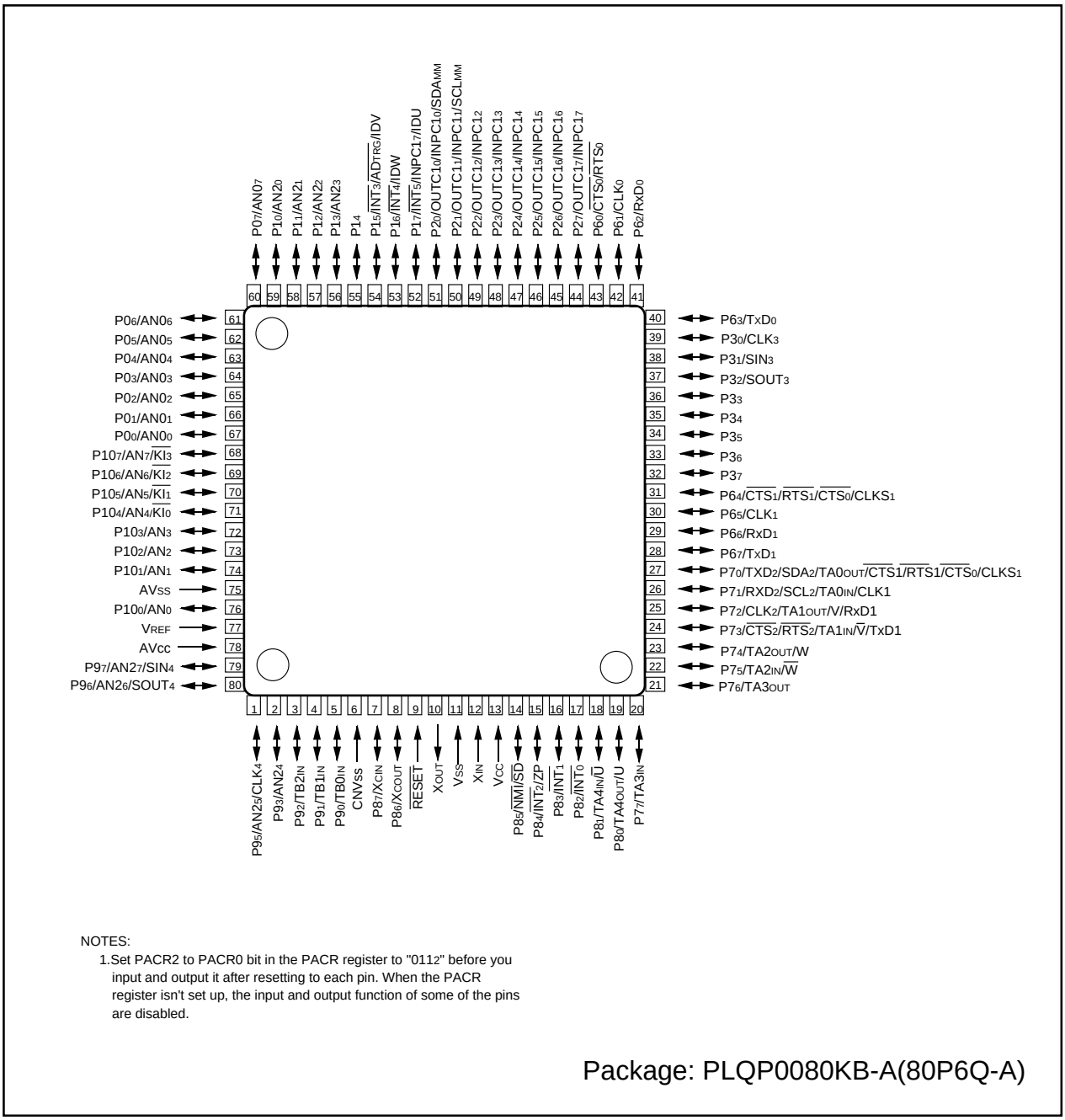
Date code seven digits
Manufacturing management code
Type No. M30281MAHP
Chip version and product code
XXX: ROM No.
A : Chip version and product code(1)
The first edition is shown to be blank and continues with A, B and C.
U5 : Product code. (**Table 1.6**)

NOTES:
1. The following functinos are not available in the first version and version A products.
-Delay trigger mode 0 of A/D conversion
-Delay trigger mode 1 of A/D conversion

Figure 1.4 Marking Diagram-M16C/28 Normal-ver.

Table 1.8 Pin Characteristics for 85-pin Package

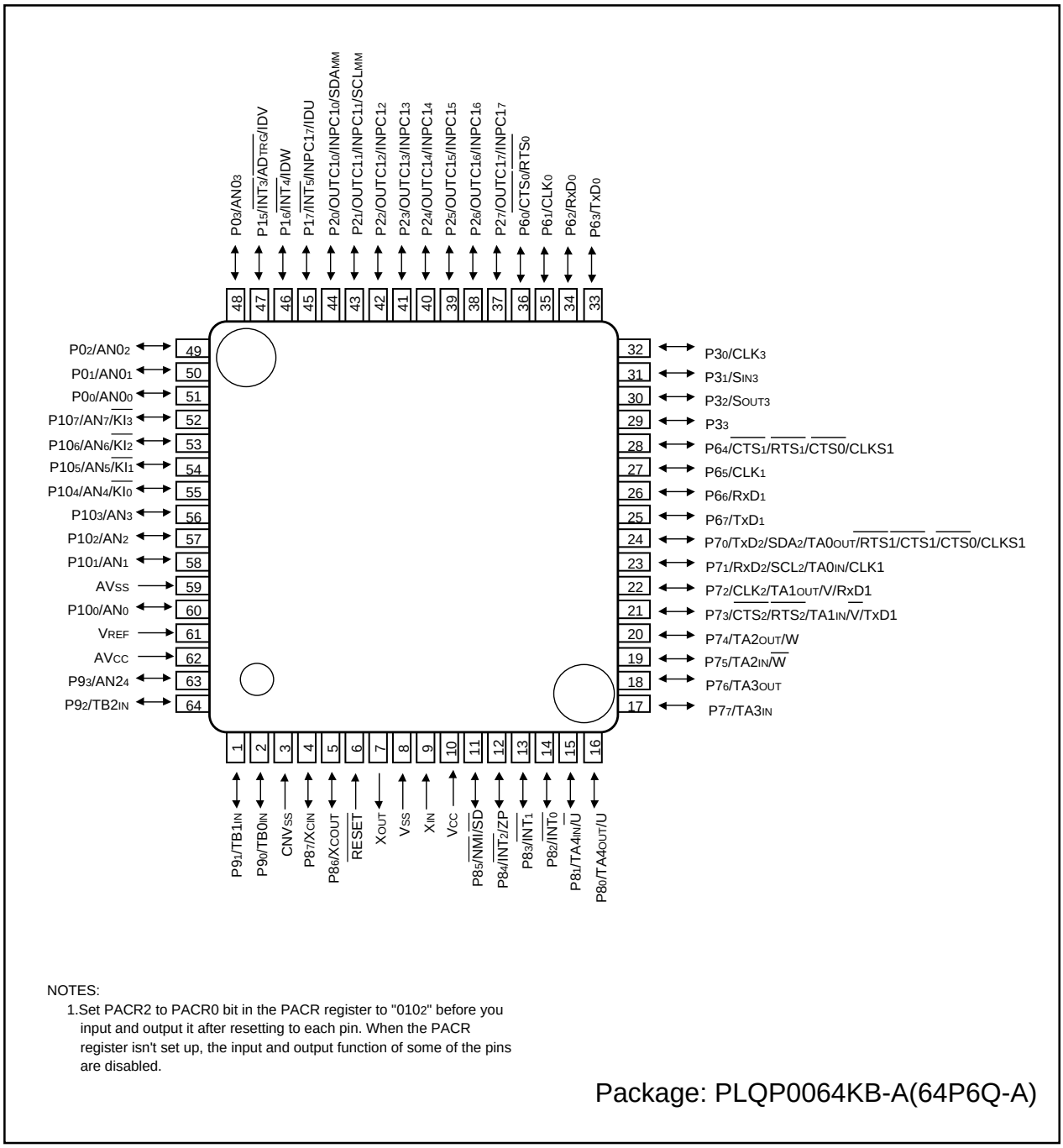
Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	Timer S Pin	UART Pin	Multi-master I^2C bus Pin	Analog Pin	PLQP0080KB-A Pin Number
A1		$P9_5$				CLK_4		$AN2_5$	1
A2		$P9_6$				$SOUT_4$		$AN2_6$	80
A3	AVcc								78
A4	V_{REF}								77
A5		$P10_1$						AN_1	74
A6		$P10_5$	$\overline{KI}_1$					AN_5	70
A7		$P0_0$						$AN0_0$	67
A8		$P0_3$						$AN0_3$	64
A9		$P0_5$						$AN0_5$	62
A10		$P0_6$						$AN0_6$	61
B1		$P9_2$		TB_{2IN}					3
B2		$P9_3$						$AN2_4$	2
B3		$P9_7$				SIN_4		$AN2_7$	79
B4		$P10_0$						AN_0	76
B5		$P10_2$						AN_2	73
B6		$P10_4$	$\overline{KI}_0$					AN_4	71
B7		$P10_7$	$\overline{KI}_3$					AN_7	68
B8		$P0_2$						$AN0_2$	65
B9		$P0_4$						$AN0_4$	63
B10		$P0_7$						$AN0_7$	60
C1	CNVss								6
C2		$P9_0$		TB_{0IN}					5
C3		$P9_1$		TB_{1IN}					4
C4	AVss								75
C5		$P10_3$						AN_3	72
C6	V_{SS}(1)								(11)
C7		$P10_6$	$\overline{KI}_2$					AN_6	69
C8		$P0_1$						$AN0_1$	66
C9		$P1_0$						$AN2_0$	59
C10		$P1_1$						$AN2_1$	58
D1	X_{COUT}	$P8_6$							8
D2	X_{CIN}	$P8_7$							7
D3	$\overline{RESET}$								9
D4	V_{SS}(1)								(11)
D8		$P1_2$						$AN2_2$	57
D9		$P1_3$						$AN2_3$	56
D10		$P1_4$							55
E1	X_{OUT}								10
E2	X_{IN}								12
E3	Vss								11



NOTES:
1. Set PACR2 to PACR0 bit in the PACR register to "011₂" before you input and output it after resetting to each pin. When the PACR register isn't set up, the input and output function of some of the pins are disabled.

Package: PLQP0080KB-A(80P6Q-A)

Figure 1.5 Pin Assignment (Top View) of 80-Pin Package



NOTES:
1. Set PACR2 to PACR0 bit in the PACR register to "010₂" before you input and output it after resetting to each pin. When the PACR register isn't set up, the input and output function of some of the pins are disabled.

Package: PLQP0064KB-A(64P6Q-A)

Figure 1.6 Pin Assignment (Top View) of 64-Pin Package

Table 1.10 Pin Characteristics for 64-Pin Package

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	Timer S Pin	UART Pin	Mult-master I^2C bus Pin	Analog Pin
1		$P9_1$		TA_{1IN}				
2		$P9_0$		TB_{0IN}				
3	CNVss							
4	X_{CIN}	$P8_7$						
5	X_{COUT}	$P8_6$						
6	$\overline{RESET}$							
7	X_{OUT}							
8	Vss							
9	X_{IN}							
10	Vcc							
11		$P8_5$	$\overline{NMI}$	$\overline{SD}$				
12		$P8_4$	$\overline{INT_2}$	ZP				
13		$P8_3$	$\overline{INT_1}$					
14		$P8_2$	$\overline{INT_0}$					
15		$P8_1$		TA_{4IN} / $\overline{U}$				
16		$P8_0$		TA_{4OUT} / U				
17		$P7_7$		TA_{3IN}				
18		$P7_6$		TA_{3OUT}				
19		$P7_5$		TA_{2IN} / $\overline{W}$				
20		$P7_4$		TA_{2OUT} / W				
21		$P7_3$		TA_{1IN} / $\overline{V}$		$\overline{CTS_2}$ / $\overline{RTS_2}$ / TxD_1		
22		$P7_2$		TA_{1OUT} / V		CLK_2 / RxD_1		
23		$P7_1$		TA_{0IN}		RxD_2 / SCL_2 / CLK_1		
24		$P7_0$		TA_{0OUT}		TxD_2 / SDA_2 / $\overline{RTS_1}$ / $\overline{CTS_1}$ / $\overline{CTS_0}$ / $CLKS_1$		
25		$P6_7$				TxD_1		
26		$P6_6$				RxD_1		
27		$P6_5$				CLK_1		
28		$P6_4$				$\overline{RTS_1}$ / $\overline{CTS_1}$/ $\overline{CTS_0}$ / $CLKS_1$		
29		$P3_3$						
30		$P3_2$				$SOUT_3$		
31		$P3_1$				SIN_3		
32		$P3_0$				CLK_3		
33		$P6_3$				TxD_0		
34		$P6_2$				RxD_0		
35		$P6_1$				CLK_0		
36		$P6_0$				$\overline{RTS_0}$ / $\overline{CTS_0}$		
37		$P2_7$			$OUTC1_7$ / $INPC1_7$			
38		$P2_6$			$OUTC1_6$ / $INPC1_6$			
39		$P2_5$			$OUTC1_5$ / $INPC1_5$			
40		$P2_4$			$OUTC1_4$ / $INPC1_4$			

Table 1.10 Pin Description (80-Pin and 85-Pin Packages only) (Continued)

Classification	Symbol	I/O Type	Function
Serial I/O	CLK4	I/O	Inputs and outputs the transfer clock
	SIN4	I	Inputs serial data
	SOUT4	O	Outputs serial data
A/D Converter	AN04 to AN07 AN20 to AN23 AN25 to AN27	I	Analog input pins for the A/D converter
I/O Ports	P04 to P07 P10 to P14 P34 to P37	I/O	I/O ports for CMOS. Each port can be programmed for input or output under the control of the direction register. An input port can be set, by program, for a pull-up resistor available or for no pull-up resister available in 4-bit units
	P95 to P97	I/O	I/O ports having equivalent functions to P0

I : Input O : Output I/O : Input and output

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers. The register bank is comprised of 7 registers (R0, R1, R2, R3, A0, A1 and FB) out of 13 CPU registers. Two sets of register banks are provided.

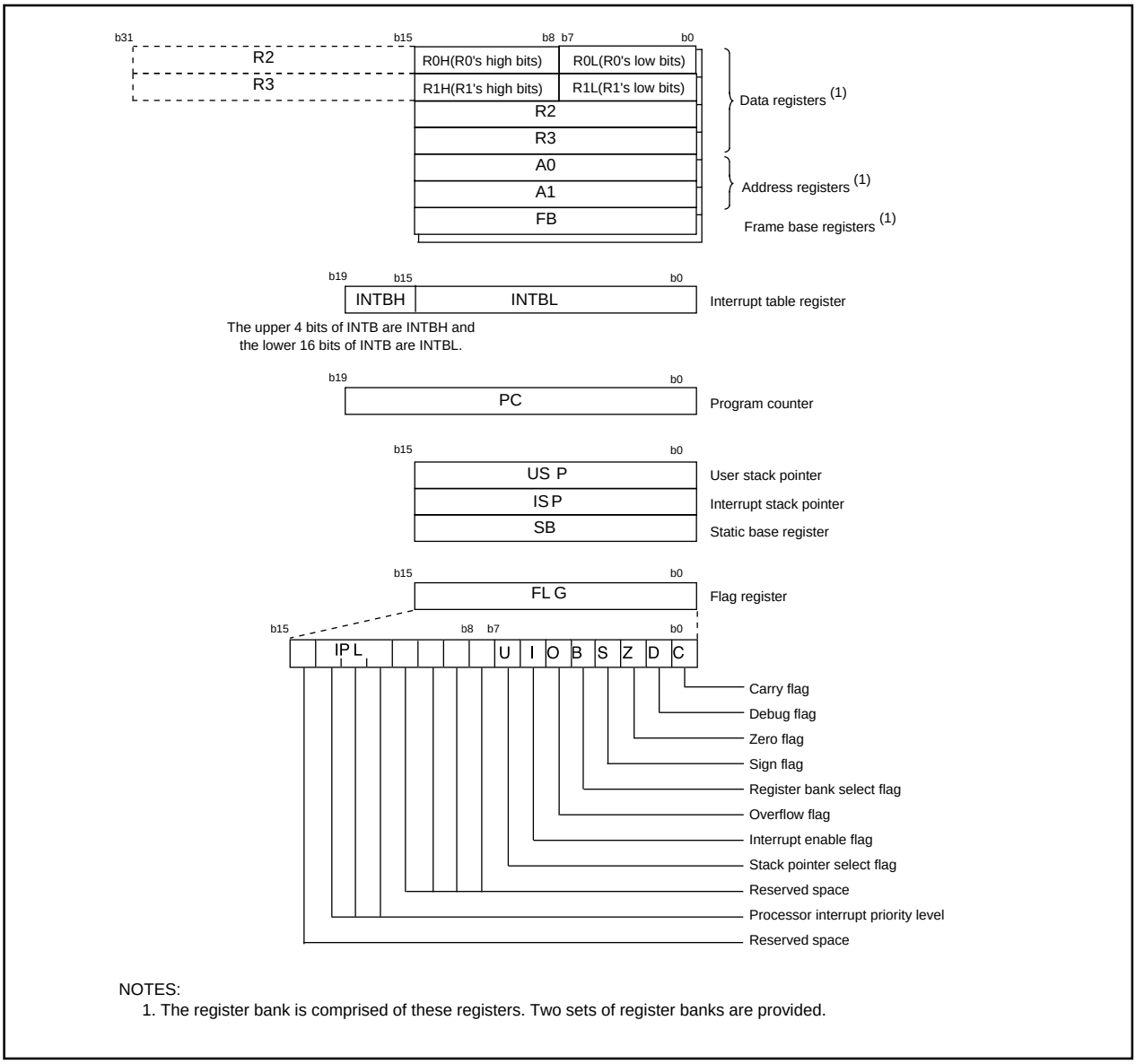


Figure 2.1 Central Processing Unit Register

2.1 Data Registers (R0, R1, R2 and R3)

The R0, R1, R2 and R3 registers are 16 bit registers for transfer and arithmetic/logic operations.

The R0 and R1 registers can be split into high-order bits(R0H, R1H) and low-order bits (R0L, R1L) to be used seperately as 8-bit data registers. Conversely, R2 and R0 can be combined with R2 to be used as a 32-bit data register (R2R0). The same applies to R1 and R2.

2.2 Address Registers (A0 and A1)

The register A0 consists of 16 bits, and is used for address register indirect addressing and address register relative addressing. They also are used for transfers and arithmetic/logic operations. A1 is the same as A0. In some instructions, registers A1 and A0 can be combined for use as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is configured with 16 bits, and is used for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is configured with 20 bits, indicating the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC is configured with 20 bits, indicating the address of an instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

Stack pointer (SP) comes in two types: USP and ISP, each configured with 16 bits.

Your desired type of stack pointer (USP or ISP) can be selected by the U flag of FLG.

2.7 Static Base Register (SB)

SB is configured with 16 bits, and is used for SB relative addressing.

2.8 Flag Register (FLG)

FLG consists of 11 bits, indicating the CPU status.

2.8.1 Carry Flag (C Flag)

This flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic/logic unit.

2.8.2 Debug Flag (D Flag)

The D flag is used exclusively for debugging purpose. During normal use, it must be set to 0.

2.8.3 Zero Flag (Z Flag)

This flag is set to 1 when an arithmetic operation resulted in 0; otherwise, it is 0.

2.8.4 Sign Flag (S Flag)

This flag is set to 1 when an arithmetic operation resulted in a negative value; otherwise, it is 0.

2.8.5 Register Bank Select Flag (B Flag)

Register bank 0 is selected when this flag is 0 ; register bank 1 is selected when this flag is 1.

2.8.6 Overflow Flag (O Flag)

This flag is set to 1 when the operation resulted in an overflow; otherwise, it is 0.

2.8.7 Interrupt Enable Flag (I Flag)

This flag enables a maskable interrupt.

Maskable interrupts are disabled when the I flag is 0, and are enabled when the I flag is 1. The I flag is cleared to 0 when the interrupt request is accepted.

2.8.8 Stack Pointer Select Flag (U Flag)

ISP is selected when the U flag is 0; USP is selected when the U flag is 1.

The U flag is cleared to 0 when a hardware interrupt request is accepted or an INT instruction for software interrupt Nos. 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is configured with three bits, for specification of up to eight processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has priority greater than IPL, the interrupt is enabled.

2.8.10 Reserved Area

When write to this bit, write 0. When read, its content is indeterminate.

3. Memory

Figure 3.1 is a memory map of the M16C/28 Group (M16C/28, M16C/28B). M16C/28 Group provides 1-Mbyte address space from addresses 00000_{16} to $FFFFF_{16}$. The internal ROM is allocated lower addresses beginning with address $FFFFF_{16}$. For example, 64 Kbytes internal ROM is allocated addresses $F0000_{16}$ to $FFFFF_{16}$.

Two 2-Kbyte internal ROM areas, block A and block B, are available in the flash memory version. The blocks are allocated addresses $F000_{16}$ to $FFFF_{16}$.

The fixed interrupt vector tables are allocated addresses $FFFDC_{16}$ to $FFFFF_{16}$. It stores the starting address of each interrupt routine. See the section on interrupts for details.

The internal RAM is allocated higher addresses beginning with address 00400_{16}. For example, 4-Kbytes internal RAM is allocated addresses 00400_{16} to $013FF_{16}$. Besides storing data, it becomes stacks when the subroutine is called or an interrupt is acknowledged.

SFR, consisting of control registers for peripheral functions such as I/O port, A/D converter, serial I/O, timers is allocated addresses 00000_{16} to $003FF_{16}$. All blank spaces within SFR are reserved and cannot be accessed by users.

The special page vector table is allocated to the addresses $FFE00_{16}$ to $FFFDB_{16}$. This vector is used by the JMPS or JSRS instruction. For details, refer to the ***M16C/60 and M16C/20 Series Software Manual***.

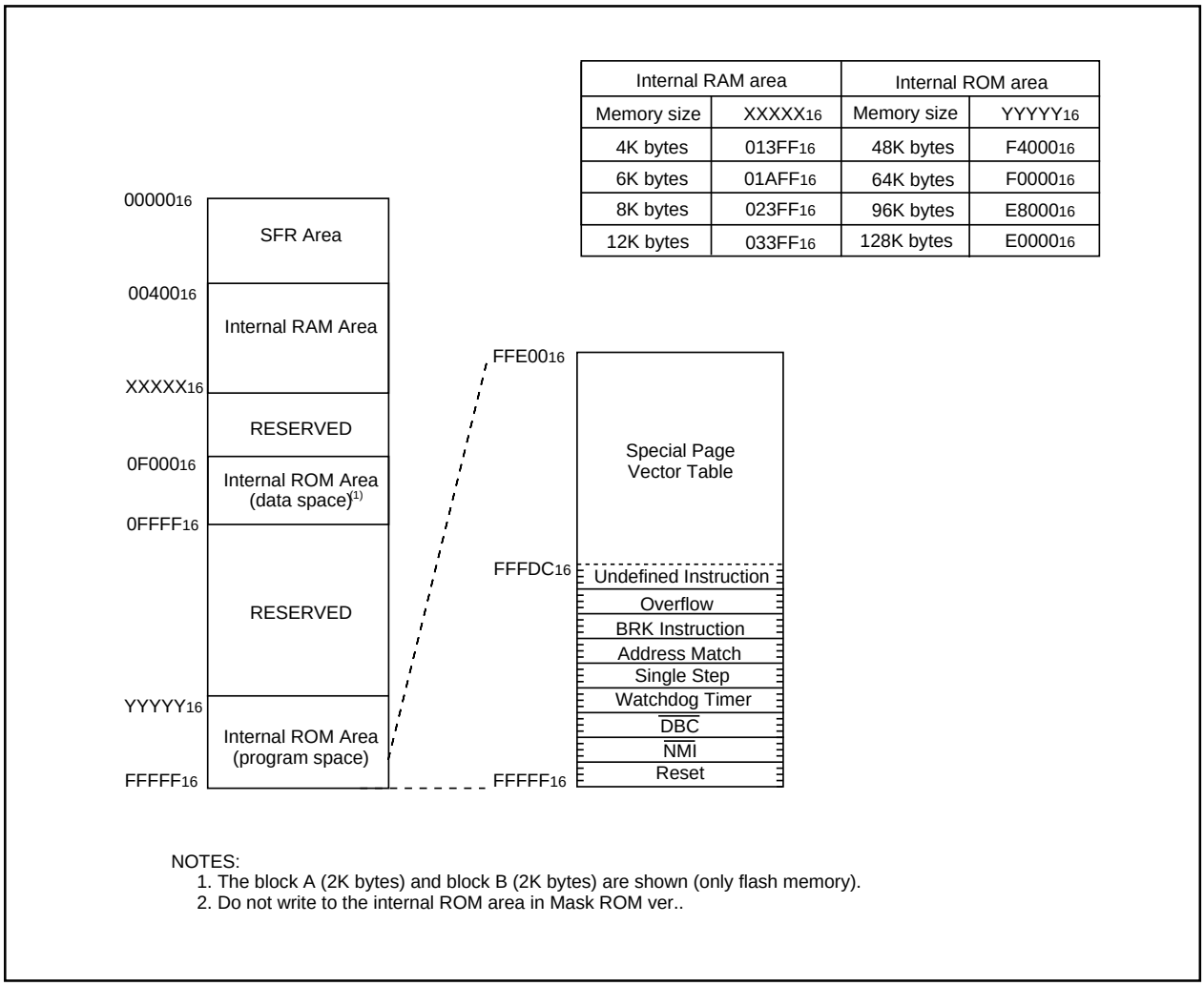


Figure 3.1 Memory Map

Table 4.4 SFR Information(4)(1)

Address	Register	Symbol	After Reset
0300₁₆ 0301₁₆	TM, WG register 0	G1TM0, G1PO0	XX16 XX16
0302₁₆ 0303₁₆	TM, WG register 1	G1TM1, G1PO1	XX16 XX16
0304₁₆ 0305₁₆	TM, WG register 2	G1TM2, G1PO2	XX16 XX16
0306₁₆ 0307₁₆	TM, WG register 3	G1TM3, G1PO3	XX16 XX16
0308₁₆ 0309₁₆	TM, WG register 4	G1TM4, G1PO4	XX16 XX16
030A₁₆ 030B₁₆	TM, WG register 5	G1TM5, G1PO5	XX16 XX16
030C₁₆ 030D₁₆	TM, WG register 6	G1TM6, G1PO6	XX16 XX16
030E₁₆ 030F₁₆	TM, WG register 7	G1TM7, G1PO7	XX16 XX16
0310₁₆	WG control register 0	G1POCR0	0X00XX002
0311₁₆	WG control register 1	G1POCR1	0X00XX002
0312₁₆	WG control register 2	G1POCR2	0X00XX002
0313₁₆	WG control register 3	G1POCR3	0X00XX002
0314₁₆	WG control register 4	G1POCR4	0X00XX002
0315₁₆	WG control register 5	G1POCR5	0X00XX002
0316₁₆	WG control register 6	G1POCR6	0X00XX002
0317₁₆	WG control register 7	G1POCR7	0X00XX002
0318₁₆	TM control register 0	G1TMCR0	0016
0319₁₆	TM control register 1	G1TMCR1	0016
031A₁₆	TM control register 2	G1TMCR2	0016
031B₁₆	TM control register 3	G1TMCR3	0016
031C₁₆	TM control register 4	G1TMCR4	0016
031D₁₆	TM control register 5	G1TMCR5	0016
031E₁₆	TM control register 6	G1TMCR6	0016
031F₁₆	TM control register 7	G1TMCR7	0016
0320₁₆ 0321₁₆	Base timer register	G1BT	XX16 XX16
0322₁₆	Base timer control register 0	G1BCR0	0016
0323₁₆	Base timer control register 1	G1BCR1	0016
0324₁₆	TM prescale register 6	G1TPR6	0016
0325₁₆	TM prescale register 7	G1TPR7	0016
0326₁₆	Function enable register	G1FE	0016
0327₁₆	Function select register	G1FS	0016
0328₁₆ 0329₁₆	Base timer reset register	G1BTRR	XX16 XX16
032A₁₆	Divider register	G1DV	0016
032B₁₆			
032C₁₆			
032D₁₆			
032E₁₆			
032F₁₆			
0330₁₆	Interrupt request register	G1IR	XX16
0331₁₆	Interrupt enable register 0	G1IE0	0016
0332₁₆	Interrupt enable register 1	G1IE1	0016
0333₁₆			
0334₁₆			
0335₁₆			
0336₁₆			
0337₁₆			
0338₁₆			
0339₁₆			
033A₁₆			
033B₁₆			
033C₁₆			
033D₁₆			
033E₁₆	NMI digital debounce register	NDDR	FF16
033F₁₆	P17 digital debounce register	P17DDR	FF16

Note 1:The blank spaces are reserved. No access is allowed.

X : Undefined

Table 4.5 SFR Information(5)(1)

Address	Register	Symbol	After Reset
034016			
034116			
034216	Timer A1-1 register	TA11	XX16
034316			XX16
034416	Timer A2-1 register	TA21	XX16
034516			XX16
034616	Timer A4-1 register	TA41	XX16
034716			XX16
034816	Three-phase PWM control register 0	INVC0	0016
034916	Three-phase PWM control register 1	INVC1	0016
034A16	Three-phase output buffer register 0	IDB0	001111112
034B16	Three-phase output buffer register 1	IDB1	001111112
034C16	Dead time timer	DTT	XX16
034D16	Timer B2 interrupt occurrence frequency set counter	ICTB2	XX16
034E16	Position-data-retain function control register	PDRF	XXXX00002
034F16			
035016			
035116			
035216			
035316			
035416			
035516			
035616			
035716			
035816			
035916			
035A16			
035B16			
035C16			
035D16			
035E16	Interrupt request cause select register 2	IFSR2A	00XXXXX02(2)
035F16	Interrupt request cause select register	IFSR	0016
036016	SI/O3 transmit/receive register	S3TRR	XX16
036116			
036216	SI/O3 control register	S3C	010000002
036316	SI/O3 bit rate generator	S3BRG	XX16
036416	SI/O4 transmit/receive register	S4TRR	XX16
036516			
036616	SI/O4 control register	S4C	010000002
036716	SI/O4 bit rate generator	S4BRG	XX16
036816			
036916			
036A16			
036B16			
036C16			
036D16			
036E16			
036F16			
037016			
037116			
037216			
037316			
037416	UART2 special mode register 4	U2SMR4	0016
037516	UART2 special mode register 3	U2SMR3	000X0X0X2
037616	UART2 special mode register 2	U2SMR2	X0000000 2
037716	UART2 special mode register	U2SMR	X0000000 2
037816	UART2 transmit/receive mode register	U2MR	0016
037916	UART2 bit rate generator	U2BRG	XX16
037A16	UART2 transmit buffer register	U2TB	XX16
037B16			XX16
037C16	UART2 transmit/receive control register 0	U2C0	000010002
037D16	UART2 transmit/receive control register 1	U2C1	000000102
037E16	UART2 receive buffer register	U2RB	XX16
037F16			XX16

Note 1: The blank spaces are reserved. No access is allowed.
Note 2: Write 1 to bit 0 after reset.

X : Undefined

Table 4.7 SFR Information(7)(1)

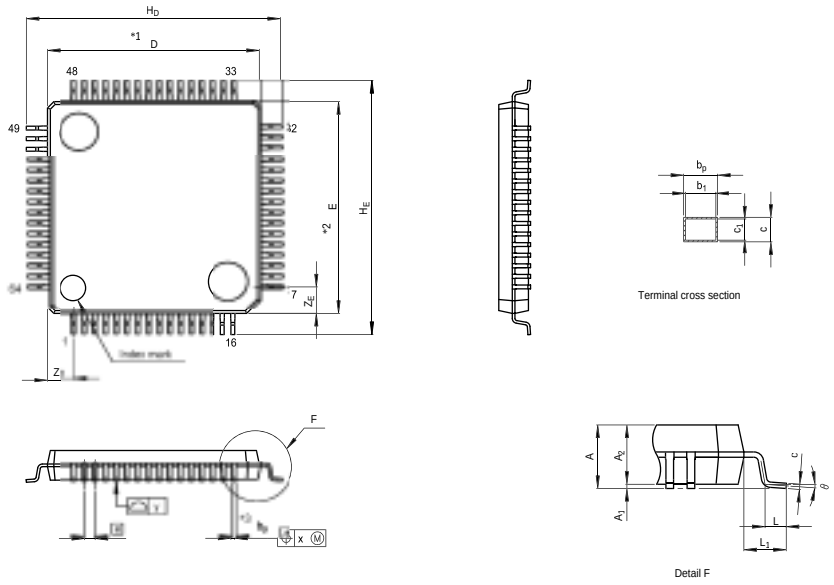
Address	Register	Symbol	After Reset
03C0₁₆	A/D register 0	AD0	XX₁₆
03C1₁₆			XX₁₆
03C2₁₆	A/D register 1	AD1	XX₁₆
03C3₁₆			XX₁₆
03C4₁₆	A/D register 2	AD2	XX₁₆
03C5₁₆			XX₁₆
03C6₁₆	A/D register 3	AD3	XX₁₆
03C7₁₆			XX₁₆
03C8₁₆	A/D register 4	AD4	XX₁₆
03C9₁₆			XX₁₆
03CA₁₆	A/D register 5	AD5	XX₁₆
03CB₁₆			XX₁₆
03CC₁₆	A/D register 6	AD6	XX₁₆
03CD₁₆			XX₁₆
03CE₁₆	A/D register 7	AD7	XX₁₆
03CF₁₆			XX₁₆
03D0₁₆			
03D1₁₆			
03D2₁₆	A/D trigger control register	ADTRGCON	00₁₆
03D3₁₆	A/D convert status register 0	ADSTAT0	00000X00₂
03D4₁₆	A/D control register 2	ADCON2	00₁₆
03D5₁₆			
03D6₁₆	A/D control register 0	ADCON0	00000XXX₂
03D7₁₆	A/D control register 1	ADCON1	00₁₆
03D8₁₆			
03D9₁₆			
03DA₁₆			
03DB₁₆			
03DC₁₆			
03DD₁₆			
03DE₁₆			
03DF₁₆			
03E0₁₆	Port P0 register	P0	XX₁₆
03E1₁₆	Port P1 register	P1	XX₁₆
03E2₁₆	Port P0 direction register	PD0	00₁₆
03E3₁₆	Port P1 direction register	PD1	00₁₆
03E4₁₆	Port P2 register	P2	XX₁₆
03E5₁₆	Port P3 register	P3	XX₁₆
03E6₁₆	Port P2 direction register	PD2	00₁₆
03E7₁₆	Port P3 direction register	PD3	00₁₆
03E8₁₆			
03E9₁₆			
03EA₁₆			
03EB₁₆			
03EC₁₆	Port P6 register	P6	XX₁₆
03ED₁₆	Port P7 register	P7	XX₁₆
03EE₁₆	Port P6 direction register	PD6	00₁₆
03EF₁₆	Port P7 direction register	PD7	00₁₆
03F0₁₆	Port P8 register	P8	XX₁₆
03F1₁₆	Port P9 register	P9	XX₁₆
03F2₁₆	Port P8 direction register	PD8	00₁₆
03F3₁₆	Port P9 direction register	PD9	000X0000₂
03F4₁₆	Port P10 register	P10	XX₁₆
03F5₁₆			
03F6₁₆	Port P10 direction register	PD10	00₁₆
03F7₁₆			
03F8₁₆			
03F9₁₆			
03FA₁₆			
03FB₁₆			
03FC₁₆	Pull-up control register 0	PUR0	00₁₆
03FD₁₆	Pull-up control register 1	PUR1	00₁₆
03FE₁₆	Pull-up control register 2	PUR2	00₁₆
03FF₁₆	Port control register	PCR	00₁₆

Note 1:The blank spaces are reserved. No access is allowed.

X : Undefined

Appendix 1. Package Dimensions

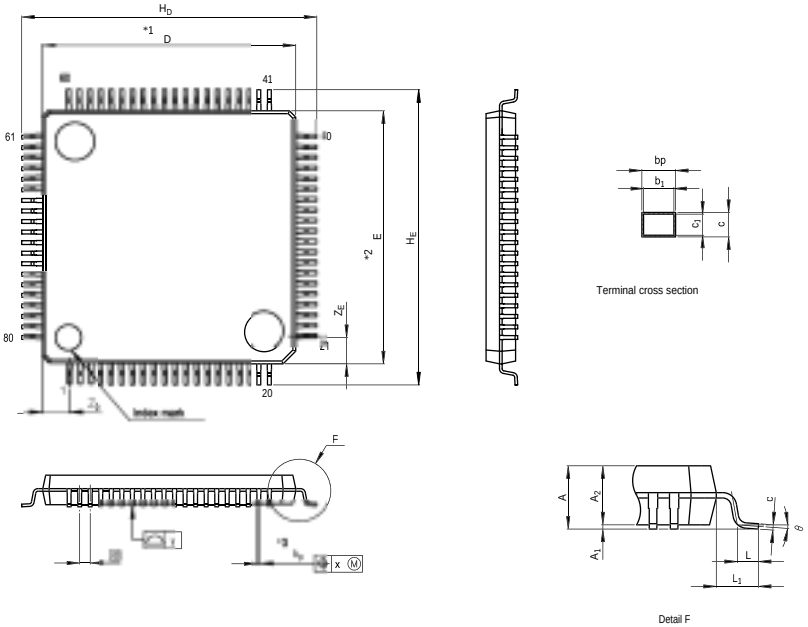
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP64-10x10-0.50	PLQP0064KB-A	64P6Q-A / FP-64K / FP-64KV	0.3g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP80-12x12-0.50	PLQP0080KB-A	80P6Q-A	0.5g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	11.9	12.0	12.1
E	11.9	12.0	12.1
A_2	—	1.4	—
H_D	13.8	14.0	14.2
H_E	13.8	14.0	14.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	10°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.3	0.5	0.7
L_1	—	1.0	—

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