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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	M16C/60
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, IEBus, SIO, UART/USART
Peripherals	DMA, POR, PWM, Voltage Detect, WDT
Number of I/O	71
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30280fchp-u7b

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1.3 Block Diagram

Figure 1.1 is a block diagram of the M16C/28 Group (M16C/28, M16C/28B), 80-pin and 85-pin package.
Figure 1.2 is a block diagram of the M16C/28 Group (M16C/28, M16C/28B), 64-pin package.

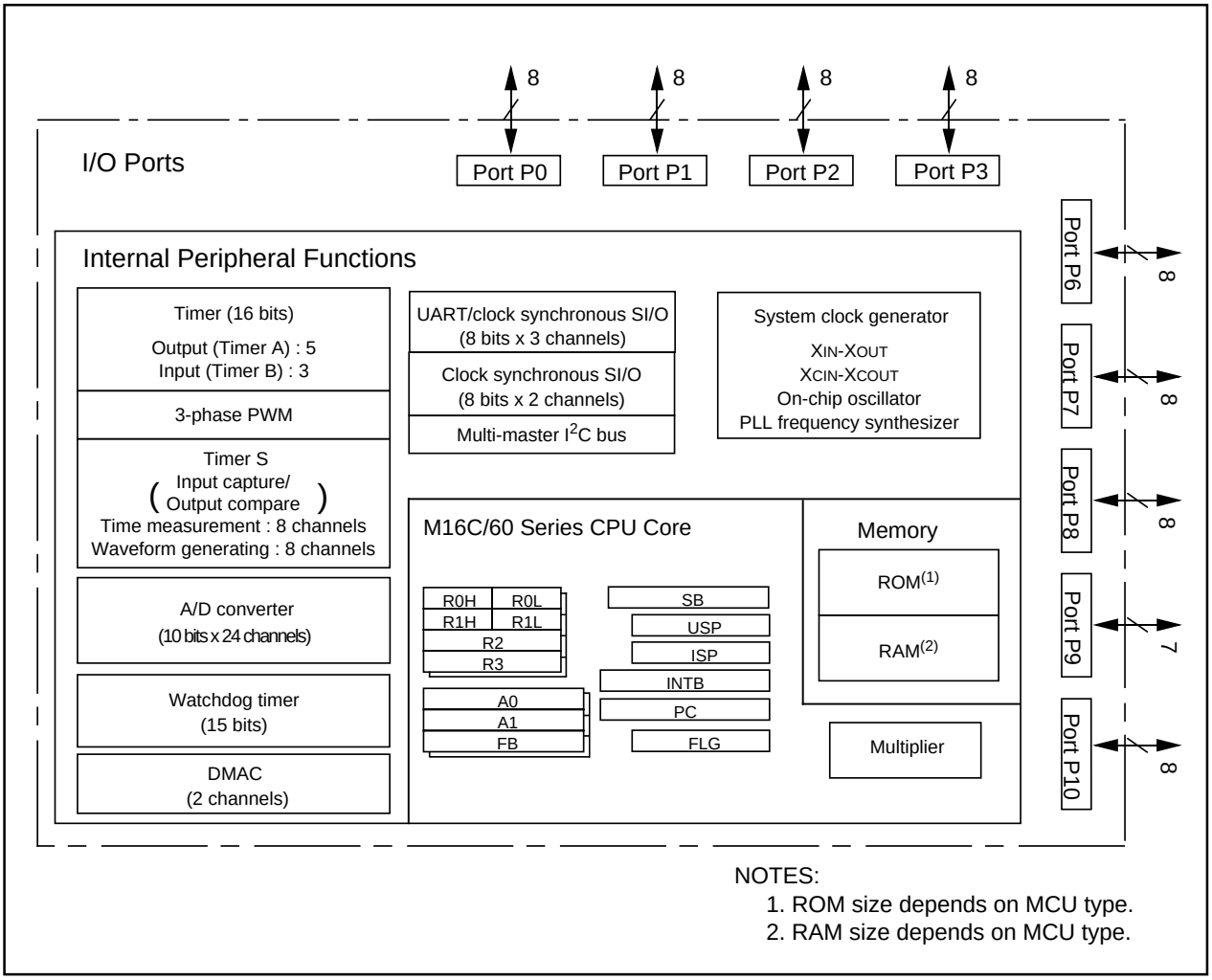


Figure 1.1 M16C/28 Group (M16C/28, M16C/28B), 80-Pin/85-Pin Block Diagram

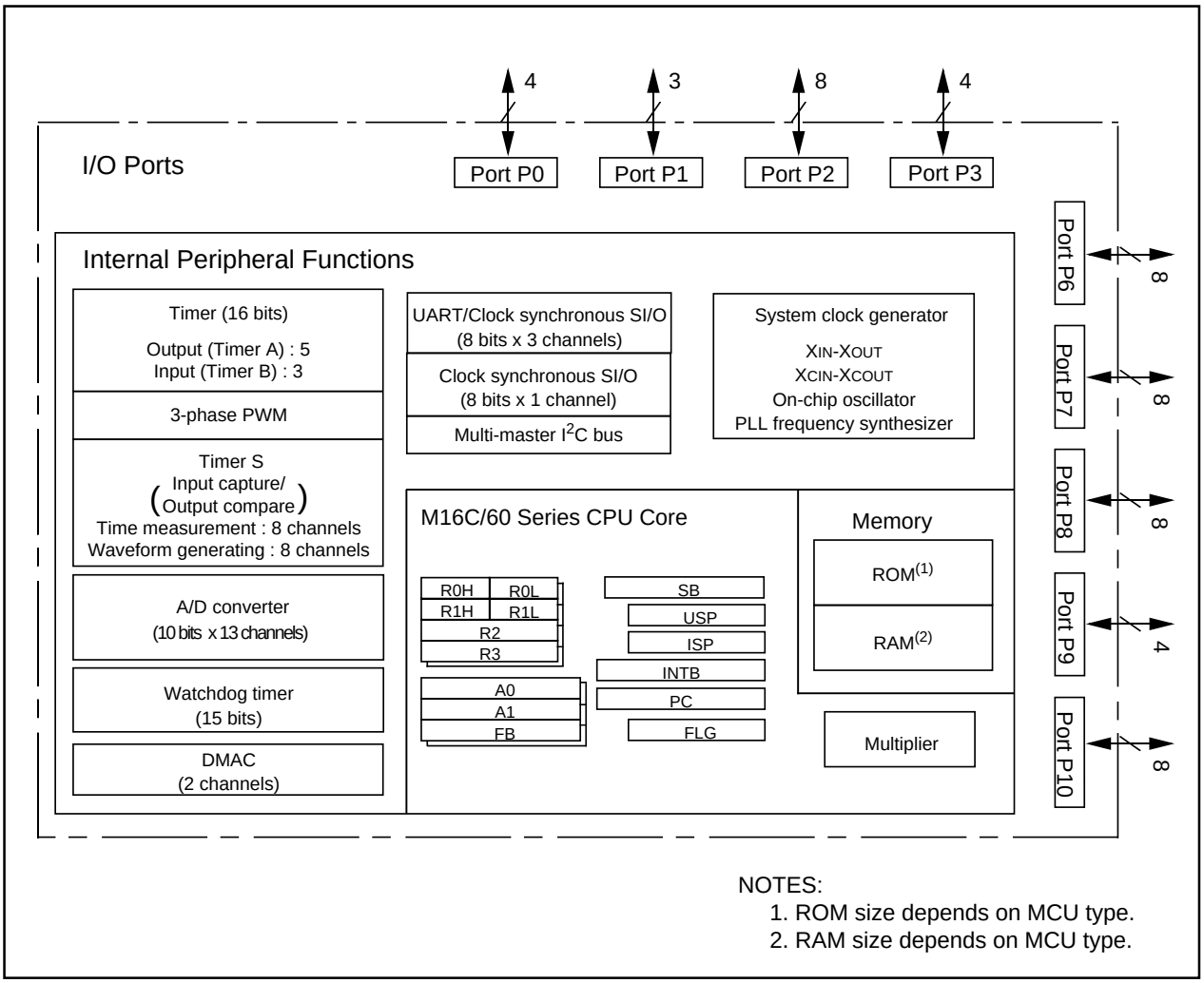


Figure 1.2 M16C/28 Group (M16C/28, M16C/28B), 64-Pin Block Diagram

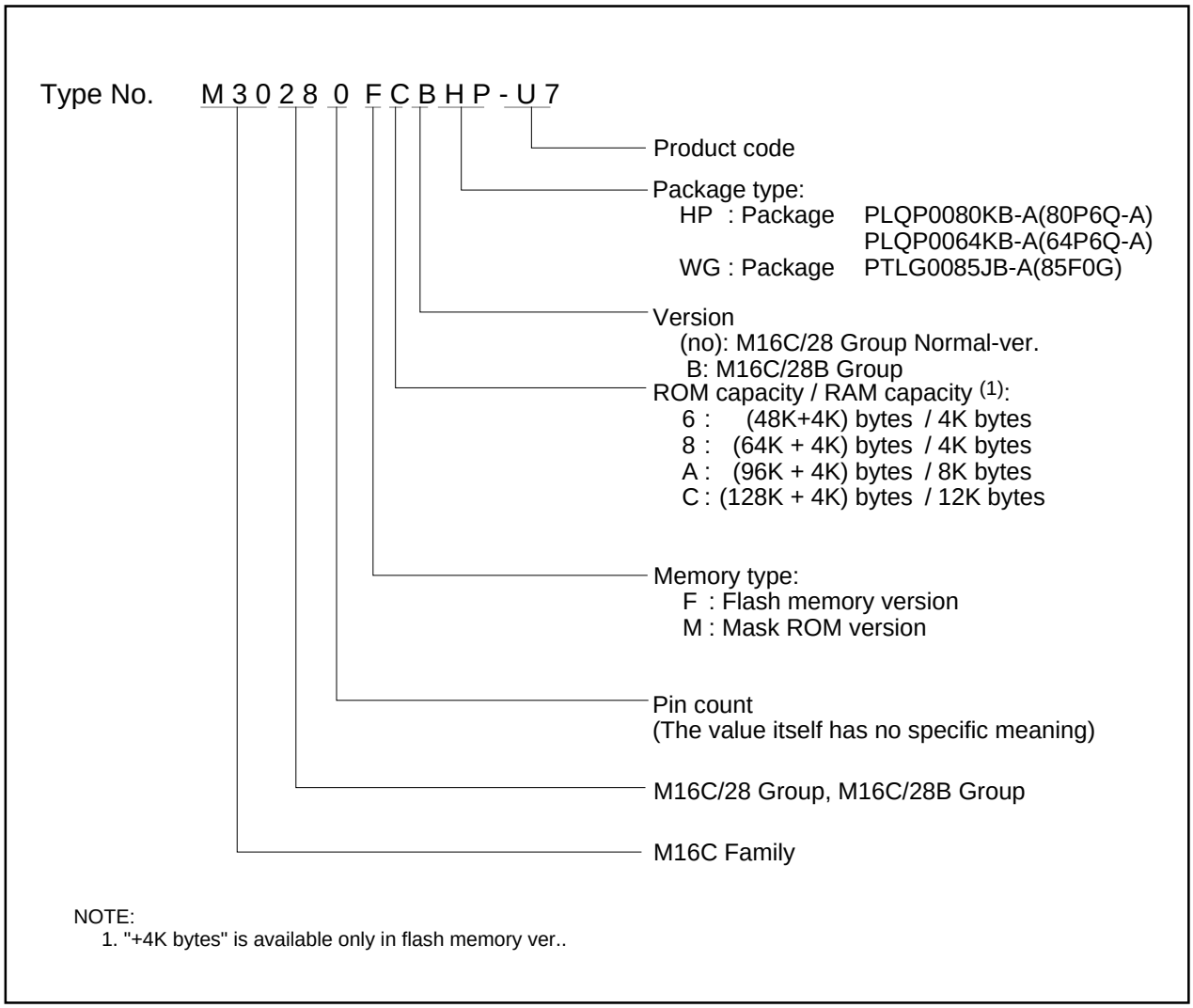
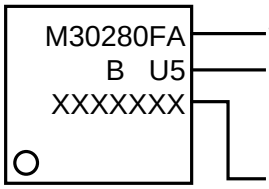


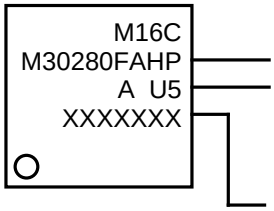
Figure 1.3 Product Numbering System

(1) Flash Memory Version, PTLG0085JB-A (85F0G), Normal-ver.



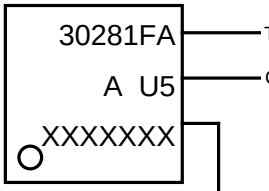
Type No. M30280FAWG
Chip version and product code
B : Chip version.
The first edition is shown to be blank and continues with A, B, and C.
U5 : Product code. (See **Table 1.5**)
Date code seven digits
Manufacturing management code

(2) Flash Memory Version, PLQP0080KB-A (80P6Q-A), Normal-ver.



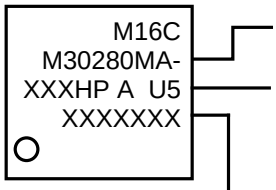
Type No. M30280FAHP
Chip version and product code
A : Chip version and product code(1)
The first edition is shown to be blank and continues with A, B and C.
U5 : Product code. (**Table 1.4**)
Date code seven digits
Manufacturing management code

(3) Flash Memory Version, PLQP0064KB-A (64P6Q-A), Normal-ver.



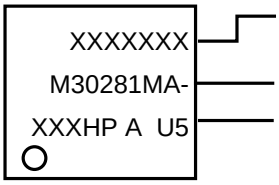
Type No. M30281FAHP
Chip version and product code
A : Chip version and product code(1)
The first edition is shown to be blank and continues with A, B and C.
U5 : Product code. (**Table 1.4**)
Date code seven digits
Manufacturing management code

(4) Mask ROM Version, PLQP0080KB-A (80P6Q-A), Normal-ver.



Type No. M30280MAHP
Chip version and product code
XXX : ROM No.
A : Chip version and product code(1)
The first edition is shown to be blank and continues with A, B and C.
U5 : Product code. (**Table 1.6**)
Date code seven digits
Manufacturing management code

(5) Mask ROM Version, PLQP0064-KB-A (64P6Q-A), Normal-ver.



Date code seven digits
Manufacturing management code
Type No. M30281MAHP
Chip version and product code
XXX: ROM No.
A : Chip version and product code(1)
The first edition is shown to be blank and continues with A, B and C.
U5 : Product code. (**Table 1.6**)

NOTES:
1. The following functinos are not available in the first version and version A products.
-Delay trigger mode 0 of A/D conversion
-Delay trigger mode 1 of A/D conversion

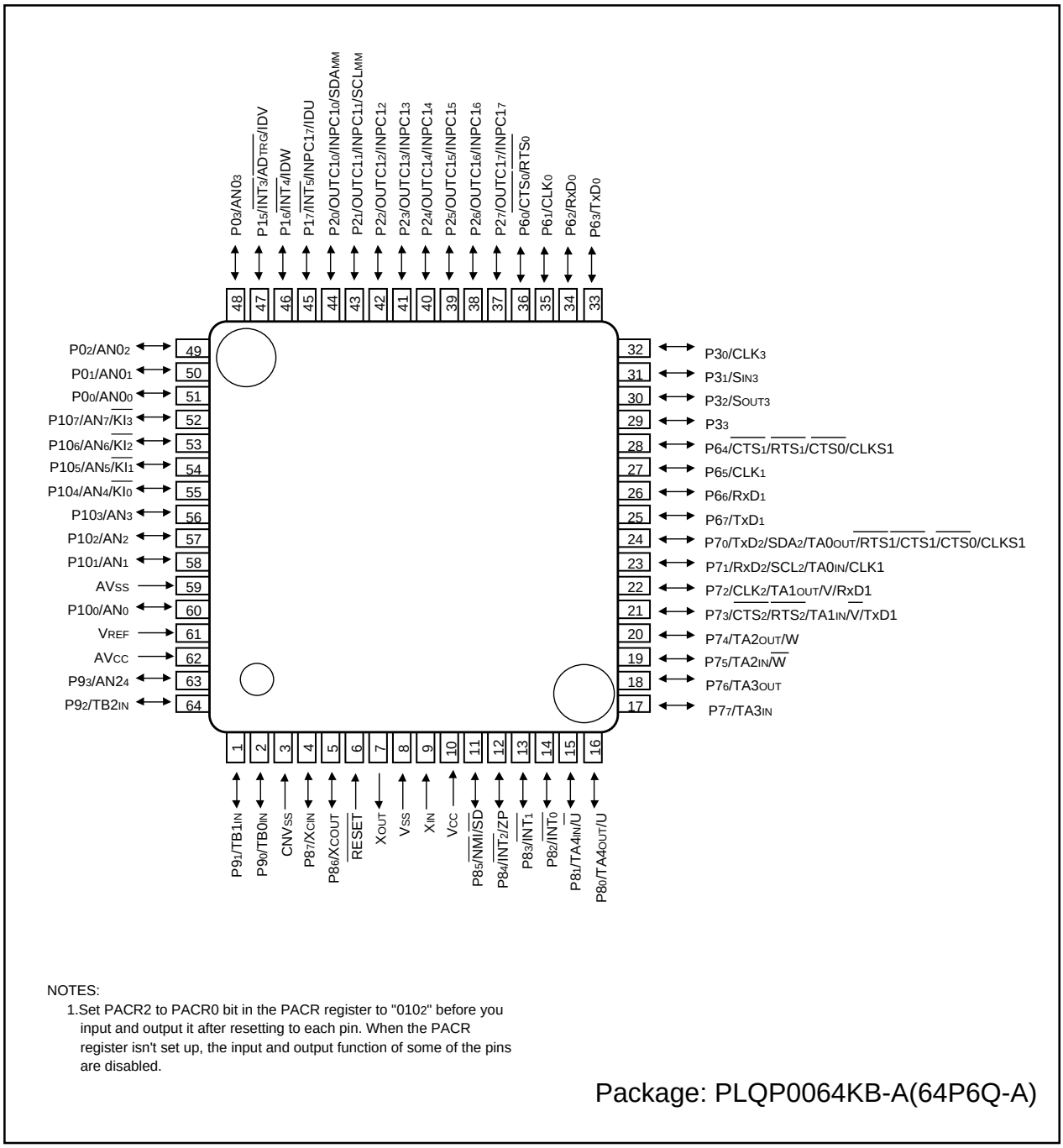
Figure 1.4 Marking Diagram-M16C/28 Normal-ver.

Table 1.9 Pin Characteristics for 80-Pin Package

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	Timer S Pin	UART Pin	Multi-master I^2C bus Pin	Analog Pin
1		$P9_5$				CLK_4		$AN2_5$
2		$P9_3$						$AN2_4$
3		$P9_2$		TB_{2IN}				
4		$P9_1$		TB_{1IN}				
5		$P9_0$		TB_{0IN}				
6	CNVss							
7	X_{CIN}	$P8_7$						
8	X_{COUT}	$P8_6$						
9	$\overline{RESET}$							
10	X_{OUT}							
11	Vss							
12	X_{IN}							
13	Vcc							
14		$P8_5$	$\overline{NMI}$	$\overline{SD}$				
15		$P8_4$	$\overline{INT_2}$	ZP				
16		$P8_3$	$\overline{INT_1}$					
17		$P8_2$	$\overline{INT_0}$					
18		$P8_1$		TA_{4IN} / $\overline{U}$				
19		$P8_0$		TA_{4OUT} / U				
20		$P7_7$		TA_{3IN}				
21		$P7_6$		TA_{3OUT}				
22		$P7_5$		TA_{2IN} / $\overline{W}$				
23		$P7_4$		TA_{2OUT} / W				
24		$P7_3$		TA_{1IN} / $\overline{V}$		$\overline{CTS_2}$ / $\overline{RTS_2}$ / TxD_1		
25		$P7_2$		TA_{1OUT} / V		CLK_2 / RxD_1		
26		$P7_1$		TA_{0IN}		RxD_2 / SCL_2 / CLK_1		
27		$P7_0$		TA_{0OUT}		TxD_2 / SDA_2 / $\overline{RTS_1}$ / $\overline{CTS_1}$ / $\overline{CTS_0}$ / $CLKS_1$		
28		$P6_7$				TxD_1		
29		$P6_6$				RxD_1		
30		$P6_5$				CLK_1		
31		$P6_4$				RTS_1 / $\overline{CTS_1}$/ $\overline{CTS_0}$ / $CLKS_1$		
32		$P3_7$						
33		$P3_6$						
34		$P3_5$						
35		$P3_4$						
36		$P3_3$						
37		$P3_2$				$SOUT_3$		
38		$P3_1$				SIN_3		
39		$P3_0$				CLK_3		
40		$P6_3$				TxD_0		

Table 1.9 Pin Characteristics for 80-Pin Package (Continued)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	Timer S Pin	UART Pin	Multi-master I^2C bus Pin	Analog Pin
41		$P6_2$				RxD_0		
42		$P6_1$				CLK_0		
43		$P6_0$				$\overline{RTS_0}$ / $\overline{CTS_0}$		
44		$P2_7$			$OUTC1_7$ / $INPC1_7$			
45		$P2_6$			$OUTC1_6$ / $INPC1_6$			
46		$P2_5$			$OUTC1_5$ / $INPC1_5$			
47		$P2_4$			$OUTC1_4$ / $INPC1_4$			
48		$P2_3$			$OUTC1_3$ / $INPC1_3$			
49		$P2_2$			$OUTC1_2$ / $INPC1_2$			
50		$P2_1$			$OUTC1_1$ / $INPC1_1$		SCL_{MM}	
51		$P2_0$			$OUTC1_0$ / $INPC1_0$		SDA_{MM}	
52		$P1_7$	$\overline{INT_5}$	IDU	$INPC1_7$			
53		$P1_6$	$\overline{INT_4}$	IDW				
54		$P1_5$	$\overline{INT_3}$	IDV				$\overline{ADTRG}$
55		$P1_4$						
56		$P1_3$						$AN2_3$
57		$P1_2$						$AN2_2$
58		$P1_1$						$AN2_1$
59		$P1_0$						$AN2_0$
60		$P0_7$						$AN0_7$
61		$P0_6$						$AN0_6$
62		$P0_5$						$AN0_5$
63		$P0_4$						$AN0_4$
64		$P0_3$						$AN0_3$
65		$P0_2$						$AN0_2$
66		$P0_1$						$AN0_1$
67		$P0_0$						$AN0_0$
68		$P10_7$	$\overline{KI_3}$					AN_7
69		$P10_6$	$\overline{KI_2}$					AN_6
70		$P10_5$	$\overline{KI_1}$					AN_5
71		$P10_4$	$\overline{KI_0}$					AN_4
72		$P10_3$						AN_3
73		$P10_2$						AN_2
74		$P10_1$						AN_1
75	AVss							
76		$P10_0$						AN_0
77	V_{REF}							
78	AVcc							
79		$P9_7$				SIN_4		$AN2_7$
80		$P9_6$				$SOUT_4$		$AN2_6$



NOTES:
1. Set PACR2 to PACR0 bit in the PACR register to "010₂" before you input and output it after resetting to each pin. When the PACR register isn't set up, the input and output function of some of the pins are disabled.

Package: PLQP0064KB-A(64P6Q-A)

Figure 1.6 Pin Assignment (Top View) of 64-Pin Package

Table 1.10 Pin Characteristics for 64-Pin Package

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	Timer S Pin	UART Pin	Mult-master I^2C bus Pin	Analog Pin
1		$P9_1$		TA_{1IN}				
2		$P9_0$		TB_{0IN}				
3	CNVss							
4	X_{CIN}	$P8_7$						
5	X_{COUT}	$P8_6$						
6	$\overline{RESET}$							
7	X_{OUT}							
8	Vss							
9	X_{IN}							
10	Vcc							
11		$P8_5$	$\overline{NMI}$	$\overline{SD}$				
12		$P8_4$	$\overline{INT_2}$	ZP				
13		$P8_3$	$\overline{INT_1}$					
14		$P8_2$	$\overline{INT_0}$					
15		$P8_1$		TA_{4IN} / $\overline{U}$				
16		$P8_0$		TA_{4OUT} / U				
17		$P7_7$		TA_{3IN}				
18		$P7_6$		TA_{3OUT}				
19		$P7_5$		TA_{2IN} / $\overline{W}$				
20		$P7_4$		TA_{2OUT} / W				
21		$P7_3$		TA_{1IN} / $\overline{V}$		$\overline{CTS_2}$ / $\overline{RTS_2}$ / TxD_1		
22		$P7_2$		TA_{1OUT} / V		CLK_2 / RxD_1		
23		$P7_1$		TA_{0IN}		RxD_2 / SCL_2 / CLK_1		
24		$P7_0$		TA_{0OUT}		TxD_2 / SDA_2 / $\overline{RTS_1}$ / $\overline{CTS_1}$ / $\overline{CTS_0}$ / $CLKS_1$		
25		$P6_7$				TxD_1		
26		$P6_6$				RxD_1		
27		$P6_5$				CLK_1		
28		$P6_4$				$\overline{RTS_1}$ / $\overline{CTS_1}$/ $\overline{CTS_0}$ / $CLKS_1$		
29		$P3_3$						
30		$P3_2$				$SOUT_3$		
31		$P3_1$				SIN_3		
32		$P3_0$				CLK_3		
33		$P6_3$				TxD_0		
34		$P6_2$				RxD_0		
35		$P6_1$				CLK_0		
36		$P6_0$				$\overline{RTS_0}$ / $\overline{CTS_0}$		
37		$P2_7$			$OUTC1_7$ / $INPC1_7$			
38		$P2_6$			$OUTC1_6$ / $INPC1_6$			
39		$P2_5$			$OUTC1_5$ / $INPC1_5$			
40		$P2_4$			$OUTC1_4$ / $INPC1_4$			

Table 10 Pin Characteristics for 64-Pin Package (Continued)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	Timer S Pin	UART Pin	Multi-master I^2C bus Pin	Analog Pin
41		$P2_3$			$OUTC1_3$ / $INPC1_3$			
42		$P2_2$			$OUTC1_2$ / $INPC1_2$			
43		$P2_1$			$OUTC1_1$ / $INPC1_1$		SCL_{MM}	
44		$P2_0$			$OUTC1_0$ / $INPC1_0$		SDA_{MM}	
45		$P1_7$	$\overline{INT}_5$	IDU	$INPC1_7$			
46		$P1_6$	$\overline{INT}_4$	IDW				
47		$P1_5$	$\overline{INT}_3$	IDV				$\overline{AD_{TRG}}$
48		$P0_3$						$AN0_3$
49		$P0_2$						$AN0_2$
50		$P0_1$						$AN0_1$
51		$P0_0$						$AN0_0$
52		$P10_7$	$\overline{KI}_3$					AN_7
53		$P10_6$	$\overline{KI}_2$					AN_6
54		$P10_5$	$\overline{KI}_1$					AN_5
55		$P10_4$	$\overline{KI}_0$					AN_4
56		$P10_3$						AN_3
57		$P10_2$						AN_2
58		$P10_1$						AN_1
59	AVss							
60		$P10_0$						AN_0
61	V_{REF}							
62	AVcc							
63		$P9_3$						$AN2_4$
64		$P9_2$		TB_{2IN}				

1.6 Pin Description

Table 1.10 Pin Description (64-Pin, 80-Pin and 85-Pin Packages)

Classification	Symbol	I/O Type	Function
Power Supply	VCC, VSS	I	Apply 2.7 to 5.5V to the Vcc pin. Apply 0V to the Vss pin.
Analog Power Supply	AVCC AVSS	I	Supplies power to the A/D converter. Connect the AVCC pin to VCC and the AVSS pin to VSS.
Reset Input	$\overline{\text{RESET}}$	I	The MCU is in a reset state when "L" is applied to the $\overline{\text{RESET}}$ pin
CNVSS	CNVSS	I	Connect the CNVSS pin to VSS.
Main Clock Input	XIN	I	I/O pins for the main clock oscillation circuit. Connect a ceramic resonator or crystal oscillator between XIN and XOUT. To apply external clock, apply it to XIN and leave XOUT open. If XIN is not used (for external oscillator or external clock) connect XIN pin to VCC and leave XOUT open.
Main Clock Output	XOUT	O	
Sub Clock Input	XCIN	I	I/O pins for the sub clock oscillation circuit. Connect a crystal oscillator between XCIN and XCOUT.
Sub Clock Output	XCOUT	O	
$\overline{\text{INT}}$ Interrupt Input	$\overline{\text{INT0}}$ to $\overline{\text{INT5}}$	I	Input pins for the $\overline{\text{INT}}$ interrupt. $\overline{\text{INT2}}$ can be used for Timer A Z-phase function.
$\overline{\text{NMI}}$ Interrupt Input	$\overline{\text{NMI}}$	I	Input pin for the $\overline{\text{NMI}}$ interrupt. $\overline{\text{NMI}}$ cannot be used as I/O port while the three-phase motor control is enabled. Apply a stable "H" to $\overline{\text{NMI}}$ after setting it's direction register to "0" when the three-phase motor control is enabled.
Key Input Interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	Input pins for the key input interrupt
Timer A	TA0OUT to TA4OUT	I/O	I/O pins for the timer A0 to A4
	TA0IN to TA4IN	I	Input pins for the timer A0 to A4
	ZP	I	Input pin for Z-phase
Timer B	TB0IN to TB2IN	I	Input pins for the timer B0 to B2
Three-phase Motor Control Timer Output	U, $\overline{\text{U}}$, V, $\overline{\text{V}}$, W, $\overline{\text{W}}$	O	Output pins for the three-phase motor control timer
	IDU, IDW, IDV, $\overline{\text{SD}}$	I/O	Input and output pins for the three-phase motor control timer
Serial I/O	$\overline{\text{CTS0}}$ to $\overline{\text{CTS2}}$	I	Input pins for data transmission control
	$\overline{\text{RTS0}}$ to $\overline{\text{RTS2}}$	O	Output pins for data reception control
	CLK0 to CLK3	I/O	Inputs and outputs the transfer clock
	RxD0 to RxD2	I	Inputs serial data
	TxD0 to TxD2	O	Outputs serial data
	CLKS1	O	Output pin for transfer clock
I^2C Mode	SDA2	I/O	Inputs and outputs serial data
	SCL2		Inputs and outputs the transfer clock
Multi-master I^2C bus	SDAMM	I/O	Inputs and outputs serial data
	SCLMM		Inputs and outputs the transfer clock
Reference Voltage Input	VREF	I	Applies reference voltage to the A/D converter
A/D Converter	AN0 to AN7 AN00 to AN03 AN24	I	Analog input pins for the A/D converter
	$\overline{\text{ADTRG}}$		Input pin for an external A/D trigger

I : Input O : Output I/O : Input and output

Table 1.10 Pin Description (80-Pin and 85-Pin Packages only) (Continued)

Classification	Symbol	I/O Type	Function
Serial I/O	CLK4	I/O	Inputs and outputs the transfer clock
	SIN4	I	Inputs serial data
	SOUT4	O	Outputs serial data
A/D Converter	AN04 to AN07 AN20 to AN23 AN25 to AN27	I	Analog input pins for the A/D converter
I/O Ports	P04 to P07 P10 to P14 P34 to P37	I/O	I/O ports for CMOS. Each port can be programmed for input or output under the control of the direction register. An input port can be set, by program, for a pull-up resistor available or for no pull-up resister available in 4-bit units
	P95 to P97	I/O	I/O ports having equivalent functions to P0

I : Input O : Output I/O : Input and output

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers. The register bank is comprised of 7 registers (R0, R1, R2, R3, A0, A1 and FB) out of 13 CPU registers. Two sets of register banks are provided.

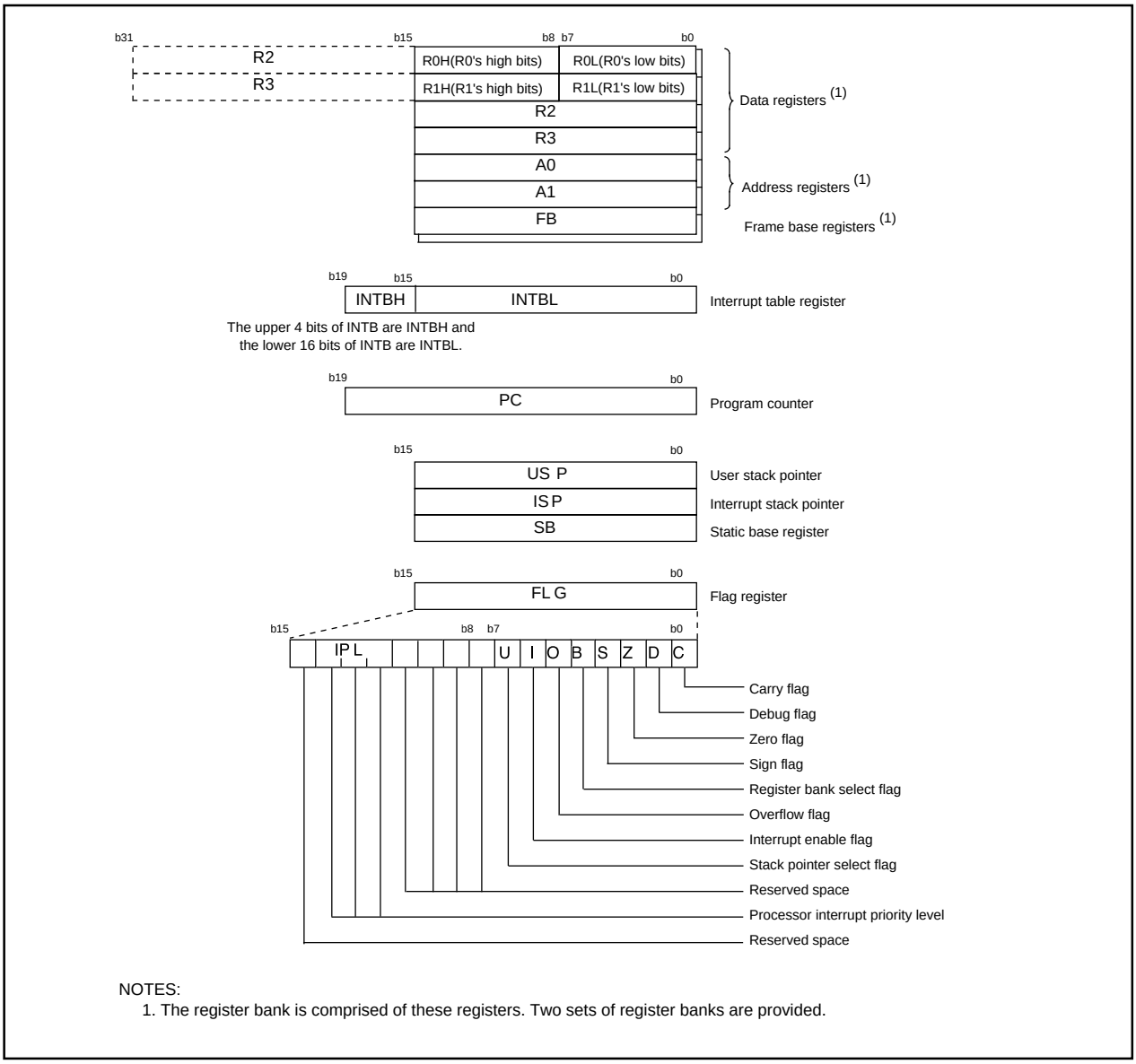


Figure 2.1 Central Processing Unit Register

2.1 Data Registers (R0, R1, R2 and R3)

The R0, R1, R2 and R3 registers are 16 bit registers for transfer and arithmetic/logic operations.

The R0 and R1 registers can be split into high-order bits(R0H, R1H) and low-order bits (R0L, R1L) to be used seperately as 8-bit data registers. Conversely, R2 and R0 can be combined with R2 to be used as a 32-bit data register (R2R0). The same applies to R1 and R2.

2.2 Address Registers (A0 and A1)

The register A0 consists of 16 bits, and is used for address register indirect addressing and address register relative addressing. They also are used for transfers and arithmetic/logic operations. A1 is the same as A0. In some instructions, registers A1 and A0 can be combined for use as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is configured with 16 bits, and is used for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is configured with 20 bits, indicating the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC is configured with 20 bits, indicating the address of an instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

Stack pointer (SP) comes in two types: USP and ISP, each configured with 16 bits.

Your desired type of stack pointer (USP or ISP) can be selected by the U flag of FLG.

2.7 Static Base Register (SB)

SB is configured with 16 bits, and is used for SB relative addressing.

2.8 Flag Register (FLG)

FLG consists of 11 bits, indicating the CPU status.

2.8.1 Carry Flag (C Flag)

This flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic/logic unit.

2.8.2 Debug Flag (D Flag)

The D flag is used exclusively for debugging purpose. During normal use, it must be set to 0.

2.8.3 Zero Flag (Z Flag)

This flag is set to 1 when an arithmetic operation resulted in 0; otherwise, it is 0.

2.8.4 Sign Flag (S Flag)

This flag is set to 1 when an arithmetic operation resulted in a negative value; otherwise, it is 0.

2.8.5 Register Bank Select Flag (B Flag)

Register bank 0 is selected when this flag is 0 ; register bank 1 is selected when this flag is 1.

2.8.6 Overflow Flag (O Flag)

This flag is set to 1 when the operation resulted in an overflow; otherwise, it is 0.

2.8.7 Interrupt Enable Flag (I Flag)

This flag enables a maskable interrupt.

Maskable interrupts are disabled when the I flag is 0, and are enabled when the I flag is 1. The I flag is cleared to 0 when the interrupt request is accepted.

2.8.8 Stack Pointer Select Flag (U Flag)

ISP is selected when the U flag is 0; USP is selected when the U flag is 1.

The U flag is cleared to 0 when a hardware interrupt request is accepted or an INT instruction for software interrupt Nos. 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is configured with three bits, for specification of up to eight processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has priority greater than IPL, the interrupt is enabled.

2.8.10 Reserved Area

When write to this bit, write 0. When read, its content is indeterminate.

Table 4.2 SFR Information(2)(1)

Address	Register	Symbol	After Reset
0040₁₆			
0041₁₆			
0042₁₆			
0043₁₆			
0044₁₆	INT3 interrupt control register	INT3IC	XX00X000₂
0045₁₆	IC/OC 0 interrupt control register	ICOC0IC	XXXXX000₂
0046₁₆	IC/OC 1 interrupt control register, I²C bus interface interrupt control register	ICOC1IC, IICIC	XXXXX000₂
0047₁₆	IC/OC base timer interrupt control register, SCLSDA interrupt control register	BTIC, SCLDAIC	XXXXX000₂
0048₁₆	SI/O4 interrupt control register, INT5 interrupt control register	S4IC, INT5IC	XX00X000₂
0049₁₆	SI/O3 interrupt control register, INT4 interrupt control register	S3IC, INT4IC	XX00X000₂
004A₁₆	UART2 Bus collision detection interrupt control register	BCNIC	XXXXX000₂
004B₁₆	DMA0 interrupt control register	DM0IC	XXXXX000₂
004C₁₆	DMA1 interrupt control register	DM1IC	XXXXX000₂
004D₁₆	Key input interrupt control register	KUPIC	XXXXX000₂
004E₁₆	A/D conversion interrupt control register	ADIC	XXXXX000₂
004F₁₆	UART2 transmit interrupt control register	S2TIC	XXXXX000₂
0050₁₆	UART2 receive interrupt control register	S2RIC	XXXXX000₂
0051₁₆	UART0 transmit interrupt control register	S0TIC	XXXXX000₂
0052₁₆	UART0 receive interrupt control register	S0RIC	XXXXX000₂
0053₁₆	UART1 transmit interrupt control register	S1TIC	XXXXX000₂
0054₁₆	UART1 receive interrupt control register	S1RIC	XXXXX000₂
0055₁₆	Timer A0 interrupt control register	TA0IC	XXXXX000₂
0056₁₆	Timer A1 interrupt control register	TA1IC	XXXXX000₂
0057₁₆	Timer A2 interrupt control register	TA2IC	XXXXX000₂
0058₁₆	Timer A3 interrupt control register	TA3IC	XXXXX000₂
0059₁₆	Timer A4 interrupt control register	TA4IC	XXXXX000₂
005A₁₆	Timer B0 interrupt control register	TB0IC	XXXXX000₂
005B₁₆	Timer B1 interrupt control register	TB1IC	XXXXX000₂
005C₁₆	Timer B2 interrupt control register	TB2IC	XXXXX000₂
005D₁₆	INT0 interrupt control register	INT0IC	XX00X000₂
005E₁₆	INT1 interrupt control register	INT1IC	XX00X000₂
005F₁₆	INT2 interrupt control register	INT2IC	XX00X000₂
0060₁₆			
0061₁₆			
0062₁₆			
0063₁₆			
0064₁₆			
0065₁₆			
0066₁₆			
0067₁₆			
0068₁₆			
0069₁₆			
006A₁₆			
006B₁₆			
006C₁₆			
006D₁₆			
006E₁₆			
006F₁₆			
0070₁₆			
0071₁₆			
0072₁₆			
0073₁₆			
0074₁₆			
0075₁₆			
0076₁₆			
0077₁₆			
0078₁₆			
0079₁₆			
007A₁₆			
007B₁₆			
007C₁₆			
007D₁₆			
007E₁₆			
007F₁₆			

Note 1: The blank spaces are reserved. No access is allowed.

X : Undefined

Table 4.3 SFR Information(3)(1)

Address	Register	Symbol	After Reset
≈			≈
01B016			
01B116			
01B216			
01B316	Flash memory control register 4 (2)	FMR4	010000002
01B416			
01B516	Flash memory control register 1 (2)	FMR1	000XXX0X2
01B616			
01B716	Flash memory control register 0 (2)	FMR0	000000012
01B816			
01B916			
≈			≈
021016	Low-power Consumption Control 0	LPCC0	X00000012
021116			
021216			
021316			
021416			
021516			
021616			
021716			
021816			
021916			
≈			≈
025016			
025116			
025216			
025316			
025416			
025516			
025616			
025716			
025816			
025916			
025A16			
025B16			
025C16	On-chip oscillator control register	ROCR	X00001012
025D16	Pin assignment control register	PACR	0016
025E16	Peripheral clock select register	PCLKR	000000112
025F16	Low-power Consumption Control 1	LPCC1	0016
≈			≈
02E016	I^2C0 data shift register	S00	XX16
02E116			
02E216	I^2C0 address register	S0D0	0016
02E316	I^2C0 control register 0	S1D0	0016
02E416	I^2C0 clock control register	S20	0016
02E516	I^2C0 start/stop condition control register	S2D0	000110102
02E616	I^2C0 control register 1	S3D0	001100002
02E716	I^2C0 control register 2	S4D0	0016
02E816	I^2C0 status register	S10	0001000X2
02E916			
02EA16			
≈			≈
02FE16			
02FF16			

Note 1:The blank spaces are reserved. No access is allowed.
Note 2:This register is included in the flash memory version.

X : Undefined

Table 4.5 SFR Information(5)(1)

Address	Register	Symbol	After Reset
034016			
034116			
034216	Timer A1-1 register	TA11	XX16
034316			XX16
034416	Timer A2-1 register	TA21	XX16
034516			XX16
034616	Timer A4-1 register	TA41	XX16
034716			XX16
034816	Three-phase PWM control register 0	INVC0	0016
034916	Three-phase PWM control register 1	INVC1	0016
034A16	Three-phase output buffer register 0	IDB0	001111112
034B16	Three-phase output buffer register 1	IDB1	001111112
034C16	Dead time timer	DTT	XX16
034D16	Timer B2 interrupt occurrence frequency set counter	ICTB2	XX16
034E16	Position-data-retain function control register	PDRF	XXXX00002
034F16			
035016			
035116			
035216			
035316			
035416			
035516			
035616			
035716			
035816			
035916			
035A16			
035B16			
035C16			
035D16			
035E16	Interrupt request cause select register 2	IFSR2A	00XXXXX02(2)
035F16	Interrupt request cause select register	IFSR	0016
036016	SI/O3 transmit/receive register	S3TRR	XX16
036116			
036216	SI/O3 control register	S3C	010000002
036316	SI/O3 bit rate generator	S3BRG	XX16
036416	SI/O4 transmit/receive register	S4TRR	XX16
036516			
036616	SI/O4 control register	S4C	010000002
036716	SI/O4 bit rate generator	S4BRG	XX16
036816			
036916			
036A16			
036B16			
036C16			
036D16			
036E16			
036F16			
037016			
037116			
037216			
037316			
037416	UART2 special mode register 4	U2SMR4	0016
037516	UART2 special mode register 3	U2SMR3	000X0X0X2
037616	UART2 special mode register 2	U2SMR2	X0000000 2
037716	UART2 special mode register	U2SMR	X0000000 2
037816	UART2 transmit/receive mode register	U2MR	0016
037916	UART2 bit rate generator	U2BRG	XX16
037A16	UART2 transmit buffer register	U2TB	XX16
037B16			XX16
037C16	UART2 transmit/receive control register 0	U2C0	000010002
037D16	UART2 transmit/receive control register 1	U2C1	000000102
037E16	UART2 receive buffer register	U2RB	XX16
037F16			XX16

Note 1: The blank spaces are reserved. No access is allowed.
Note 2: Write 1 to bit 0 after reset.

X : Undefined

Table 4.6 SFR Information(6)(1)

Address	Register	Symbol	After Reset
038016	Count start flag	TABSR	0016
038116	Clock prescaler reset flag	CPSRF	0XXXXXXX2
038216	One-shot start flag	ONSF	0016
038316	Trigger select register	TRGSR	0016
038416	Up-down flag	UDF	0016
038516			
038616	Timer A0 register	TA0	XX16
038716			XX16
038816	Timer A1 register	TA1	XX16
038916			XX16
038A16	Timer A2 register	TA2	XX16
038B16			XX16
038C16	Timer A3 register	TA3	XX16
038D16			XX16
038E16	Timer A4 register	TA4	XX16
038F16			XX16
039016	Timer B0 register	TB0	XX16
039116			XX16
039216	Timer B1 register	TB1	XX16
039316			XX16
039416	Timer B2 register	TB2	XX16
039516			XX16
039616	Timer A0 mode register	TA0MR	0016
039716	Timer A1 mode register	TA1MR	0016
039816	Timer A2 mode register	TA2MR	0016
039916	Timer A3 mode register	TA3MR	0016
039A16	Timer A4 mode register	TA4MR	0016
039B16	Timer B0 mode register	TB0MR	00XX00002
039C16	Timer B1 mode register	TB1MR	00XX00002
039D16	Timer B2 mode register	TB2MR	00XX00002
039E16	Timer B2 special mode register	TB2SC	X00000002
039F16			
03A016	UART0 transmit/receive mode register	U0MR	0016
03A116	UART0 bit rate generator	U0BRG	XX16
03A216	UART0 transmit buffer register	U0TB	XX16
03A316			XX16
03A416	UART0 transmit/receive control register 0	U0C0	000010002
03A516	UART0 transmit/receive control register 1	U0C1	000000102
03A616	UART0 receive buffer register	U0RB	XX16
03A716			XX16
03A816	UART1 transmit/receive mode register	U1MR	0016
03A916	UART1 bit rate generator	U1BRG	XX16
03AA16	UART1 transmit buffer register	U1TB	XX16
03AB16			XX16
03AC16	UART1 transmit/receive control register 0	U1C0	000010002
03AD16	UART1 transmit/receive control register 1	U1C1	000000102
03AE16	UART1 receive buffer register	U1RB	XX16
03AF16			XX16
03B016	UART transmit/receive control register 2	UCON	X00000002
03B116			
03B216			
03B316			
03B416			
03B516			
03B616			
03B716			
03B816	DMA0 request cause select register	DM0SL	0016
03B916			
03BA16	DMA1 request cause select register	DM1SL	0016
03BB16			
03BC16			
03BD16			
03BE16			
03BF16			

Note 1:The blank spaces are reserved. No access is allowed.

X : Undefined

Table 4.7 SFR Information(7)(1)

Address	Register	Symbol	After Reset
03C0₁₆	A/D register 0	AD0	XX₁₆
03C1₁₆			XX₁₆
03C2₁₆	A/D register 1	AD1	XX₁₆
03C3₁₆			XX₁₆
03C4₁₆	A/D register 2	AD2	XX₁₆
03C5₁₆			XX₁₆
03C6₁₆	A/D register 3	AD3	XX₁₆
03C7₁₆			XX₁₆
03C8₁₆	A/D register 4	AD4	XX₁₆
03C9₁₆			XX₁₆
03CA₁₆	A/D register 5	AD5	XX₁₆
03CB₁₆			XX₁₆
03CC₁₆	A/D register 6	AD6	XX₁₆
03CD₁₆			XX₁₆
03CE₁₆	A/D register 7	AD7	XX₁₆
03CF₁₆			XX₁₆
03D0₁₆			
03D1₁₆			
03D2₁₆	A/D trigger control register	ADTRGCON	00₁₆
03D3₁₆	A/D convert status register 0	ADSTAT0	00000X00₂
03D4₁₆	A/D control register 2	ADCON2	00₁₆
03D5₁₆			
03D6₁₆	A/D control register 0	ADCON0	00000XXX₂
03D7₁₆	A/D control register 1	ADCON1	00₁₆
03D8₁₆			
03D9₁₆			
03DA₁₆			
03DB₁₆			
03DC₁₆			
03DD₁₆			
03DE₁₆			
03DF₁₆			
03E0₁₆	Port P0 register	P0	XX₁₆
03E1₁₆	Port P1 register	P1	XX₁₆
03E2₁₆	Port P0 direction register	PD0	00₁₆
03E3₁₆	Port P1 direction register	PD1	00₁₆
03E4₁₆	Port P2 register	P2	XX₁₆
03E5₁₆	Port P3 register	P3	XX₁₆
03E6₁₆	Port P2 direction register	PD2	00₁₆
03E7₁₆	Port P3 direction register	PD3	00₁₆
03E8₁₆			
03E9₁₆			
03EA₁₆			
03EB₁₆			
03EC₁₆	Port P6 register	P6	XX₁₆
03ED₁₆	Port P7 register	P7	XX₁₆
03EE₁₆	Port P6 direction register	PD6	00₁₆
03EF₁₆	Port P7 direction register	PD7	00₁₆
03F0₁₆	Port P8 register	P8	XX₁₆
03F1₁₆	Port P9 register	P9	XX₁₆
03F2₁₆	Port P8 direction register	PD8	00₁₆
03F3₁₆	Port P9 direction register	PD9	000X0000₂
03F4₁₆	Port P10 register	P10	XX₁₆
03F5₁₆			
03F6₁₆	Port P10 direction register	PD10	00₁₆
03F7₁₆			
03F8₁₆			
03F9₁₆			
03FA₁₆			
03FB₁₆			
03FC₁₆	Pull-up control register 0	PUR0	00₁₆
03FD₁₆	Pull-up control register 1	PUR1	00₁₆
03FE₁₆	Pull-up control register 2	PUR2	00₁₆
03FF₁₆	Port control register	PCR	00₁₆

Note 1:The blank spaces are reserved. No access is allowed.

X : Undefined

REVISION HISTORY	M16C/28 Group (M16C/28, M16C/28B) Shortsheet

Rev.	Date	Description	
		Page	Summary
0.50	09/15/06	-	First edition