



Welcome to [E-XFL.COM](#)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	M16C/60
Core Size	16-Bit
Speed	20MHz
Connectivity	I ² C, IEBus, SIO, UART/USART
Peripherals	DMA, POR, PWM, Voltage Detect, WDT
Number of I/O	55
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 13x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30281f6hp-u7b

1. Overview

The M16C/28 Group (M16C/28 and M16C/28B) MCU are single-chip control MCU, fabricated using high-performance silicon gate CMOS technology with the M16C/60 series CPU core. The M16C/28 Group (M16C/28 and M16C/28B) are housed in 64-pin and 80-pin plastic molded LQFP packages and also in 85-pin plastic molded TFLGA (Thin Fine Pitch Land Grid Array) package. With a 1-Mbyte address space, this MCU combines advanced instruction manipulation capabilities to process complex instructions by less bytes and execute instructions at higher speed. It includes a multiplier and DMAC adequate for office automation, communication devices and other high-speed processing applications.

The M16C/28 has Normal-ver., T-ver., and V-ver.. The M16C/28B has Normal-ver. only.

This hardware manual describes the Normal-ver. only. Please contact Renesas Technology Corp. for T-ver./V-ver. information.

1.1 Applications

Audio, cameras, office equipment, communication equipment, portable equipment, home appliances (inverter solution), motor control, industrial equipment, etc.

1.2 Performance Overview

Table 1.1 and **1.2** outline performance overview of the M16C/28 Group (M16C/28, M16C/28B).

Table 1.1 M16C/28 Group (M16C/28, M16C/28B) Performance (80/85-Pin Package)

	Item	Performance
CPU	Number of basic instructions	91 instructions
	Minimum instruction execution time	41.7 ns (f(BCLK) = 24 MHz, Vcc = 4.2 V to 5.5 V) (M16C/28B) 50 ns (f(BCLK) = 20 MHz, Vcc = 3.0 V to 5.5 V) (M16C/28, M16C/28B) 100 ns (f(BCLK) = 10 MHz, Vcc = 2.7 V to 5.5 V) (M16C/28, M16C/28B)
	Operation mode	Single chip mode
	Address space	1M bytes
	Memory capacity	See Table 1.3
Peripheral Function	I/O port	Input/Output : 71 lines
	Multifunction timer	TimerA:16 bits x 5 channels, TimerB:16 bits x 3 channels Three-phase Motor Control Timer TimerS (Input Capture/Output Compare) : 16bit base timer x 1 channel (Input/Output x 8 channels)
	Serial I/O	2 channels (UART0, UART1) UART, clock synchronous 1 channel (UART2) UART, clock synchronous, I ² C bus ⁽¹⁾ , or IEBus ⁽²⁾ 2 channels (SI/O3, SI/O4) Clock synchronous 1 channel (Multi-Master I ² C bus ⁽¹⁾)
	A/D converter	10 bits x 24 channels
	DMAC	2 channels
	Watchdog timer	15 bits x 1 (with prescaler)
	Interrupt	25 internal and 8 external sources, 4 software sources, 7 levels
	Clock generation circuit	4 circuits • Main clock (*) • Sub-clock (*) • On-chip oscillator • PLL frequency synthesizer (*) Equipped with a built-in feedback resistor
	Oscillation Stop Detect Function	Main clock oscillation stop, re-oscillation detect function
	Voltage detection circuit	Available
Electrical Characteristics	Power supply voltage	Vcc = 4.2 V to 5.5 V (f(BCLK) = 24 MHz) (M16C/28B) Vcc = 3.0 V to 5.5 V (f(BCLK) = 20 MHz) (M16C/28, M16C/28B) Vcc = 2.7 V to 5.5 V (f(BCLK) = 10 MHz) (M16C/28, M16C/28B)
	Power consumption	16 mA (Vcc = 5V, f(BCLK) = 20 MHz) 25 μ A (f(XCIN) = 32 KHz on RAM) 3.0 μ A (Vcc = 3V, f(XCIN) = 32 KHz, in wait mode) 0.7 μ A (Vcc = 3V, in stop mode)
Flash Memory	Program/erase supply voltage	2.7 V to 5.5 V
	Program and erase endurance	100 times (all space) or 1,000 times (Blocks 0 to 5) /10,000 times (Block A, Block B ⁽³⁾)
Operating Ambient Temperature		-20 to 85°C/-40 to 85°C ⁽³⁾
Package		80-pin plastic mold LQFP, 85-pin plastic mold TFLGA

NOTES:

1. I²C bus is a trademark of Koninklijke Philips Electronics N. V.
2. IEBus is a trademark of NEC Electronics Corporation.
3. Refer to **Table 1.5** to **1.7** for number of program/erase.
4. Use PLL frequency synthesizer to use M16C/28B at f(BCLK) = 24 MHz.

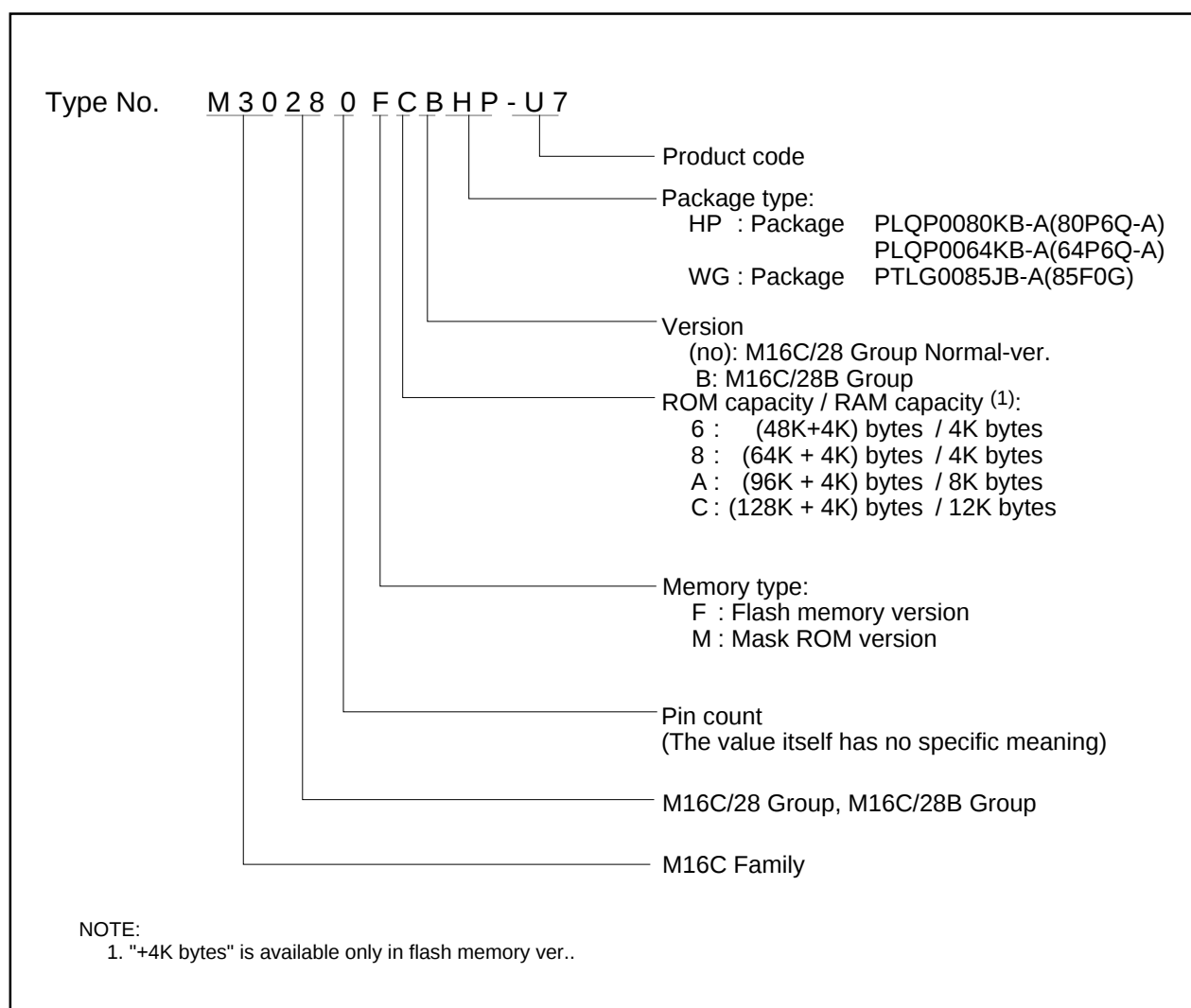


Figure 1.3 Product Numbering System

Table 1.5 Product Code (Flash Memory-ver.) - M16C/28 Normal-ver., 64-Pin⁽¹⁾/80-Pin⁽¹⁾/85-Pin Package

Product Code	Package	Internal ROM (User Program Space)		Internal ROM (Data Space)		Operating Ambient Temperature
		Program and Erase Endurance	Temperature Range	Program and Erase Endurance	Temperature Range	
U3	Lead free	100	0 to 60°C	100	0 to 60°C	-40 to 85°C
U5					-20 to 85°C	
U7		1,000		10,000	-40 to 85°C	-40 to 85°C
U9					-20 to 85°C	-20 to 85°C

NOTE:

1. The lead contained products, D3, D5, D7 and D9, are put together with U3, U5, U7 and U9 respectively. Lead-free (Sn-Ag-Cu plating) products can be mounted by both conventional Sn-Pb paste and Lead-free paste.

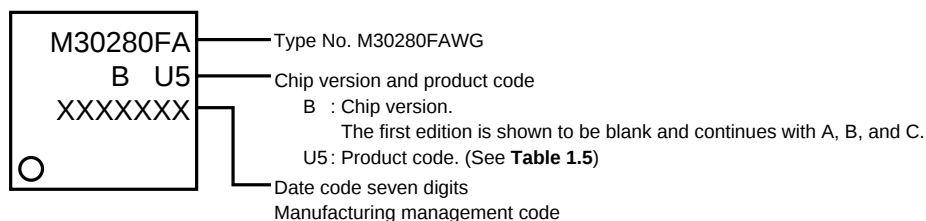
Table 1.6 Product Code (Flash Memory-ver.) - M16C/28B Normal-ver., 64-Pin/85-Pin Package

Product Code	Package	Internal ROM (User Program Space)		Internal ROM (Data Space)		Operating Ambient Temperature
		Program and Erase Endurance	Temperature Range	Program and Erase Endurance	Temperature Range	
U7	Lead-free	1,000	0 to 60°C	10,000	-40 to 85°C	-40 to 85°C

Table 1.7 Product Code (Mask ROM ver.) - M16C/28B Normal-ver., 64-Pin/80-Pin/85-Pin Package

Product Code	Package	Operating Ambient Temperature
U3	Lead-free	-40 to 85°C
U5		-20 to 85°C

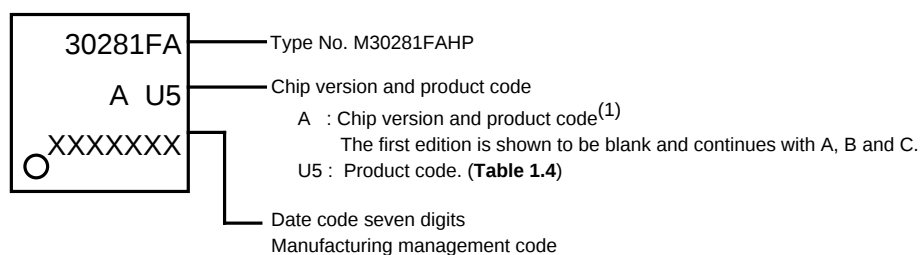
(1) Flash Memory Version, PTLG0085JB-A (85F0G), Normal-ver.



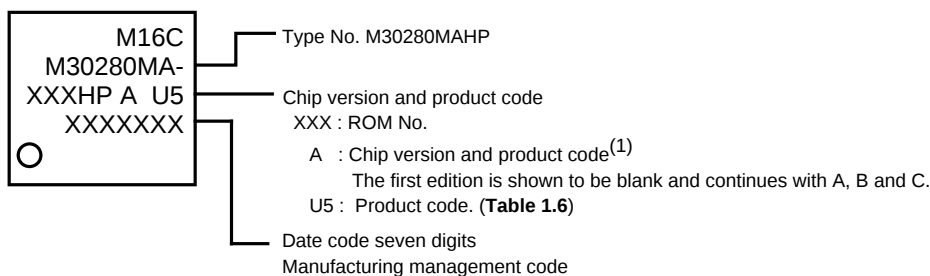
(2) Flash Memory Version, PLQP0080KB-A (80P6Q-A), Normal-ver.



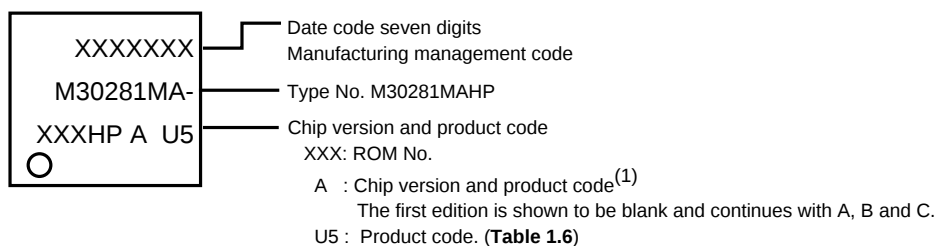
(3) Flash Memory Version, PLQP0064KB-A (64P6Q-A), Normal-ver.



(4) Mask ROM Version, PLQP0080KB-A (80P6Q-A), Normal-ver.



(5) Mask ROM Version, PLQP0064-KB-A (64P6Q-A), Normal-ver.



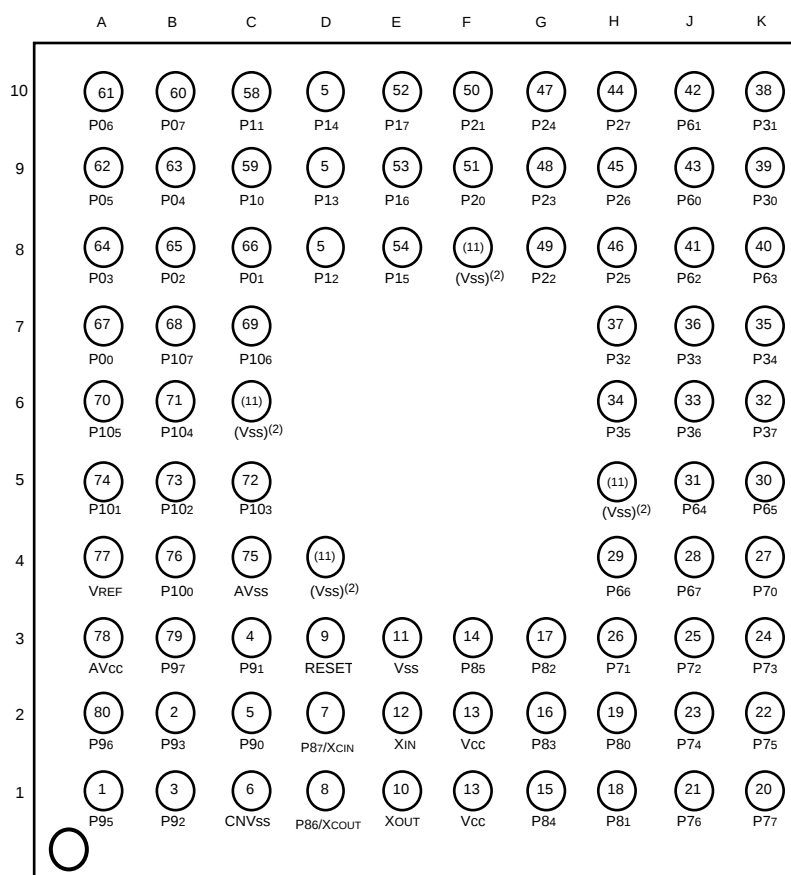
NOTES:

- The following functions are not available in the first version and version A products.
 - Delay trigger mode 0 of A/D conversion
 - Delay trigger mode 1 of A/D conversion

Figure 1.4 Marking Diagram-M16C/28 Normal-ver.

1.5 Pin Assignment

Figures 1.5 to 1.7 show the pin Assignments (top view).



NOTES :

1. The numbers in each grid (circle) show the pin numbers of the M30280FAHP (80P6Q-A package)
2. Connect grids written as (Vss) to Vss(GND) or leave them open.
3. Set PACR2 to PACR0 bits in the PACR register to "0112" before you input and output it after resetting to each pin. When the PACR register is not set, the input and output function of some pins are disabled.

Package: PTLG0085JB-A(85F0G)

Figure 1.5 Pin Assignment (Top View) of 85-pin Package

Table 1.8 Pin Characteristics for 85-pin Package (continued)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	Timer S Pin	UART Pin	Multi-master I ² C bus Pin	Analog Pin	PLQP0080KB-A Pin Number
E8		P15	$\overline{\text{INT}}_3$	IDV				ADTRG	54
E9		P16	$\overline{\text{INT}}_4$	IDW					53
E10		P17	$\overline{\text{INT}}_5$	IDU	INPC17				52
F1	Vcc								13
F2	Vcc								13
F3		P85	$\overline{\text{NMI}}$	$\overline{\text{SD}}$					14
F8	Vss ⁽¹⁾								(11)
F9		P20			OUTC10 / INPC10		SDAMM		51
F10		P21			OUTC11 / INPC11		SCLMM		50
G1		P84	$\overline{\text{INT}}_2$	ZP					15
G2		P83	$\overline{\text{INT}}_1$						16
G3		P82	$\overline{\text{INT}}_0$						17
G8		P22			OUTC12 / INPC12				49
G9		P23			OUTC13 / INPC13				48
G10		P24			OUTC14 / INPC14				47
H1		P81		TA4IN / $\overline{\text{U}}$					18
H2		P80		TA4OUT / U					19
H3		P71		TA0IN		RxD2 / SCL2 / CLK1			26
H4		P66				RxD1			29
H5	Vss ⁽¹⁾								(11)
H6		P35							34
H7		P32				SOUT3			37
H8		P25			OUTC15 / INPC15				46
H9		P26			OUTC16 / INPC16				45
H10		P27			OUTC17 / INPC17				44
J1		P76		TA3OUT					21
J2		P74		TA2OUT / W					23
J3		P72		TA1OUT / V		CLK2 / RxD1			25
J4		P67				TxD1			28
J5		P64				$\overline{\text{RTS}}_1 / \overline{\text{CTS}}_1 / \overline{\text{CTS}}_0 / \text{CLKS}_1$			31
J6		P36							33
J7		P33							36
J8		P62				RxD0			41
J9		P60				$\overline{\text{RTS}}_0 / \overline{\text{CTS}}_0$			43
J10		P61				CLK0			42
K1		P77		TA3IN					20
K2		P75		TA2IN / $\overline{\text{W}}$					22
K3		P73		TA1IN / $\overline{\text{V}}$		$\overline{\text{CTS}}_2 / \overline{\text{RTS}}_2 / \overline{\text{TxD}}_1$			24
K4		P70		TA0OUT		TxD2 / SDA2 / $\overline{\text{RTS}}_1 / \overline{\text{CTS}}_1 / \overline{\text{CTS}}_0 / \text{CLKS}_1$			27
K5		P65				CLK1			30
K6		P37							32
K7		P34							35
K8		P63				TxD0			40
K9		P30				CLK3			39
K10		P31				SIN3			38

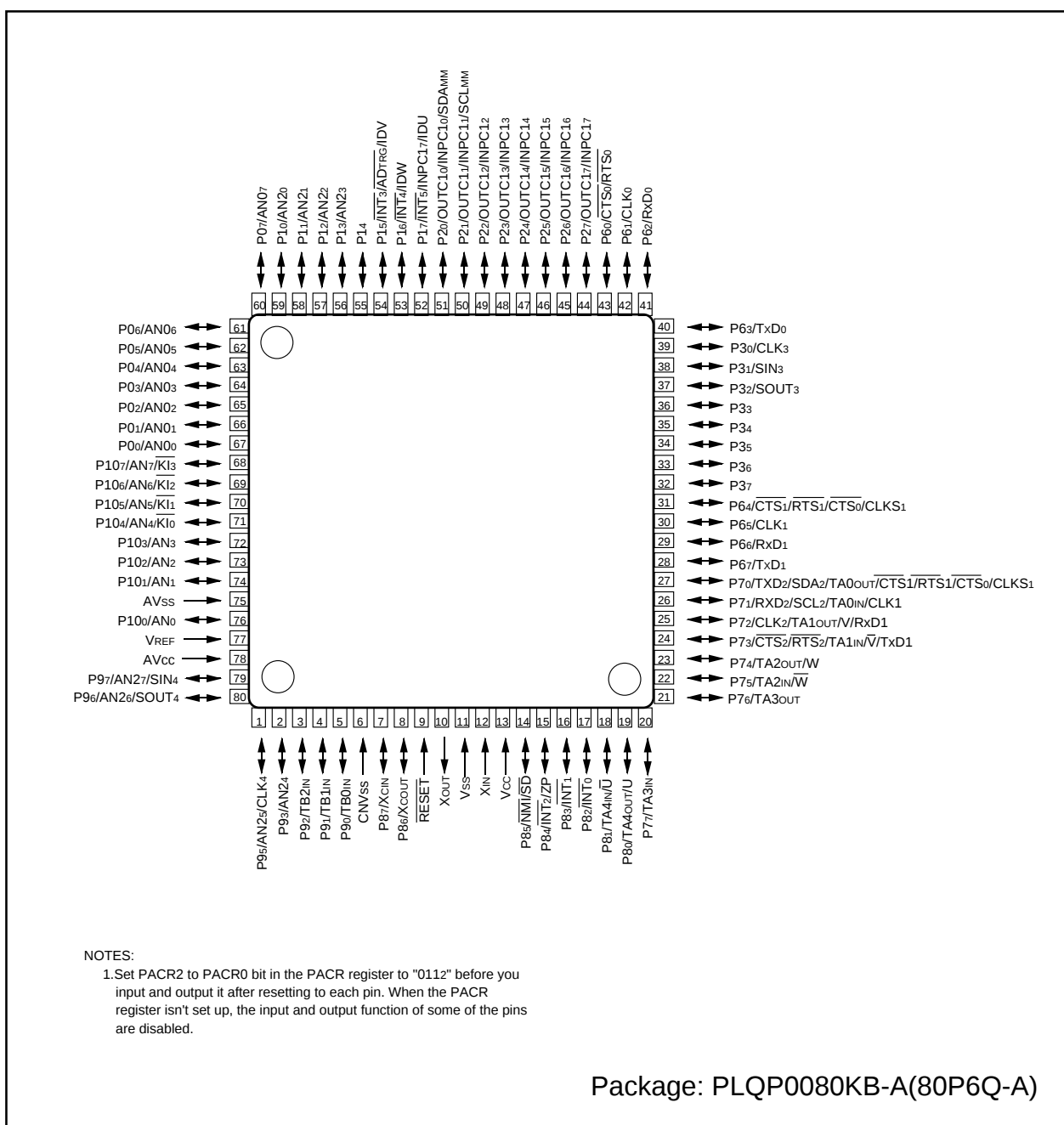


Figure 1.5 Pin Assignment (Top View) of 80-Pin Package

Table 1.9 Pin Characteristics for 80-Pin Package (Continued)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	Timer S Pin	UART Pin	Multi-master I ² C bus Pin	Analog Pin
41		P62				RxD0		
42		P61				CLK0		
43		P60				$\overline{\text{RTS}}_0 / \overline{\text{CTS}}_0$		
44		P27			OUTC17 / INPC17			
45		P26			OUTC16 / INPC16			
46		P25			OUTC15 / INPC15			
47		P24			OUTC14 / INPC14			
48		P23			OUTC13 / INPC13			
49		P22			OUTC12 / INPC12			
50		P21			OUTC11 / INPC11		SCLMM	
51		P20			OUTC10 / INPC10		SDAMM	
52		P17	$\overline{\text{INT}}_5$	IDU	INPC17			
53		P16	$\overline{\text{INT}}_4$	IDW				
54		P15	$\overline{\text{INT}}_3$	IDV				$\overline{\text{ADTRG}}$
55		P14						
56		P13						AN23
57		P12						AN22
58		P11						AN21
59		P10						AN20
60		P07						AN07
61		P06						AN06
62		P05						AN05
63		P04						AN04
64		P03						AN03
65		P02						AN02
66		P01						AN01
67		P00						AN00
68		P107	$\overline{\text{KI}}_3$					AN7
69		P106	$\overline{\text{KI}}_2$					AN6
70		P105	$\overline{\text{KI}}_1$					AN5
71		P104	$\overline{\text{KI}}_0$					AN4
72		P103						AN3
73		P102						AN2
74		P101						AN1
75	AVss							
76		P100						AN0
77	VREF							
78	AVcc							
79		P97				SIN4		AN27
80		P96				SOUT4		AN26

Table 10 Pin Characteristics for 64-Pin Package (Continued)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	Timer S Pin	UART Pin	Multi-master I ² C bus Pin	Analog Pin
41		P23			OUTC13 / INPC13			
42		P22			OUTC12 / INPC12			
43		P21			OUTC11 / INPC11		SCLMM	
44		P20			OUTC10 / INPC10		SDAMM	
45		P17	$\overline{\text{INT}}_5$	IDU	INPC17			
46		P16	$\overline{\text{INT}}_4$	IDW				
47		P15	$\overline{\text{INT}}_3$	IDV				$\overline{\text{ADTRG}}$
48		P03						AN03
49		P02						AN02
50		P01						AN01
51		P00						AN00
52		P107	$\overline{\text{KI}}_3$					AN7
53		P106	$\overline{\text{KI}}_2$					AN6
54		P105	$\overline{\text{KI}}_1$					AN5
55		P104	$\overline{\text{KI}}_0$					AN4
56		P103						AN3
57		P102						AN2
58		P101						AN1
59	AVss							
60		P100						AN0
61	VREF							
62	AVcc							
63		P93						AN24
64		P92		TB2IN				

1.6 Pin Description

Table 1.10 Pin Description (64-Pin, 80-Pin and 85-Pin Packages)

Classification	Symbol	I/O Type	Function
Power Supply	VCC, VSS	I	Apply 2.7 to 5.5V to the VCC pin. Apply 0V to the VSS pin.
Analog Power Supply	AVCC AVSS	I	Supplies power to the A/D converter. Connect the AVCC pin to VCC and the AVSS pin to VSS.
Reset Input	RESET	I	The MCU is in a reset state when "L" is applied to the RESET pin
CNVSS	CNVSS	I	Connect the CNVSS pin to VSS.
Main Clock Input	XIN	I	I/O pins for the main clock oscillation circuit. Connect a ceramic resonator or crystal oscillator between XIN and XOUT. To apply external clock, apply it to XIN and leave XOUT open. If XIN is not used (for external oscillator or external clock) connect XIN pin to VCC and leave XOUT open.
Main Clock Output	XOUT	O	
Sub Clock Input	XCIN	I	I/O pins for the sub clock oscillation circuit. Connect a crystal oscillator between XCIN and XCOUT.
Sub Clock Output	XCOUT	O	
INT Interrupt Input	INT0 to INT5	I	Input pins for the INT interrupt. INT2 can be used for Timer A Z-phase function.
NMI Interrupt Input	NMI	I	Input pin for the NMI interrupt. NMI cannot be used as I/O port while the three-phase motor control is enabled. Apply a stable "H" to NMI after setting it's direction register to "0" when the three-phase motor control is enabled.
Key Input Interrupt	KI0 to KI3	I	Input pins for the key input interrupt
Timer A	TA0OUT to TA4OUT	I/O	I/O pins for the timer A0 to A4
	TA0IN to TA4IN	I	Input pins for the timer A0 to A4
	ZP	I	Input pin for Z-phase
Timer B	TB0IN to TB2IN	I	Input pins for the timer B0 to B2
Three-phase Motor Control	U, $\bar{U}$, V, $\bar{V}$, W, $\bar{W}$	O	Output pins for the three-phase motor control timer
Timer Output	IDU, IDW, IDV, $\bar{S}\bar{D}$	I/O	Input and output pins for the three-phase motor control timer
Serial I/O	CTS0 to CTS2	I	Input pins for data transmission control
	RTS0 to RTS2	O	Output pins for data reception control
	CLK0 to CLK3	I/O	Inputs and outputs the transfer clock
	RxD0 to RxD2	I	Inputs serial data
	TxD0 to TxD2	O	Outputs serial data
	CLKS1	O	Output pin for transfer clock
I ² C Mode	SDA2	I/O	Inputs and outputs serial data
	SCL2		Inputs and outputs the transfer clock
Multi-master I ² C bus	SDAMM	I/O	Inputs and outputs serial data
	SCLMM		Inputs and outputs the transfer clock
Reference Voltage Input	VREF	I	Applies reference voltage to the A/D converter
A/D Converter	AN0 to AN7 AN00 to AN03 AN24	I	Analog input pins for the A/D converter
	ADTRG		Input pin for an external A/D trigger

I : Input O : Output I/O : Input and output

Table 1.10 Pin Description (64-Pin, 80-Pin and 85-Pin Packages) (Continued)

Classification	Symbol	I/O Type	Function
Timer S	INPC10 to INPC17	I	Input pins for the time measurement function
	OUTC10 to OUTC17	O	Output pins for the waveform generating function
I/O Ports	P00 to P03 P15 to P17 P20 to P27 P30 to P33 P60 to P67 P70 to P77 P80 to P87 P100 to P107	I/O	I/O ports for CMOS. Each port can be programmed for input or output under the control of the direction register. An input port can be set, by program, for a pull-up resistor available or for no pull-up resistor available in 4-bit units
	P90 to P93	I/O	I/O ports having equivalent functions to P0

I : Input O : Output I/O : Input and output

2.3 Frame Base Register (FB)

FB is configured with 16 bits, and is used for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is configured with 20 bits, indicating the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC is configured with 20 bits, indicating the address of an instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

Stack pointer (SP) comes in two types: USP and ISP, each configured with 16 bits.

Your desired type of stack pointer (USP or ISP) can be selected by the U flag of FLG.

2.7 Static Base Register (SB)

SB is configured with 16 bits, and is used for SB relative addressing.

2.8 Flag Register (FLG)

FLG consists of 11 bits, indicating the CPU status.

2.8.1 Carry Flag (C Flag)

This flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic/logic unit.

2.8.2 Debug Flag (D Flag)

The D flag is used exclusively for debugging purpose. During normal use, it must be set to 0.

2.8.3 Zero Flag (Z Flag)

This flag is set to 1 when an arithmetic operation resulted in 0; otherwise, it is 0.

2.8.4 Sign Flag (S Flag)

This flag is set to 1 when an arithmetic operation resulted in a negative value; otherwise, it is 0.

2.8.5 Register Bank Select Flag (B Flag)

Register bank 0 is selected when this flag is 0 ; register bank 1 is selected when this flag is 1.

2.8.6 Overflow Flag (O Flag)

This flag is set to 1 when the operation resulted in an overflow; otherwise, it is 0.

2.8.7 Interrupt Enable Flag (I Flag)

This flag enables a maskable interrupt.

Maskable interrupts are disabled when the I flag is 0, and are enabled when the I flag is 1. The I flag is cleared to 0 when the interrupt request is accepted.

2.8.8 Stack Pointer Select Flag (U Flag)

ISP is selected when the U flag is 0; USP is selected when the U flag is 1.

The U flag is cleared to 0 when a hardware interrupt request is accepted or an INT instruction for software interrupt Nos. 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is configured with three bits, for specification of up to eight processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has priority greater than IPL, the interrupt is enabled.

2.8.10 Reserved Area

When write to this bit, write 0. When read, its content is indeterminate.

3. Memory

Figure 3.1 is a memory map of the M16C/28 Group (M16C/28, M16C/28B). M16C/28 Group provides 1-Mbyte address space from addresses 00000₁₆ to FFFFF₁₆. The internal ROM is allocated lower addresses beginning with address FFFFF₁₆. For example, 64 Kbytes internal ROM is allocated addresses F0000₁₆ to FFFFF₁₆.

Two 2-Kbyte internal ROM areas, block A and block B, are available in the flash memory version. The blocks are allocated addresses F000₁₆ to FFFF₁₆.

The fixed interrupt vector tables are allocated addresses FFFDC₁₆ to FFFFF₁₆. It stores the starting address of each interrupt routine. See the section on interrupts for details.

The internal RAM is allocated higher addresses beginning with address 00400₁₆. For example, 4-Kbytes internal RAM is allocated addresses 00400₁₆ to 013FF₁₆. Besides storing data, it becomes stacks when the subroutine is called or an interrupt is acknowledged.

SFR, consisting of control registers for peripheral functions such as I/O port, A/D converter, serial I/O, timers is allocated addresses 00000₁₆ to 003FF₁₆. All blank spaces within SFR are reserved and cannot be accessed by users.

The special page vector table is allocated to the addresses FFE00₁₆ to FFFDB₁₆. This vector is used by the JMPS or JSRS instruction. For details, refer to the **M16C/60 and M16C/20 Series Software Manual**.

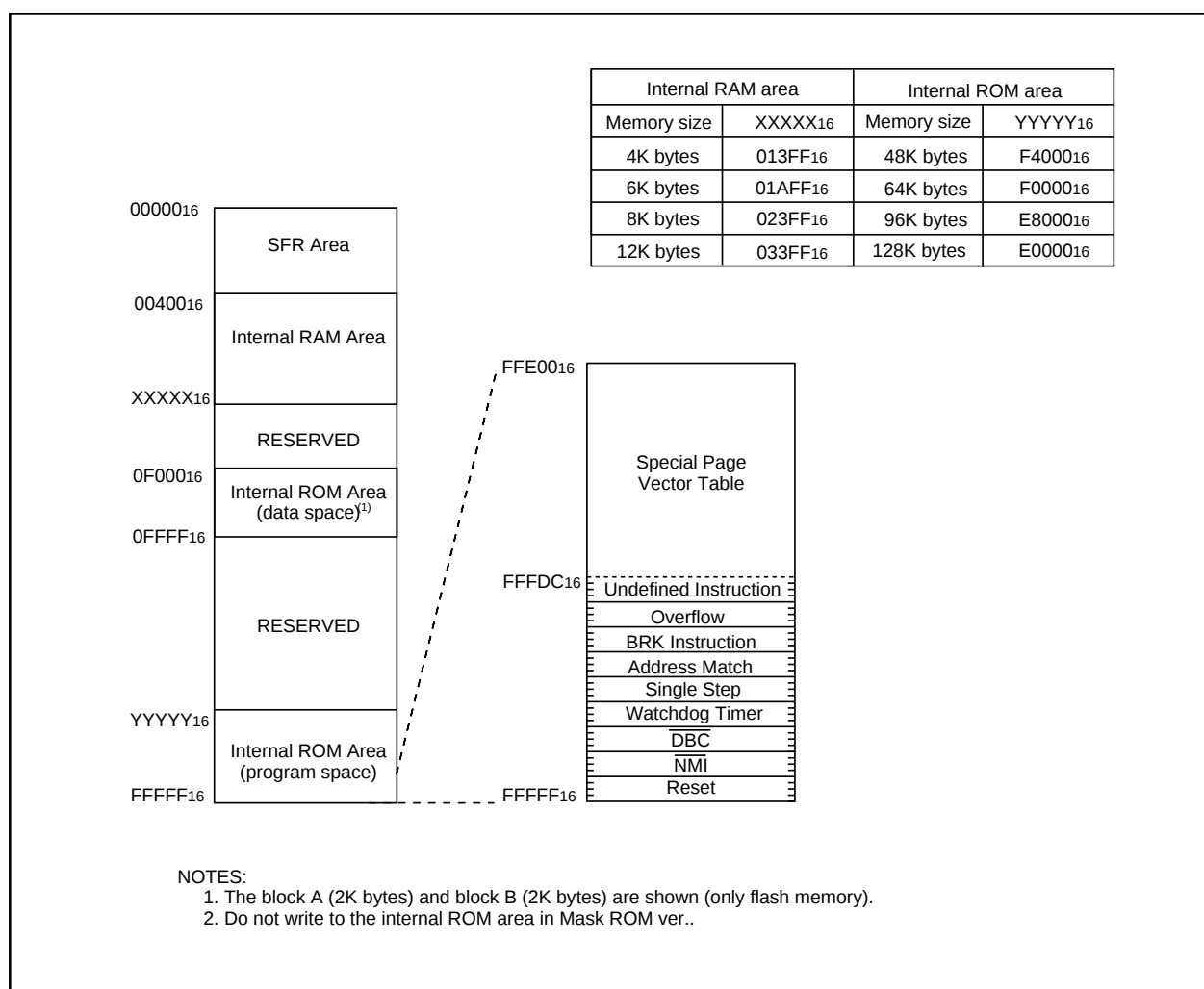


Figure 3.1 Memory Map

Table 4.3 SFR Information(3)(1)

Address	Register	Symbol	After Reset
01B0 ₁₆			
01B1 ₁₆			
01B2 ₁₆			
01B3 ₁₆	Flash memory control register 4 ⁽²⁾	FMR4	010000002
01B4 ₁₆			
01B5 ₁₆	Flash memory control register 1 ⁽²⁾	FMR1	000XX0X2
01B6 ₁₆			
01B7 ₁₆	Flash memory control register 0 ⁽²⁾	FMR0	000000012
01B8 ₁₆			
01B9 ₁₆			
0210 ₁₆	Low-power Consumption Control 0	LPCC0	X00000012
0211 ₁₆			
0212 ₁₆			
0213 ₁₆			
0214 ₁₆			
0215 ₁₆			
0216 ₁₆			
0217 ₁₆			
0218 ₁₆			
0219 ₁₆			
0250 ₁₆			
0251 ₁₆			
0252 ₁₆			
0253 ₁₆			
0254 ₁₆			
0255 ₁₆			
0256 ₁₆			
0257 ₁₆			
0258 ₁₆			
0259 ₁₆			
025A ₁₆			
025B ₁₆			
025C ₁₆	On-chip oscillator control register	ROCR	X00001012
025D ₁₆	Pin assignment control register	PACR	0016
025E ₁₆	Peripheral clock select register	PCLKR	000000112
025F ₁₆	Low-power Consumption Control 1	LPCC1	0016
02E0 ₁₆	I ² C0 data shift register	S00	XX16
02E1 ₁₆			
02E2 ₁₆	I ² C0 address register	S0D0	0016
02E3 ₁₆	I ² C0 control register 0	S1D0	0016
02E4 ₁₆	I ² C0 clock control register	S20	0016
02E5 ₁₆	I ² C0 start/stop condition control register	S2D0	000110102
02E6 ₁₆	I ² C0 control register 1	S3D0	001100002
02E7 ₁₆	I ² C0 control register 2	S4D0	0016
02E8 ₁₆	I ² C0 status register	S10	0001000X2
02E9 ₁₆			
02EA ₁₆			
02FE ₁₆			
02FF ₁₆			

Note 1: The blank spaces are reserved. No access is allowed.

Note 2: This register is included in the flash memory version.

X : Undefined

Table 4.4 SFR Information(4)(1)

Address	Register	Symbol	After Reset
0300 ₁₆ 0301 ₁₆	TM, WG register 0	G1TM0, G1PO0	XX ₁₆ XX ₁₆
0302 ₁₆ 0303 ₁₆	TM, WG register 1	G1TM1, G1PO1	XX ₁₆ XX ₁₆
0304 ₁₆ 0305 ₁₆	TM, WG register 2	G1TM2, G1PO2	XX ₁₆ XX ₁₆
0306 ₁₆ 0307 ₁₆	TM, WG register 3	G1TM3, G1PO3	XX ₁₆ XX ₁₆
0308 ₁₆ 0309 ₁₆	TM, WG register 4	G1TM4, G1PO4	XX ₁₆ XX ₁₆
030A ₁₆ 030B ₁₆	TM, WG register 5	G1TM5, G1PO5	XX ₁₆ XX ₁₆
030C ₁₆ 030D ₁₆	TM, WG register 6	G1TM6, G1PO6	XX ₁₆ XX ₁₆
030E ₁₆ 030F ₁₆	TM, WG register 7	G1TM7, G1PO7	XX ₁₆ XX ₁₆
0310 ₁₆	WG control register 0	G1POCR0	0X00XX002
0311 ₁₆	WG control register 1	G1POCR1	0X00XX002
0312 ₁₆	WG control register 2	G1POCR2	0X00XX002
0313 ₁₆	WG control register 3	G1POCR3	0X00XX002
0314 ₁₆	WG control register 4	G1POCR4	0X00XX002
0315 ₁₆	WG control register 5	G1POCR5	0X00XX002
0316 ₁₆	WG control register 6	G1POCR6	0X00XX002
0317 ₁₆	WG control register 7	G1POCR7	0X00XX002
0318 ₁₆	TM control register 0	G1TMCR0	00 ₁₆
0319 ₁₆	TM control register 1	G1TMCR1	00 ₁₆
031A ₁₆	TM control register 2	G1TMCR2	00 ₁₆
031B ₁₆	TM control register 3	G1TMCR3	00 ₁₆
031C ₁₆	TM control register 4	G1TMCR4	00 ₁₆
031D ₁₆	TM control register 5	G1TMCR5	00 ₁₆
031E ₁₆	TM control register 6	G1TMCR6	00 ₁₆
031F ₁₆	TM control register 7	G1TMCR7	00 ₁₆
0320 ₁₆ 0321 ₁₆	Base timer register	G1BT	XX ₁₆ XX ₁₆
0322 ₁₆	Base timer control register 0	G1BCR0	00 ₁₆
0323 ₁₆	Base timer control register 1	G1BCR1	00 ₁₆
0324 ₁₆	TM prescale register 6	G1TPR6	00 ₁₆
0325 ₁₆	TM prescale register 7	G1TPR7	00 ₁₆
0326 ₁₆	Function enable register	G1FE	00 ₁₆
0327 ₁₆	Function select register	G1FS	00 ₁₆
0328 ₁₆ 0329 ₁₆	Base timer reset register	G1BTRR	XX ₁₆ XX ₁₆
032A ₁₆ 032B ₁₆	Divider register	G1DV	00 ₁₆
032C ₁₆			
032D ₁₆			
032E ₁₆			
032F ₁₆			
0330 ₁₆	Interrupt request register	G1IR	XX ₁₆
0331 ₁₆	Interrupt enable register 0	G1IE0	00 ₁₆
0332 ₁₆	Interrupt enable register 1	G1IE1	00 ₁₆
0333 ₁₆			
0334 ₁₆			
0335 ₁₆			
0336 ₁₆			
0337 ₁₆			
0338 ₁₆			
0339 ₁₆			
033A ₁₆			
033B ₁₆			
033C ₁₆			
033D ₁₆			
033E ₁₆	NMI digital debounce register	NDDR	FF ₁₆
033F ₁₆	P17 digital debounce register	P17DDR	FF ₁₆

Note 1: The blank spaces are reserved. No access is allowed.

X : Undefined

Table 4.6 SFR Information(6)⁽¹⁾

Address	Register	Symbol	After Reset
0380 ₁₆	Count start flag	TABSR	00 ₁₆
0381 ₁₆	Clock prescaler reset flag	CPSRF	0XXXXXX2
0382 ₁₆	One-shot start flag	ONSF	00 ₁₆
0383 ₁₆	Trigger select register	TRGSR	00 ₁₆
0384 ₁₆	Up-down flag	UDF	00 ₁₆
0385 ₁₆			
0386 ₁₆	Timer A0 register	TA0	XX ₁₆
0387 ₁₆			XX ₁₆
0388 ₁₆	Timer A1 register	TA1	XX ₁₆
0389 ₁₆			XX ₁₆
038A ₁₆	Timer A2 register	TA2	XX ₁₆
038B ₁₆			XX ₁₆
038C ₁₆	Timer A3 register	TA3	XX ₁₆
038D ₁₆			XX ₁₆
038E ₁₆	Timer A4 register	TA4	XX ₁₆
038F ₁₆			XX ₁₆
0390 ₁₆	Timer B0 register	TB0	XX ₁₆
0391 ₁₆			XX ₁₆
0392 ₁₆	Timer B1 register	TB1	XX ₁₆
0393 ₁₆			XX ₁₆
0394 ₁₆	Timer B2 register	TB2	XX ₁₆
0395 ₁₆			XX ₁₆
0396 ₁₆	Timer A0 mode register	TA0MR	00 ₁₆
0397 ₁₆	Timer A1 mode register	TA1MR	00 ₁₆
0398 ₁₆	Timer A2 mode register	TA2MR	00 ₁₆
0399 ₁₆	Timer A3 mode register	TA3MR	00 ₁₆
039A ₁₆	Timer A4 mode register	TA4MR	00 ₁₆
039B ₁₆	Timer B0 mode register	TB0MR	00XX00002
039C ₁₆	Timer B1 mode register	TB1MR	00XX00002
039D ₁₆	Timer B2 mode register	TB2MR	00XX00002
039E ₁₆	Timer B2 special mode register	TB2SC	X00000002
039F ₁₆			
03A0 ₁₆	UART0 transmit/receive mode register	U0MR	00 ₁₆
03A1 ₁₆	UART0 bit rate generator	U0BRG	XX ₁₆
03A2 ₁₆	UART0 transmit buffer register	U0TB	XX ₁₆
03A3 ₁₆			XX ₁₆
03A4 ₁₆	UART0 transmit/receive control register 0	U0C0	000010002
03A5 ₁₆	UART0 transmit/receive control register 1	U0C1	000000102
03A6 ₁₆	UART0 receive buffer register	U0RB	XX ₁₆
03A7 ₁₆			XX ₁₆
03A8 ₁₆	UART1 transmit/receive mode register	U1MR	00 ₁₆
03A9 ₁₆	UART1 bit rate generator	U1BRG	XX ₁₆
03AA ₁₆	UART1 transmit buffer register	U1TB	XX ₁₆
03AB ₁₆			XX ₁₆
03AC ₁₆	UART1 transmit/receive control register 0	U1C0	000010002
03AD ₁₆	UART1 transmit/receive control register 1	U1C1	000000102
03AE ₁₆	UART1 receive buffer register	U1RB	XX ₁₆
03AF ₁₆			XX ₁₆
03B0 ₁₆	UART transmit/receive control register 2	UCON	X00000002
03B1 ₁₆			
03B2 ₁₆			
03B3 ₁₆			
03B4 ₁₆			
03B5 ₁₆			
03B6 ₁₆			
03B7 ₁₆			
03B8 ₁₆	DMA0 request cause select register	DM0SL	00 ₁₆
03B9 ₁₆			
03BA ₁₆	DMA1 request cause select register	DM1SL	00 ₁₆
03BB ₁₆			
03BC ₁₆			
03BD ₁₆			
03BE ₁₆			
03BF ₁₆			

Note 1: The blank spaces are reserved. No access is allowed.

X : Undefined

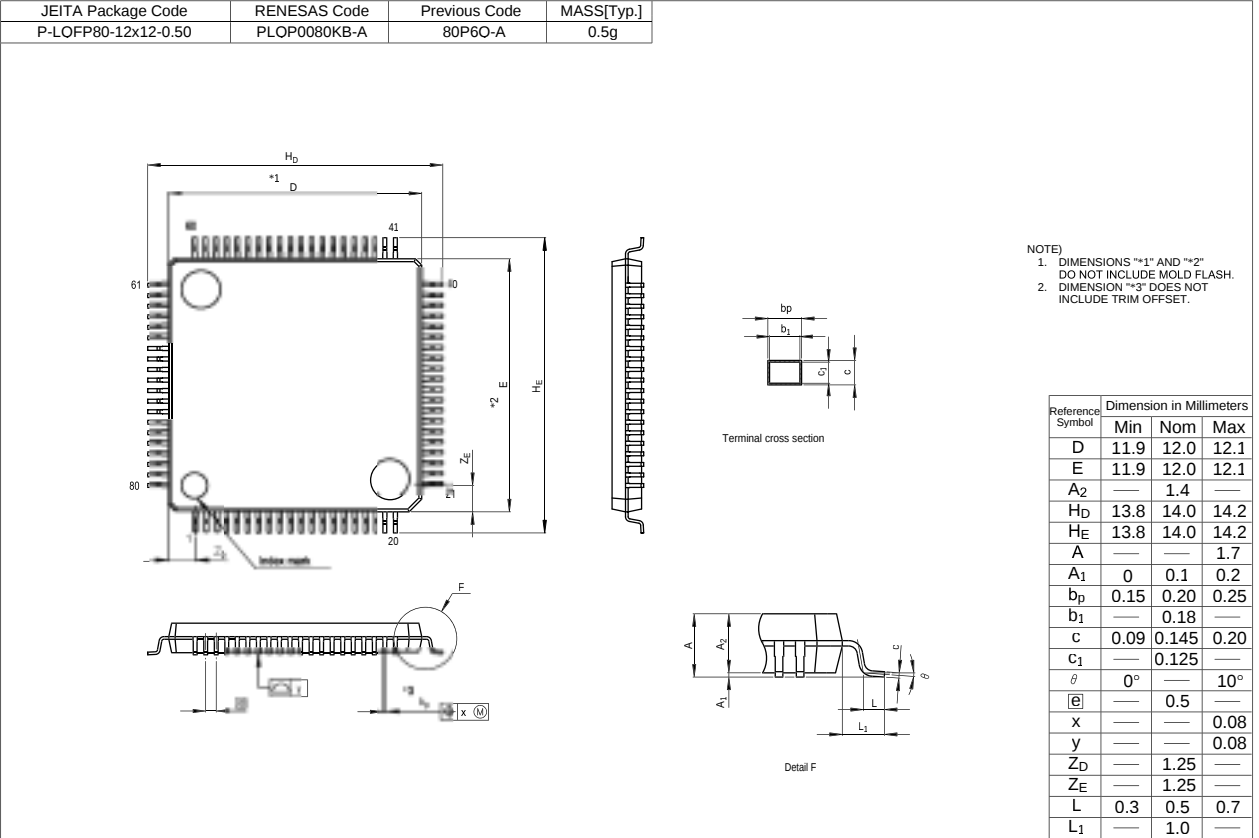
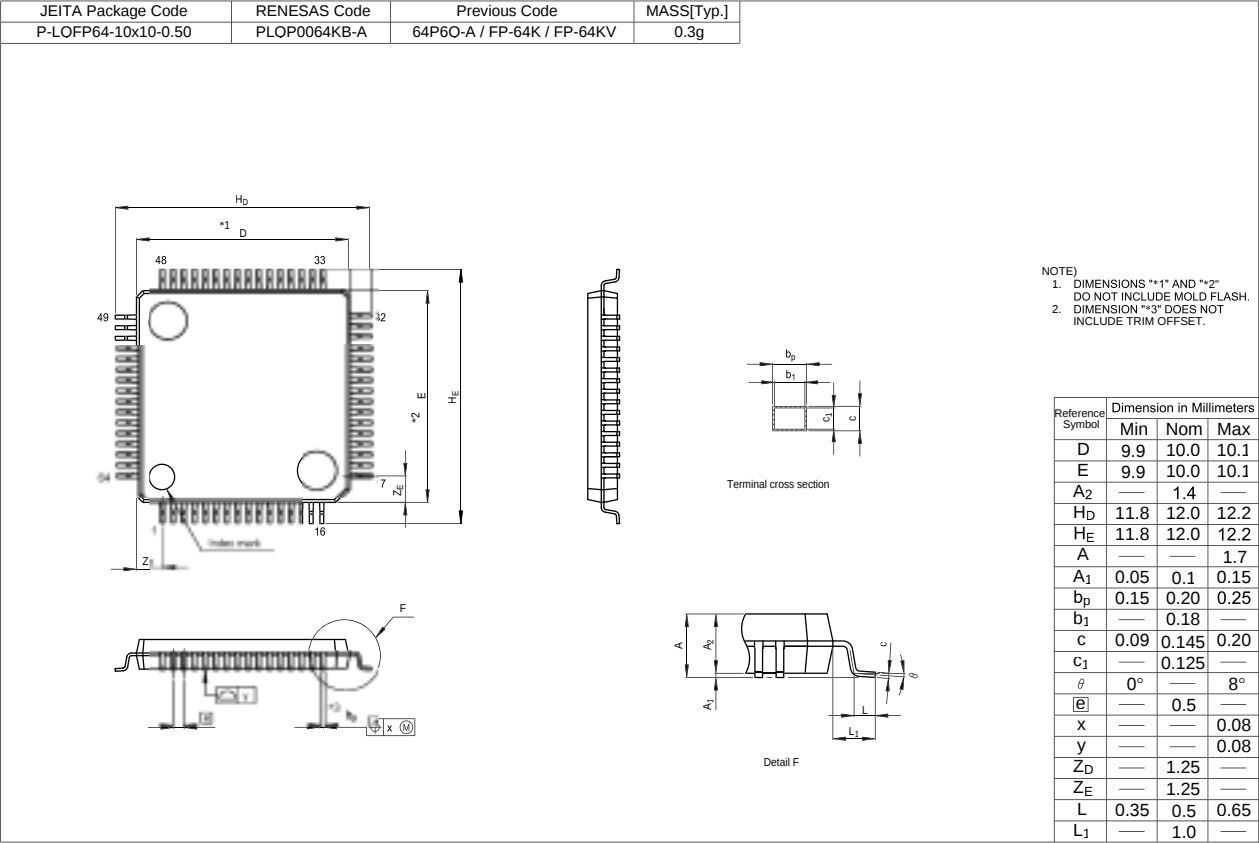
Table 4.7 SFR Information(7)(1)

Address	Register	Symbol	After Reset
03C0 ₁₆ 03C1 ₁₆	A/D register 0	AD0	XX ₁₆ XX ₁₆
03C2 ₁₆ 03C3 ₁₆	A/D register 1	AD1	XX ₁₆ XX ₁₆
03C4 ₁₆ 03C5 ₁₆	A/D register 2	AD2	XX ₁₆ XX ₁₆
03C6 ₁₆ 03C7 ₁₆	A/D register 3	AD3	XX ₁₆ XX ₁₆
03C8 ₁₆ 03C9 ₁₆	A/D register 4	AD4	XX ₁₆ XX ₁₆
03CA ₁₆ 03CB ₁₆	A/D register 5	AD5	XX ₁₆ XX ₁₆
03CC ₁₆ 03CD ₁₆	A/D register 6	AD6	XX ₁₆ XX ₁₆
03CE ₁₆ 03CF ₁₆	A/D register 7	AD7	XX ₁₆ XX ₁₆
03D0 ₁₆ 03D1 ₁₆			
03D2 ₁₆	A/D trigger control register	ADTRGCON	00 ₁₆
03D3 ₁₆	A/D convert status register 0	ADSTAT0	00000X00 ₂
03D4 ₁₆ 03D5 ₁₆	A/D control register 2	ADCON2	00 ₁₆
03D6 ₁₆	A/D control register 0	ADCON0	00000XXX ₂
03D7 ₁₆ 03D8 ₁₆	A/D control register 1	ADCON1	00 ₁₆
03D9 ₁₆ 03DA ₁₆			
03DB ₁₆ 03DC ₁₆			
03DD ₁₆ 03DE ₁₆			
03DF ₁₆			
03E0 ₁₆	Port P0 register	P0	XX ₁₆
03E1 ₁₆	Port P1 register	P1	XX ₁₆
03E2 ₁₆ 03E3 ₁₆	Port P0 direction register	PD0	00 ₁₆
03E4 ₁₆	Port P1 direction register	PD1	00 ₁₆
03E5 ₁₆	Port P2 register	P2	XX ₁₆
03E6 ₁₆	Port P3 register	P3	XX ₁₆
03E7 ₁₆ 03E8 ₁₆	Port P2 direction register	PD2	00 ₁₆
03E9 ₁₆	Port P3 direction register	PD3	00 ₁₆
03EA ₁₆ 03EB ₁₆			
03EC ₁₆	Port P6 register	P6	XX ₁₆
03ED ₁₆	Port P7 register	P7	XX ₁₆
03EE ₁₆ 03EF ₁₆	Port P6 direction register	PD6	00 ₁₆
03F0 ₁₆	Port P7 direction register	PD7	00 ₁₆
03F1 ₁₆	Port P8 register	P8	XX ₁₆
03F2 ₁₆	Port P9 register	P9	XX ₁₆
03F3 ₁₆	Port P8 direction register	PD8	00 ₁₆
03F4 ₁₆	Port P9 direction register	PD9	000X0000 ₂
03F5 ₁₆	Port P10 register	P10	XX ₁₆
03F6 ₁₆	Port P10 direction register	PD10	00 ₁₆
03F7 ₁₆ 03F8 ₁₆			
03F9 ₁₆ 03FA ₁₆			
03FB ₁₆			
03FC ₁₆	Pull-up control register 0	PUR0	00 ₁₆
03FD ₁₆	Pull-up control register 1	PUR1	00 ₁₆
03FE ₁₆	Pull-up control register 2	PUR2	00 ₁₆
03FF ₁₆	Port control register	PCR	00 ₁₆

Note 1: The blank spaces are reserved. No access is allowed.

X : Undefined

Appendix 1. Package Dimensions



Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

Keep safety first in your circuit designs!

1. Renesas Technology Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.
Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corp. product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corp. or a third party.
2. Renesas Technology Corp. assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corp. without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor for the latest product information before purchasing a product listed herein.
The information described here may contain technical inaccuracies or typographical errors.
Renesas Technology Corp. assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.
Please also pay attention to information published by Renesas Technology Corp. by various means, including the Renesas Technology Corp. Semiconductor home page (<http://www.renesas.com>).
4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corp. assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
5. Renesas Technology Corp. semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
6. The prior written approval of Renesas Technology Corp. is necessary to reprint or reproduce in whole or in part these materials.
7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.
Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
8. Please contact Renesas Technology Corp. for further details on these materials or the products contained therein.



RENESAS SALES OFFICES

<http://www.renesas.com>

Refer to "<http://www.renesas.com/en/network>" for the latest and detailed information.

Renesas Technology America, Inc.

450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited

Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology (Shanghai) Co., Ltd.

Unit 204, 205, AZIACenter, No.1233 Lujiazui Ring Rd, Pudong District, Shanghai, China 200120
Tel: <86> (21) 5877-1818, Fax: <86> (21) 6887-7898

Renesas Technology Hong Kong Ltd.

7th Floor, North Tower, World Finance Centre, Harbour City, 1 Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2730-6071

Renesas Technology Taiwan Co., Ltd.

10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology Singapore Pte. Ltd.

1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Renesas Technology Korea Co., Ltd.

Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

Renesas Technology Malaysia Sdn. Bhd

Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jalan Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510