



Welcome to [E-XFL.COM](#)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	M16C/60
Core Size	16-Bit
Speed	20MHz
Connectivity	I ² C, IEBus, SIO, UART/USART
Peripherals	DMA, POR, PWM, Voltage Detect, WDT
Number of I/O	55
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 13x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30281f6hp-u9b

1.3 Block Diagram

Figure 1.1 is a block diagram of the M16C/28 Group (M16C/28, M16C/28B), 80-pin and 85-pin package.

Figure 1.2 is a block diagram of the M16C/28 Group (M16C/28, M16C/28B), 64-pin package.

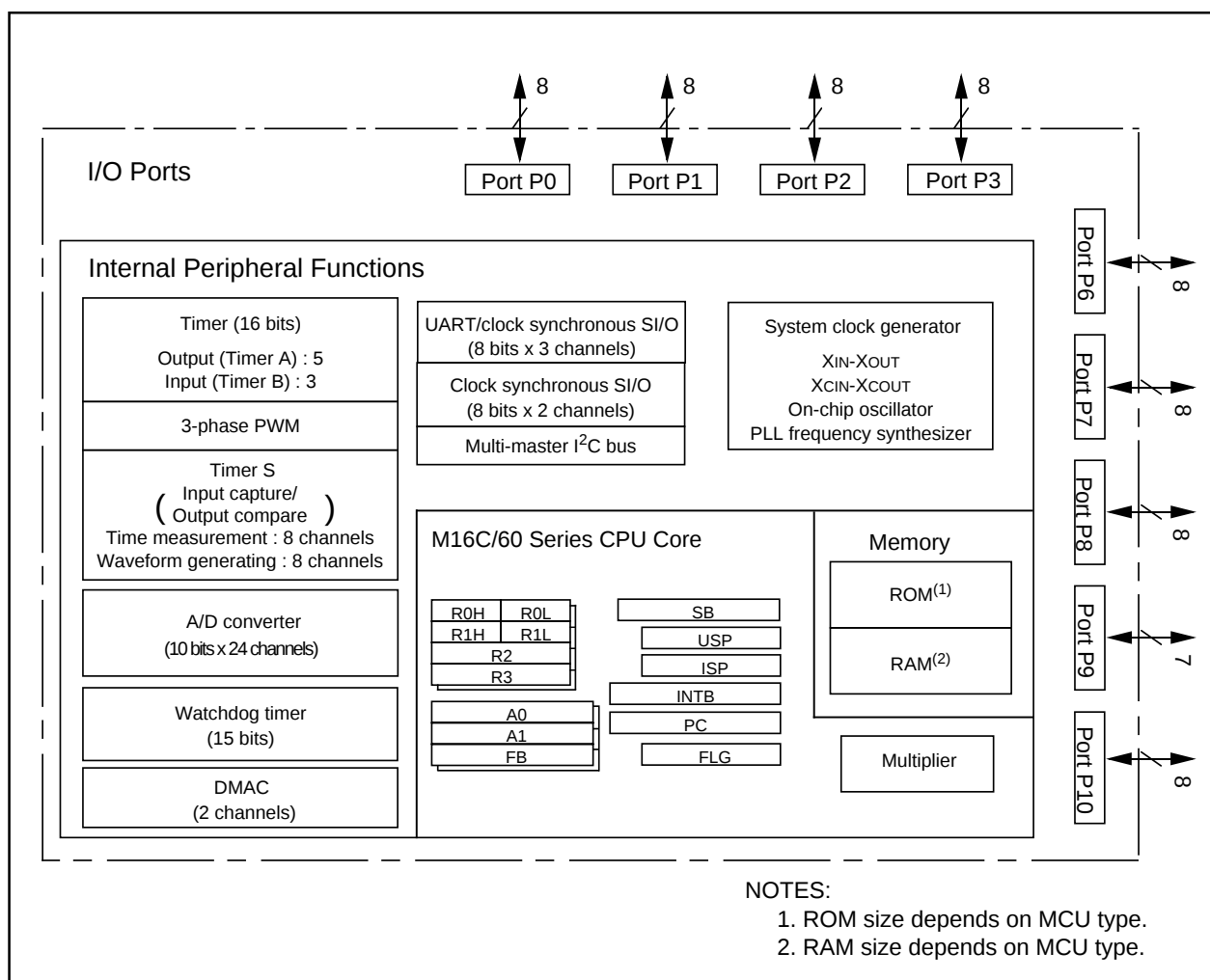


Figure 1.1 M16C/28 Group (M16C/28, M16C/28B), 80-Pin/85-Pin Block Diagram

1.4 Product Information

Tables 1.3 and 1.4 list the M16C/28 Group product information and Figure 1.3 shows the product numbering system. The specifications are partially different between normal-ver. and T/ V-ver..

Table 1.3 M16C/28 Product List -Normal-ver.

As of September, 2006

Type Number	ROM Capacity	RAM Capacity	Package Type	Remarks	Product Code
M30280F6WG (N)	48 K + 4 K	4 K	PTLG0085JB-A (85F0G)	Flash Memory	U3, U5, U7, U9
M30280F8WG (N)	64 K + 4 K	4 K			
M30280FAWG (N)	96 K + 4 K	8 K			
M30280F6HP (N)	48 K + 4 K	4 K	PLQP0080KB-A (80P6Q-A)		
M30280F8HP (N)	64 K + 4 K	4 K			
M30280FAHP (N)	96 K + 4 K	8 K			
M30280FCHP (N)	128 K + 4 K	12 K			
M30281F6HP (N)	48 K + 4 K	4 K	PLQP0064KB-A (64P6Q-A)		
M30281F8HP (N)	64 K + 4 K	4 K			
M30281FAHP (N)	96 K + 4 K	8 K			
M30281FCHP (N)	128 K + 4 K	12 K			
M30280M8-XXXHP (N)	64 K	4 K	PLQP0080KB-A (80P6Q-A)	Mask ROM	U3, U5
M30280MA-XXXHP (N)	96 K	8 K			
M30280MC-XXXHP (N)	128 K	12 K			
M30281M8-XXXHP (N)	64 K	4 K	PLQP0064KB-A (64P6Q-A)		
M30281MA-XXXHP (N)	96 K	8 K			
M30281MC-XXXHP (N)	128 K	12 K			

(N): New

Table 1.4 M16C/28B Product List -Normal-ver.

As of September, 2006

Type Number	ROM Capacity	RAM Capacity	Package Type	Remarks	Product Code
M30280FCBHP (D)	128 K + 4 K	12 K	PLQP0080KB-A (80P6Q-A)	Flash memory	U7
M30281FCBHP (D)	128 K + 4 K	12 K	PLQP0064KB-A (64P6Q-A)		

(D): Under development

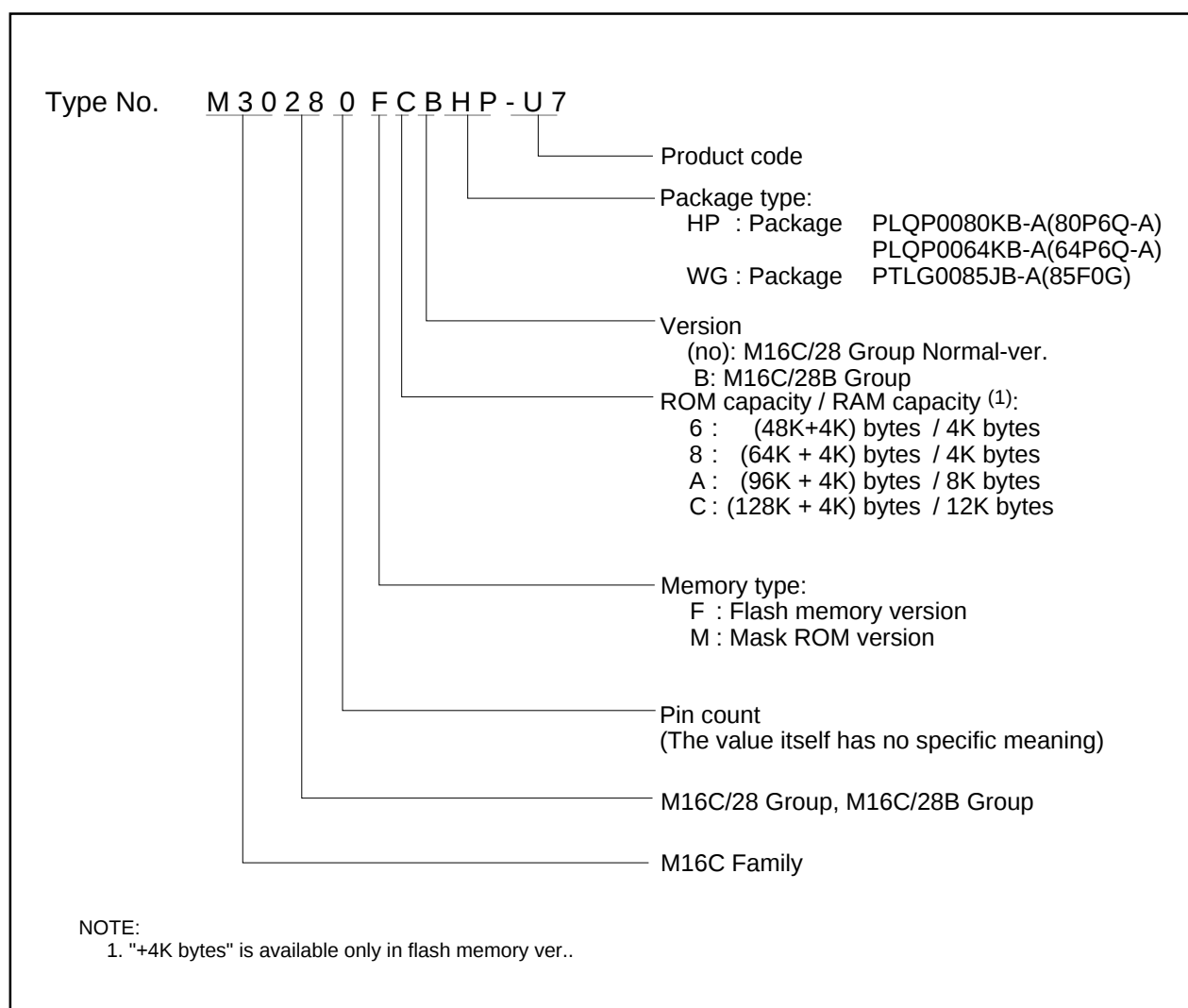


Figure 1.3 Product Numbering System

Table 1.5 Product Code (Flash Memory-ver.) - M16C/28 Normal-ver., 64-Pin⁽¹⁾/80-Pin⁽¹⁾/85-Pin Package

Product Code	Package	Internal ROM (User Program Space)		Internal ROM (Data Space)		Operating Ambient Temperature
		Program and Erase Endurance	Temperature Range	Program and Erase Endurance	Temperature Range	
U3	Lead free	100	0 to 60°C	100	0 to 60°C	-40 to 85°C
U5					-20 to 85°C	
U7		1,000		10,000	-40 to 85°C	-40 to 85°C
U9					-20 to 85°C	-20 to 85°C

NOTE:

1. The lead contained products, D3, D5, D7 and D9, are put together with U3, U5, U7 and U9 respectively. Lead-free (Sn-Ag-Cu plating) products can be mounted by both conventional Sn-Pb paste and Lead-free paste.

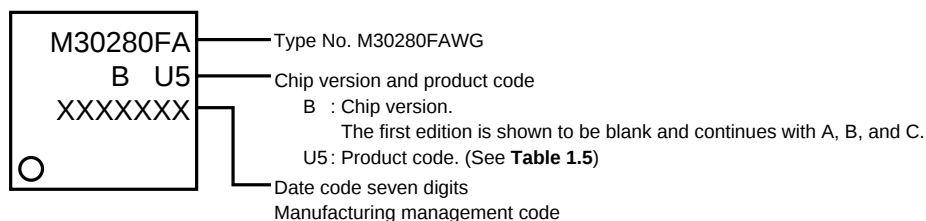
Table 1.6 Product Code (Flash Memory-ver.) - M16C/28B Normal-ver., 64-Pin/85-Pin Package

Product Code	Package	Internal ROM (User Program Space)		Internal ROM (Data Space)		Operating Ambient Temperature
		Program and Erase Endurance	Temperature Range	Program and Erase Endurance	Temperature Range	
U7	Lead-free	1,000	0 to 60°C	10,000	-40 to 85°C	-40 to 85°C

Table 1.7 Product Code (Mask ROM ver.) - M16C/28B Normal-ver., 64-Pin/80-Pin/85-Pin Package

Product Code	Package	Operating Ambient Temperature
U3	Lead-free	-40 to 85°C
U5		-20 to 85°C

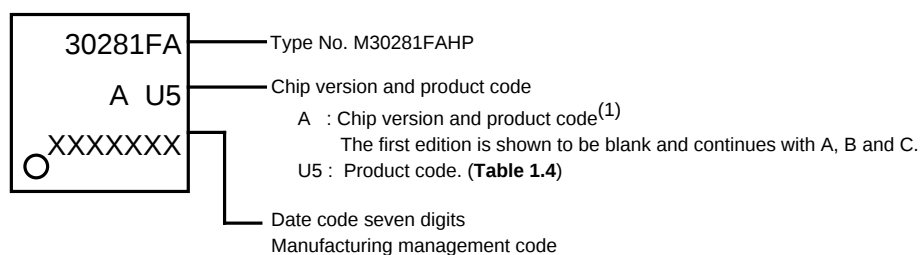
(1) Flash Memory Version, PTLG0085JB-A (85F0G), Normal-ver.



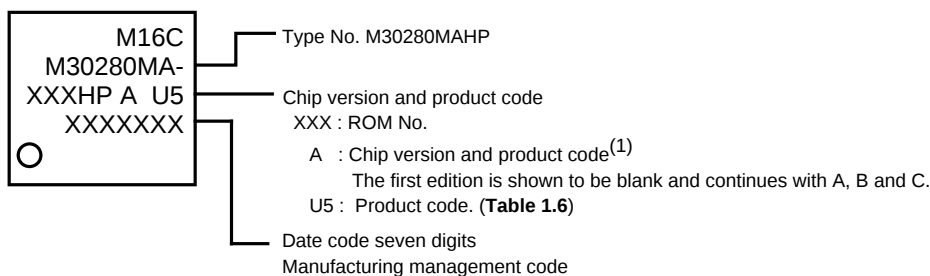
(2) Flash Memory Version, PLQP0080KB-A (80P6Q-A), Normal-ver.



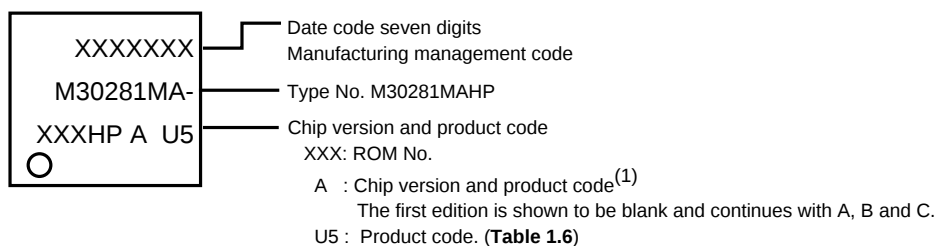
(3) Flash Memory Version, PLQP0064KB-A (64P6Q-A), Normal-ver.



(4) Mask ROM Version, PLQP0080KB-A (80P6Q-A), Normal-ver.



(5) Mask ROM Version, PLQP0064-KB-A (64P6Q-A), Normal-ver.



NOTES:

- The following functions are not available in the first version and version A products.
 - Delay trigger mode 0 of A/D conversion
 - Delay trigger mode 1 of A/D conversion

Figure 1.4 Marking Diagram-M16C/28 Normal-ver.

Table 1.8 Pin Characteristics for 85-pin Package

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	Timer S Pin	UART Pin	Multi-master I ² C bus Pin	Analog Pin	PLQP0080KB-A Pin Number
A1		P95				CLK4		AN25	1
A2		P96				SOUT4		AN26	80
A3	AVcc								78
A4	VREF								77
A5		P101						AN1	74
A6		P105	$\overline{\text{KI1}}$					AN5	70
A7		P00						AN00	67
A8		P03						AN03	64
A9		P05						AN05	62
A10		P06						AN06	61
B1		P92		TB2IN					3
B2		P93						AN24	2
B3		P97				SIN4		AN27	79
B4		P100						AN0	76
B5		P102						AN2	73
B6		P104	$\overline{\text{KI0}}$					AN4	71
B7		P107	$\overline{\text{KI3}}$					AN7	68
B8		P02						AN02	65
B9		P04						AN04	63
B10		P07						AN07	60
C1	CNVss								6
C2		P90		TB0IN					5
C3		P91		TB1IN					4
C4	AVss								75
C5		P103						AN3	72
C6	Vss ⁽¹⁾								(11)
C7		P106	$\overline{\text{KI2}}$					AN6	69
C8		P01						AN01	66
C9		P10						AN20	59
C10		P11						AN21	58
D1	XCOUT	P86							8
D2	XCIN	P87							7
D3	RESET								9
D4	Vss ⁽¹⁾								(11)
D8		P12						AN22	57
D9		P13						AN23	56
D10		P14							55
E1	XOUT								10
E2	XIN								12
E3	Vss								11

Table 1.8 Pin Characteristics for 85-pin Package (continued)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	Timer S Pin	UART Pin	Multi-master I ² C bus Pin	Analog Pin	PLQP0080KB-A Pin Number
E8		P15	$\overline{\text{INT}}_3$	IDV				ADTRG	54
E9		P16	$\overline{\text{INT}}_4$	IDW					53
E10		P17	$\overline{\text{INT}}_5$	IDU	INPC17				52
F1	Vcc								13
F2	Vcc								13
F3		P85	$\overline{\text{NMI}}$	$\overline{\text{SD}}$					14
F8	Vss ⁽¹⁾								(11)
F9		P20			OUTC10 / INPC10		SDAMM		51
F10		P21			OUTC11 / INPC11		SCLMM		50
G1		P84	$\overline{\text{INT}}_2$	ZP					15
G2		P83	$\overline{\text{INT}}_1$						16
G3		P82	$\overline{\text{INT}}_0$						17
G8		P22			OUTC12 / INPC12				49
G9		P23			OUTC13 / INPC13				48
G10		P24			OUTC14 / INPC14				47
H1		P81		TA4IN / $\overline{\text{U}}$					18
H2		P80		TA4OUT / U					19
H3		P71		TA0IN		RxD2 / SCL2 / CLK1			26
H4		P66				RxD1			29
H5	Vss ⁽¹⁾								(11)
H6		P35							34
H7		P32				SOUT3			37
H8		P25			OUTC15 / INPC15				46
H9		P26			OUTC16 / INPC16				45
H10		P27			OUTC17 / INPC17				44
J1		P76		TA3OUT					21
J2		P74		TA2OUT / W					23
J3		P72		TA1OUT / V		CLK2 / RxD1			25
J4		P67				TxD1			28
J5		P64				$\overline{\text{RTS}}_1 / \overline{\text{CTS}}_1 / \overline{\text{CTS}}_0 / \text{CLKS}_1$			31
J6		P36							33
J7		P33							36
J8		P62				RxD0			41
J9		P60				$\overline{\text{RTS}}_0 / \overline{\text{CTS}}_0$			43
J10		P61				CLK0			42
K1		P77		TA3IN					20
K2		P75		TA2IN / $\overline{\text{W}}$					22
K3		P73		TA1IN / $\overline{\text{V}}$		$\overline{\text{CTS}}_2 / \overline{\text{RTS}}_2 / \overline{\text{TXD}}_1$			24
K4		P70		TA0OUT		TxD2 / SDA2 / $\overline{\text{RTS}}_1 / \overline{\text{CTS}}_1 / \overline{\text{CTS}}_0 / \text{CLKS}_1$			27
K5		P65				CLK1			30
K6		P37							32
K7		P34							35
K8		P63				TxD0			40
K9		P30				CLK3			39
K10		P31				SIN3			38

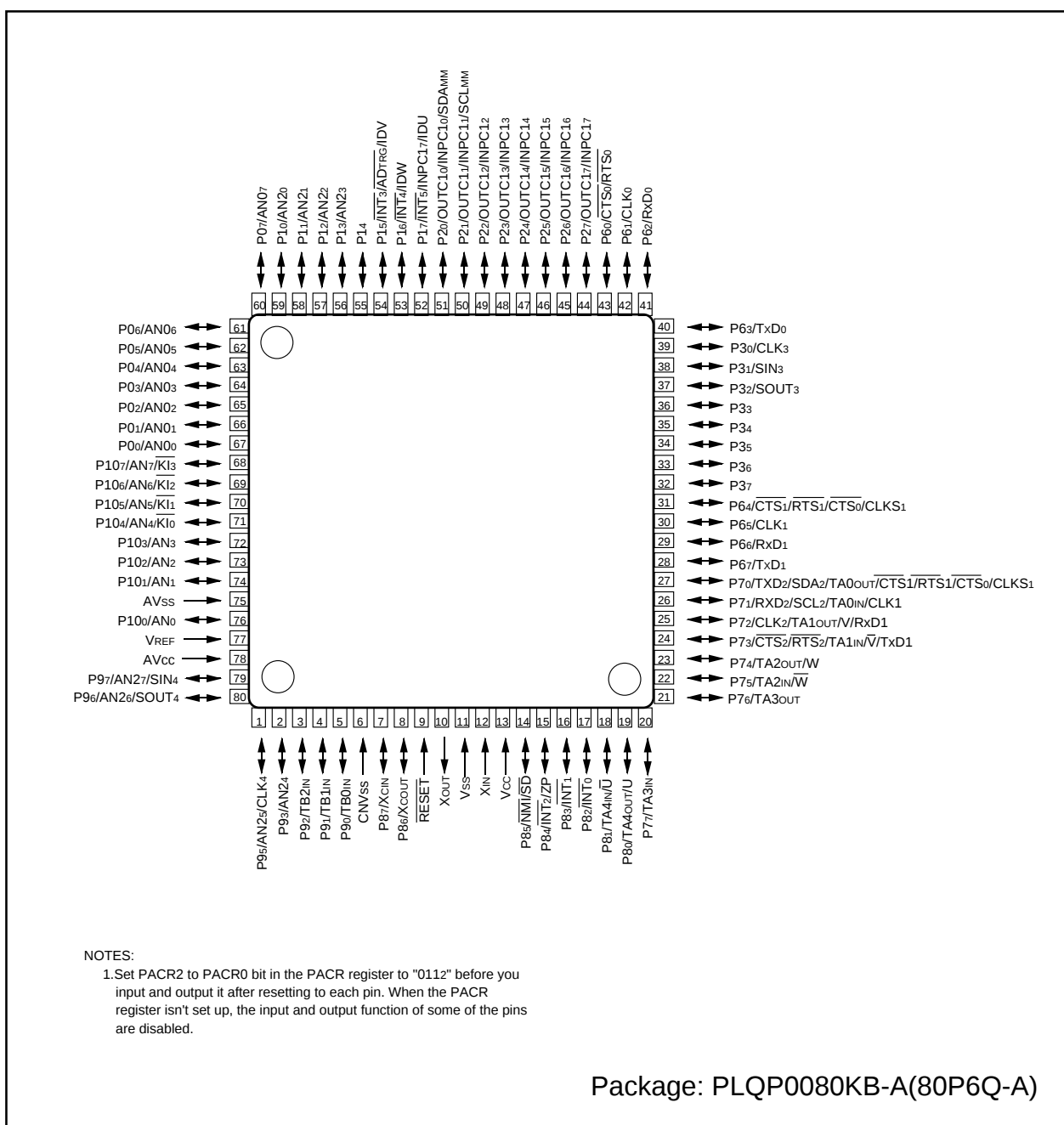


Figure 1.5 Pin Assignment (Top View) of 80-Pin Package

Table 1.9 Pin Characteristics for 80-Pin Package (Continued)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	Timer S Pin	UART Pin	Multi-master I ² C bus Pin	Analog Pin
41		P62				RxD0		
42		P61				CLK0		
43		P60				$\overline{\text{RTS}}_0 / \overline{\text{CTS}}_0$		
44		P27			OUTC17 / INPC17			
45		P26			OUTC16 / INPC16			
46		P25			OUTC15 / INPC15			
47		P24			OUTC14 / INPC14			
48		P23			OUTC13 / INPC13			
49		P22			OUTC12 / INPC12			
50		P21			OUTC11 / INPC11		SCLMM	
51		P20			OUTC10 / INPC10		SDAMM	
52		P17	$\overline{\text{INT}}_5$	IDU	INPC17			
53		P16	$\overline{\text{INT}}_4$	IDW				
54		P15	$\overline{\text{INT}}_3$	IDV				$\overline{\text{ADTRG}}$
55		P14						
56		P13						AN23
57		P12						AN22
58		P11						AN21
59		P10						AN20
60		P07						AN07
61		P06						AN06
62		P05						AN05
63		P04						AN04
64		P03						AN03
65		P02						AN02
66		P01						AN01
67		P00						AN00
68		P107	$\overline{\text{KI}}_3$					AN7
69		P106	$\overline{\text{KI}}_2$					AN6
70		P105	$\overline{\text{KI}}_1$					AN5
71		P104	$\overline{\text{KI}}_0$					AN4
72		P103						AN3
73		P102						AN2
74		P101						AN1
75	AVss							
76		P100						AN0
77	VREF							
78	AVcc							
79		P97				SIN4		AN27
80		P96				SOUT4		AN26

Table 1.10 Pin Characteristics for 64-Pin Package

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	Timer S Pin	UART Pin	Multi-master I ² C bus Pin	Analog Pin
1		P91		TA1IN				
2		P90		TB0IN				
3	CNVss							
4	XCIN	P87						
5	XCOUT	P86						
6	RESET							
7	XOUT							
8	Vss							
9	XIN							
10	Vcc							
11		P85	NMI	SD				
12		P84	INT ₂	ZP				
13		P83	INT ₁					
14		P82	INT ₀					
15		P81		TA4IN / $\bar{U}$				
16		P80		TA4OUT / U				
17		P77		TA3IN				
18		P76		TA3OUT				
19		P75		TA2IN / $\bar{W}$				
20		P74		TA2OUT / W				
21		P73		TA1IN / $\bar{V}$		CTS ₂ / $\bar{RTS}_2$ / TxD ₁		
22		P72		TA1OUT / V		CLK ₂ / RxD ₁		
23		P71		TA0IN		RxD ₂ / SCL ₂ / CLK ₁		
24		P70		TA0OUT		TxD ₂ / SDA ₂ / $\bar{RTS}_1$ / CTS ₁ / $\bar{CTS}_0$ / CLK _{S1}		
25		P67				TxD ₁		
26		P66				RxD ₁		
27		P65				CLK ₁		
28		P64				RTS ₁ / CTS ₁ / $\bar{CTS}_0$ / CLK _{S1}		
29		P33						
30		P32				SOUT ₃		
31		P31				SIN ₃		
32		P30				CLK ₃		
33		P63				TxD ₀		
34		P62				RxD ₀		
35		P61				CLK ₀		
36		P60				RTS ₀ / $\bar{CTS}_0$		
37		P27			OUTC17 / INPC17			
38		P26			OUTC16 / INPC16			
39		P25			OUTC15 / INPC15			
40		P24			OUTC14 / INPC14			

Table 10 Pin Characteristics for 64-Pin Package (Continued)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	Timer S Pin	UART Pin	Multi-master I ² C bus Pin	Analog Pin
41		P23			OUTC13 / INPC13			
42		P22			OUTC12 / INPC12			
43		P21			OUTC11 / INPC11		SCLMM	
44		P20			OUTC10 / INPC10		SDAMM	
45		P17	$\overline{\text{INT}}_5$	IDU	INPC17			
46		P16	$\overline{\text{INT}}_4$	IDW				
47		P15	$\overline{\text{INT}}_3$	IDV				$\overline{\text{ADTRG}}$
48		P03						AN03
49		P02						AN02
50		P01						AN01
51		P00						AN00
52		P107	$\overline{\text{KI}}_3$					AN7
53		P106	$\overline{\text{KI}}_2$					AN6
54		P105	$\overline{\text{KI}}_1$					AN5
55		P104	$\overline{\text{KI}}_0$					AN4
56		P103						AN3
57		P102						AN2
58		P101						AN1
59	AVss							
60		P100						AN0
61	VREF							
62	AVcc							
63		P93						AN24
64		P92		TB2IN				

1.6 Pin Description

Table 1.10 Pin Description (64-Pin, 80-Pin and 85-Pin Packages)

Classification	Symbol	I/O Type	Function
Power Supply	VCC, VSS	I	Apply 2.7 to 5.5V to the VCC pin. Apply 0V to the VSS pin.
Analog Power Supply	AVCC AVSS	I	Supplies power to the A/D converter. Connect the AVCC pin to VCC and the AVSS pin to VSS.
Reset Input	RESET	I	The MCU is in a reset state when "L" is applied to the RESET pin
CNVSS	CNVSS	I	Connect the CNVSS pin to VSS.
Main Clock Input	XIN	I	I/O pins for the main clock oscillation circuit. Connect a ceramic resonator or crystal oscillator between XIN and XOUT. To apply external clock, apply it to XIN and leave XOUT open. If XIN is not used (for external oscillator or external clock) connect XIN pin to VCC and leave XOUT open.
Main Clock Output	XOUT	O	
Sub Clock Input	XCIN	I	I/O pins for the sub clock oscillation circuit. Connect a crystal oscillator between XCIN and XCOUT.
Sub Clock Output	XCOUT	O	
INT Interrupt Input	INT0 to INT5	I	Input pins for the INT interrupt. INT2 can be used for Timer A Z-phase function.
NMI Interrupt Input	NMI	I	Input pin for the NMI interrupt. NMI cannot be used as I/O port while the three-phase motor control is enabled. Apply a stable "H" to NMI after setting it's direction register to "0" when the three-phase motor control is enabled.
Key Input Interrupt	KI0 to KI3	I	Input pins for the key input interrupt
Timer A	TA0OUT to TA4OUT	I/O	I/O pins for the timer A0 to A4
	TA0IN to TA4IN	I	Input pins for the timer A0 to A4
	ZP	I	Input pin for Z-phase
Timer B	TB0IN to TB2IN	I	Input pins for the timer B0 to B2
Three-phase Motor Control	U, $\bar{U}$, V, $\bar{V}$, W, $\bar{W}$	O	Output pins for the three-phase motor control timer
Timer Output	IDU, IDW, IDV, $\bar{S}\bar{D}$	I/O	Input and output pins for the three-phase motor control timer
Serial I/O	CTS0 to CTS2	I	Input pins for data transmission control
	RTS0 to RTS2	O	Output pins for data reception control
	CLK0 to CLK3	I/O	Inputs and outputs the transfer clock
	RxD0 to RxD2	I	Inputs serial data
	TxD0 to TxD2	O	Outputs serial data
	CLKS1	O	Output pin for transfer clock
I ² C Mode	SDA2	I/O	Inputs and outputs serial data
	SCL2		Inputs and outputs the transfer clock
Multi-master I ² C bus	SDAMM	I/O	Inputs and outputs serial data
	SCLMM		Inputs and outputs the transfer clock
Reference Voltage Input	VREF	I	Applies reference voltage to the A/D converter
A/D Converter	AN0 to AN7 AN00 to AN03 AN24	I	Analog input pins for the A/D converter
	ADTRG		Input pin for an external A/D trigger

I : Input O : Output I/O : Input and output

Table 1.10 Pin Description (64-Pin, 80-Pin and 85-Pin Packages) (Continued)

Classification	Symbol	I/O Type	Function
Timer S	INPC10 to INPC17	I	Input pins for the time measurement function
	OUTC10 to OUTC17	O	Output pins for the waveform generating function
I/O Ports	P00 to P03 P15 to P17 P20 to P27 P30 to P33 P60 to P67 P70 to P77 P80 to P87 P100 to P107	I/O	I/O ports for CMOS. Each port can be programmed for input or output under the control of the direction register. An input port can be set, by program, for a pull-up resistor available or for no pull-up resistor available in 4-bit units
	P90 to P93	I/O	I/O ports having equivalent functions to P0

I : Input O : Output I/O : Input and output

3. Memory

Figure 3.1 is a memory map of the M16C/28 Group (M16C/28, M16C/28B). M16C/28 Group provides 1-Mbyte address space from addresses 00000₁₆ to FFFFF₁₆. The internal ROM is allocated lower addresses beginning with address FFFFF₁₆. For example, 64 Kbytes internal ROM is allocated addresses F0000₁₆ to FFFFF₁₆.

Two 2-Kbyte internal ROM areas, block A and block B, are available in the flash memory version. The blocks are allocated addresses F000₁₆ to FFFF₁₆.

The fixed interrupt vector tables are allocated addresses FFFDC₁₆ to FFFFF₁₆. It stores the starting address of each interrupt routine. See the section on interrupts for details.

The internal RAM is allocated higher addresses beginning with address 00400₁₆. For example, 4-Kbytes internal RAM is allocated addresses 00400₁₆ to 013FF₁₆. Besides storing data, it becomes stacks when the subroutine is called or an interrupt is acknowledged.

SFR, consisting of control registers for peripheral functions such as I/O port, A/D converter, serial I/O, timers is allocated addresses 00000₁₆ to 003FF₁₆. All blank spaces within SFR are reserved and cannot be accessed by users.

The special page vector table is allocated to the addresses FFE00₁₆ to FFFDB₁₆. This vector is used by the JMPS or JSRS instruction. For details, refer to the **M16C/60 and M16C/20 Series Software Manual**.

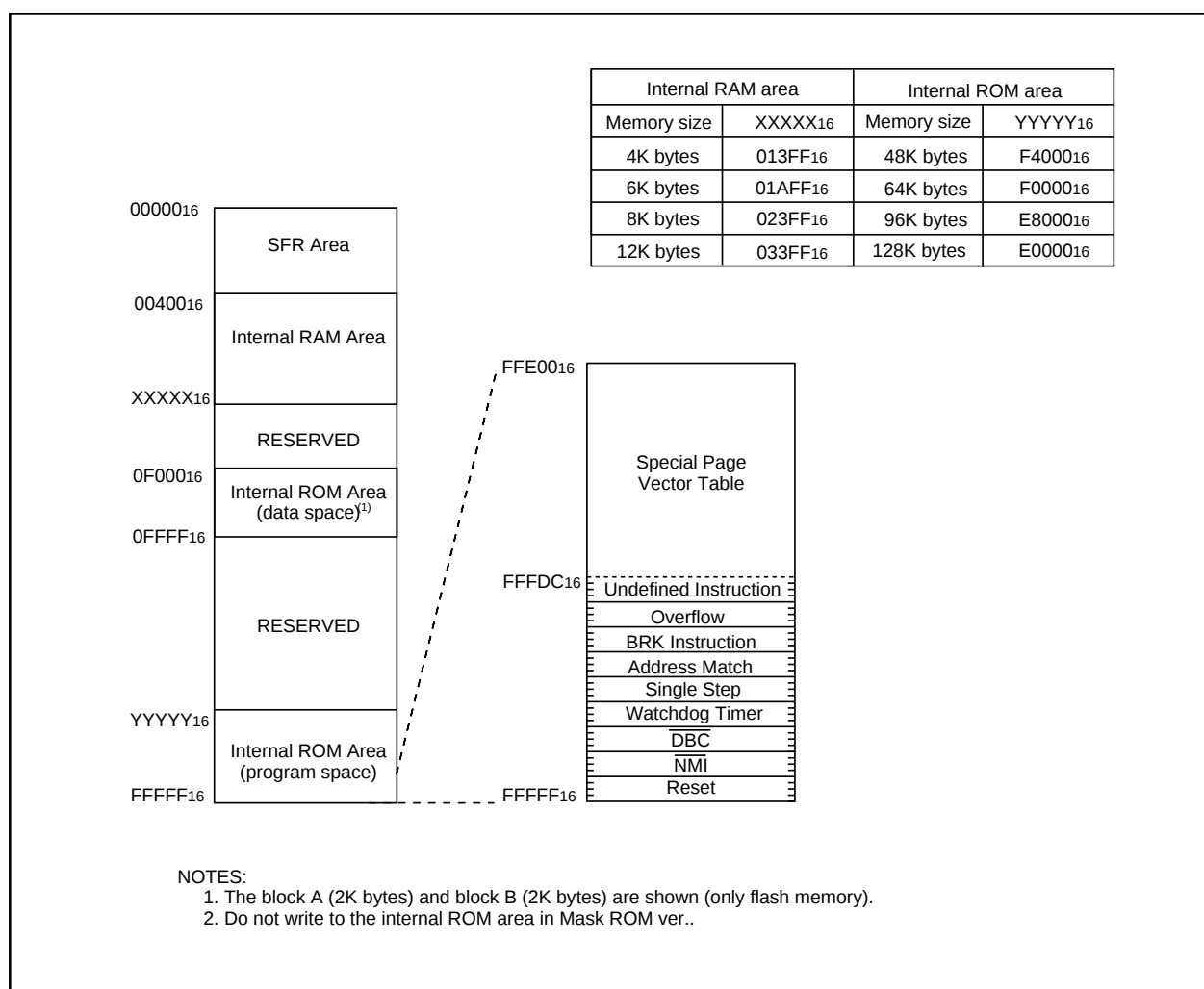


Figure 3.1 Memory Map

Table 4.2 SFR Information(2)⁽¹⁾

Address	Register	Symbol	After Reset
0040 ₁₆			
0041 ₁₆			
0042 ₁₆			
0043 ₁₆			
0044 ₁₆	INT3 interrupt control register	INT3IC	XX00X0002
0045 ₁₆	IC/OC 0 interrupt control register	ICOC0IC	XXXXX0002
0046 ₁₆	IC/OC 1 interrupt control register, I ² C bus interface interrupt control register	ICOC1IC, IICIC	XXXXX0002
0047 ₁₆	IC/OC base timer interrupt control register, SCLSDA interrupt control register	BTIC, SCLDAIC	XXXXX0002
0048 ₁₆	SI/O4 interrupt control register, INT5 interrupt control register	S4IC, INT5IC	XX00X0002
0049 ₁₆	SI/O3 interrupt control register, INT4 interrupt control register	S3IC, INT4IC	XX00X0002
004A ₁₆	UART2 Bus collision detection interrupt control register	BCNIC	XXXXX0002
004B ₁₆	DMA0 interrupt control register	DM0IC	XXXXX0002
004C ₁₆	DMA1 interrupt control register	DM1IC	XXXXX0002
004D ₁₆	Key input interrupt control register	KUPIC	XXXXX0002
004E ₁₆	A/D conversion interrupt control register	ADIC	XXXXX0002
004F ₁₆	UART2 transmit interrupt control register	S2TIC	XXXXX0002
0050 ₁₆	UART2 receive interrupt control register	S2RIC	XXXXX0002
0051 ₁₆	UART0 transmit interrupt control register	S0TIC	XXXXX0002
0052 ₁₆	UART0 receive interrupt control register	S0RIC	XXXXX0002
0053 ₁₆	UART1 transmit interrupt control register	S1TIC	XXXXX0002
0054 ₁₆	UART1 receive interrupt control register	S1RIC	XXXXX0002
0055 ₁₆	Timer A0 interrupt control register	TA0IC	XXXXX0002
0056 ₁₆	Timer A1 interrupt control register	TA1IC	XXXXX0002
0057 ₁₆	Timer A2 interrupt control register	TA2IC	XXXXX0002
0058 ₁₆	Timer A3 interrupt control register	TA3IC	XXXXX0002
0059 ₁₆	Timer A4 interrupt control register	TA4IC	XXXXX0002
005A ₁₆	Timer B0 interrupt control register	TB0IC	XXXXX0002
005B ₁₆	Timer B1 interrupt control register	TB1IC	XXXXX0002
005C ₁₆	Timer B2 interrupt control register	TB2IC	XXXXX0002
005D ₁₆	INT0 interrupt control register	INT0IC	XX00X0002
005E ₁₆	INT1 interrupt control register	INT1IC	XX00X0002
005F ₁₆	INT2 interrupt control register	INT2IC	XX00X0002
0060 ₁₆			
0061 ₁₆			
0062 ₁₆			
0063 ₁₆			
0064 ₁₆			
0065 ₁₆			
0066 ₁₆			
0067 ₁₆			
0068 ₁₆			
0069 ₁₆			
006A ₁₆			
006B ₁₆			
006C ₁₆			
006D ₁₆			
006E ₁₆			
006F ₁₆			
0070 ₁₆			
0071 ₁₆			
0072 ₁₆			
0073 ₁₆			
0074 ₁₆			
0075 ₁₆			
0076 ₁₆			
0077 ₁₆			
0078 ₁₆			
0079 ₁₆			
007A ₁₆			
007B ₁₆			
007C ₁₆			
007D ₁₆			
007E ₁₆			
007F ₁₆			

Note 1: The blank spaces are reserved. No access is allowed.

X : Undefined

Table 4.3 SFR Information(3)(1)

Address	Register	Symbol	After Reset
01B0 ₁₆			
01B1 ₁₆			
01B2 ₁₆			
01B3 ₁₆	Flash memory control register 4 ⁽²⁾	FMR4	010000002
01B4 ₁₆			
01B5 ₁₆	Flash memory control register 1 ⁽²⁾	FMR1	000XX0X2
01B6 ₁₆			
01B7 ₁₆	Flash memory control register 0 ⁽²⁾	FMR0	000000012
01B8 ₁₆			
01B9 ₁₆			
0210 ₁₆	Low-power Consumption Control 0	LPCC0	X00000012
0211 ₁₆			
0212 ₁₆			
0213 ₁₆			
0214 ₁₆			
0215 ₁₆			
0216 ₁₆			
0217 ₁₆			
0218 ₁₆			
0219 ₁₆			
0250 ₁₆			
0251 ₁₆			
0252 ₁₆			
0253 ₁₆			
0254 ₁₆			
0255 ₁₆			
0256 ₁₆			
0257 ₁₆			
0258 ₁₆			
0259 ₁₆			
025A ₁₆			
025B ₁₆			
025C ₁₆	On-chip oscillator control register	ROCR	X00001012
025D ₁₆	Pin assignment control register	PACR	0016
025E ₁₆	Peripheral clock select register	PCLKR	000000112
025F ₁₆	Low-power Consumption Control 1	LPCC1	0016
02E0 ₁₆	I ² C0 data shift register	S00	XX16
02E1 ₁₆			
02E2 ₁₆	I ² C0 address register	S0D0	0016
02E3 ₁₆	I ² C0 control register 0	S1D0	0016
02E4 ₁₆	I ² C0 clock control register	S20	0016
02E5 ₁₆	I ² C0 start/stop condition control register	S2D0	000110102
02E6 ₁₆	I ² C0 control register 1	S3D0	001100002
02E7 ₁₆	I ² C0 control register 2	S4D0	0016
02E8 ₁₆	I ² C0 status register	S10	0001000X2
02E9 ₁₆			
02EA ₁₆			
02FE ₁₆			
02FF ₁₆			

Note 1: The blank spaces are reserved. No access is allowed.

Note 2: This register is included in the flash memory version.

X : Undefined

Table 4.4 SFR Information(4)(1)

Address	Register	Symbol	After Reset
0300 ₁₆ 0301 ₁₆	TM, WG register 0	G1TM0, G1PO0	XX ₁₆ XX ₁₆
0302 ₁₆ 0303 ₁₆	TM, WG register 1	G1TM1, G1PO1	XX ₁₆ XX ₁₆
0304 ₁₆ 0305 ₁₆	TM, WG register 2	G1TM2, G1PO2	XX ₁₆ XX ₁₆
0306 ₁₆ 0307 ₁₆	TM, WG register 3	G1TM3, G1PO3	XX ₁₆ XX ₁₆
0308 ₁₆ 0309 ₁₆	TM, WG register 4	G1TM4, G1PO4	XX ₁₆ XX ₁₆
030A ₁₆ 030B ₁₆	TM, WG register 5	G1TM5, G1PO5	XX ₁₆ XX ₁₆
030C ₁₆ 030D ₁₆	TM, WG register 6	G1TM6, G1PO6	XX ₁₆ XX ₁₆
030E ₁₆ 030F ₁₆	TM, WG register 7	G1TM7, G1PO7	XX ₁₆ XX ₁₆
0310 ₁₆	WG control register 0	G1POCR0	0X00XX002
0311 ₁₆	WG control register 1	G1POCR1	0X00XX002
0312 ₁₆	WG control register 2	G1POCR2	0X00XX002
0313 ₁₆	WG control register 3	G1POCR3	0X00XX002
0314 ₁₆	WG control register 4	G1POCR4	0X00XX002
0315 ₁₆	WG control register 5	G1POCR5	0X00XX002
0316 ₁₆	WG control register 6	G1POCR6	0X00XX002
0317 ₁₆	WG control register 7	G1POCR7	0X00XX002
0318 ₁₆	TM control register 0	G1TMCR0	00 ₁₆
0319 ₁₆	TM control register 1	G1TMCR1	00 ₁₆
031A ₁₆	TM control register 2	G1TMCR2	00 ₁₆
031B ₁₆	TM control register 3	G1TMCR3	00 ₁₆
031C ₁₆	TM control register 4	G1TMCR4	00 ₁₆
031D ₁₆	TM control register 5	G1TMCR5	00 ₁₆
031E ₁₆	TM control register 6	G1TMCR6	00 ₁₆
031F ₁₆	TM control register 7	G1TMCR7	00 ₁₆
0320 ₁₆ 0321 ₁₆	Base timer register	G1BT	XX ₁₆ XX ₁₆
0322 ₁₆	Base timer control register 0	G1BCR0	00 ₁₆
0323 ₁₆	Base timer control register 1	G1BCR1	00 ₁₆
0324 ₁₆	TM prescale register 6	G1TPR6	00 ₁₆
0325 ₁₆	TM prescale register 7	G1TPR7	00 ₁₆
0326 ₁₆	Function enable register	G1FE	00 ₁₆
0327 ₁₆	Function select register	G1FS	00 ₁₆
0328 ₁₆ 0329 ₁₆	Base timer reset register	G1BTRR	XX ₁₆ XX ₁₆
032A ₁₆ 032B ₁₆	Divider register	G1DV	00 ₁₆
032C ₁₆			
032D ₁₆			
032E ₁₆			
032F ₁₆			
0330 ₁₆	Interrupt request register	G1IR	XX ₁₆
0331 ₁₆	Interrupt enable register 0	G1IE0	00 ₁₆
0332 ₁₆	Interrupt enable register 1	G1IE1	00 ₁₆
0333 ₁₆			
0334 ₁₆			
0335 ₁₆			
0336 ₁₆			
0337 ₁₆			
0338 ₁₆			
0339 ₁₆			
033A ₁₆			
033B ₁₆			
033C ₁₆			
033D ₁₆			
033E ₁₆	NMI digital debounce register	NDDR	FF ₁₆
033F ₁₆	P17 digital debounce register	P17DDR	FF ₁₆

Note 1: The blank spaces are reserved. No access is allowed.

X : Undefined

Table 4.7 SFR Information(7)(1)

Address	Register	Symbol	After Reset
03C0 ₁₆ 03C1 ₁₆	A/D register 0	AD0	XX ₁₆ XX ₁₆
03C2 ₁₆ 03C3 ₁₆	A/D register 1	AD1	XX ₁₆ XX ₁₆
03C4 ₁₆ 03C5 ₁₆	A/D register 2	AD2	XX ₁₆ XX ₁₆
03C6 ₁₆ 03C7 ₁₆	A/D register 3	AD3	XX ₁₆ XX ₁₆
03C8 ₁₆ 03C9 ₁₆	A/D register 4	AD4	XX ₁₆ XX ₁₆
03CA ₁₆ 03CB ₁₆	A/D register 5	AD5	XX ₁₆ XX ₁₆
03CC ₁₆ 03CD ₁₆	A/D register 6	AD6	XX ₁₆ XX ₁₆
03CE ₁₆ 03CF ₁₆	A/D register 7	AD7	XX ₁₆ XX ₁₆
03D0 ₁₆			
03D1 ₁₆			
03D2 ₁₆	A/D trigger control register	ADTRGCON	00 ₁₆
03D3 ₁₆	A/D convert status register 0	ADSTAT0	00000X002
03D4 ₁₆	A/D control register 2	ADCON2	00 ₁₆
03D5 ₁₆			
03D6 ₁₆	A/D control register 0	ADCON0	00000XXX2
03D7 ₁₆	A/D control register 1	ADCON1	00 ₁₆
03D8 ₁₆			
03D9 ₁₆			
03DA ₁₆			
03DB ₁₆			
03DC ₁₆			
03DD ₁₆			
03DE ₁₆			
03DF ₁₆			
03E0 ₁₆	Port P0 register	P0	XX ₁₆
03E1 ₁₆	Port P1 register	P1	XX ₁₆
03E2 ₁₆	Port P0 direction register	PD0	00 ₁₆
03E3 ₁₆	Port P1 direction register	PD1	00 ₁₆
03E4 ₁₆	Port P2 register	P2	XX ₁₆
03E5 ₁₆	Port P3 register	P3	XX ₁₆
03E6 ₁₆	Port P2 direction register	PD2	00 ₁₆
03E7 ₁₆	Port P3 direction register	PD3	00 ₁₆
03E8 ₁₆			
03E9 ₁₆			
03EA ₁₆			
03EB ₁₆			
03EC ₁₆	Port P6 register	P6	XX ₁₆
03ED ₁₆	Port P7 register	P7	XX ₁₆
03EE ₁₆	Port P6 direction register	PD6	00 ₁₆
03EF ₁₆	Port P7 direction register	PD7	00 ₁₆
03F0 ₁₆	Port P8 register	P8	XX ₁₆
03F1 ₁₆	Port P9 register	P9	XX ₁₆
03F2 ₁₆	Port P8 direction register	PD8	00 ₁₆
03F3 ₁₆	Port P9 direction register	PD9	000X00002
03F4 ₁₆	Port P10 register	P10	XX ₁₆
03F5 ₁₆			
03F6 ₁₆	Port P10 direction register	PD10	00 ₁₆
03F7 ₁₆			
03F8 ₁₆			
03F9 ₁₆			
03FA ₁₆			
03FB ₁₆			
03FC ₁₆	Pull-up control register 0	PUR0	00 ₁₆
03FD ₁₆	Pull-up control register 1	PUR1	00 ₁₆
03FE ₁₆	Pull-up control register 2	PUR2	00 ₁₆
03FF ₁₆	Port control register	PCR	00 ₁₆

Note 1: The blank spaces are reserved. No access is allowed.

X : Undefined

Appendix 1. Package Dimensions

