Renesas Electronics America Inc - M30281F8HP#U3B Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	M16C/60
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, IEBus, SIO, UART/USART
Peripherals	DMA, POR, PWM, Voltage Detect, WDT
Number of I/O	55
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 13x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30281f8hp-u3b

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1. Overview

The M16C/28 Group (M16C/28 and M16C/28B) MCU are single-chip control MCU, fabricated using high-performance silicon gate CMOS technology with the M16C/60 series CPU core. The M16C/28 Group (M16C/28 and M16C/28B) are housed in 64-pin and 80-pin plastic molded LQFP packages and also in 85-pin plastic molded TFLGA (Thin Fine Pitch Land Grid Array) package. With a 1-Mbyte address space, this MCU combines advanced instruction manipulation capabilities to process complex instructions by less bytes and execute instructions at higher speed. It includes a multiplier and DMAC adequate for office automation, communication devices and other high-speed processing applications.

The M16C/28 has Normal-ver., T-ver., and V-ver.. The M16C/28B has Normal-ver. only.

This hardware manual describes the Normal-ver. only. Please contact Renesas Technology Corp. for T-ver./V-ver. information.

1.1 Applications

Audio, cameras, office equipment, communication equipment, portable equipment, home appliances (inverter solution), motor control, industrial equipment, etc.

Table 1.2 M16C/28 Group (M16C/28, M16C/28) (64-Pin Package)

	Item	Performance
CPU	Number of basic instructions	91 instructions
	Minimum instruction excution time	41.7 ns (f(BCLK) = 24 MHZ, VCC = 4.2 V to 5.5 V) (M16C/28B) 50 ns (f(BCLK) = 20 MHZ, VCC = 3.0V to 5.5V) (M16C/28, M16C/28B) 100 ns (f(BCLK) = 10 MHZ, VCC = 2.7V to 5.5V) (M16C/28, M16C/28B)
	Operation mode	Single chip mode
	Address space	1M bytes
	Memory capacity	See **Table 1.3**
Peripheral Function	I/O Port	Input/Output : 55 lines
	Multifunction timer	TimerA:16 bits x 5 channels, TimerB:16 bits x 3 channels Three-phase Motor Control Timer TimerS (Input Capture/Output Compare) : 16bit base timer x 1 channel (Input/Output x 8 channels)
	Serial I/O	2 channels (UART0, UART1) UART, clock synchronous 1 channel (UART2) UART, clock synchronous, I^2C bus(1), or IEbus(2) 1 channels (SI/O3, SI/O4) Clock synchronous 1 channel (Multi-Master I^2C bus(1))
	A/D converter	10 bits x 13 channels
	DMAC	2 channels
	Watchdog timer	15 bits x 1 (with prescaler)
	Interrupt	24 internal and 8 external sources, 4 software sources, 7 levels
	Clock generation circuit	4 circuits • Main clock(*) • Sub-clock(*) • On-chip oscillator • PLL frequency synthesizer (*) Equipped with a built-in feedback resistor
	Oscillation Stop Detect Function	Main clock oscillation stop, re-oscillation detect function
	Voltage detection circuit	Available
Electrical Characteristics	Power supply voltage	Vcc = 4.2 V to 5.5 V (f(BCLK) = 24 MHz) (M16C/28) Vcc = 3.0 V to 5.5 V (f(BCLK) = 20 MHz) (M16C/28, M16C/28B) Vcc = 2.7 V to 5.5 V (f(BCLK) = 10 MHz) (M16C/28, M16C/28B)
	Power consumption	16 mA (Vcc = 5 V, f(BCLK) = 20 MHz) 25 µA (f(XCIN) = 32 KHz on RAM) 3.0 µA (Vcc = 3 V, f(XCIN) = 32 KHz, in wait mode) 0.7 µA (Vcc = 3 V, in stop mode)
Flash Memory	Program/erase supply voltage	2.7 V to 5.5 V
	Program and erase endurance	100 times (all space) or 1,000 times (Blocks 0 to 5) /10,000 times (Block A, Block B(3))
Operating Ambient Temperature		-20 to 85C°/-40 to 85C°(3)
Package		64-pin plastic mold LQFP

NOTES:
1. I^2C bus is a trademark of Koninklijke Philips Electronics N. V.
2. IEBus is a trademark of NEC Electronics Corporation.
3. Refer to **Table 1.5** to **1.7** for number of program/erase.
4. Use PLL frequency synthesizer to use M16C/28B at f(BCLK) = 24 MHz.

1.3 Block Diagram

Figure 1.1 is a block diagram of the M16C/28 Group (M16C/28, M16C/28B), 80-pin and 85-pin package.
Figure 1.2 is a block diagram of the M16C/28 Group (M16C/28, M16C/28B), 64-pin package.

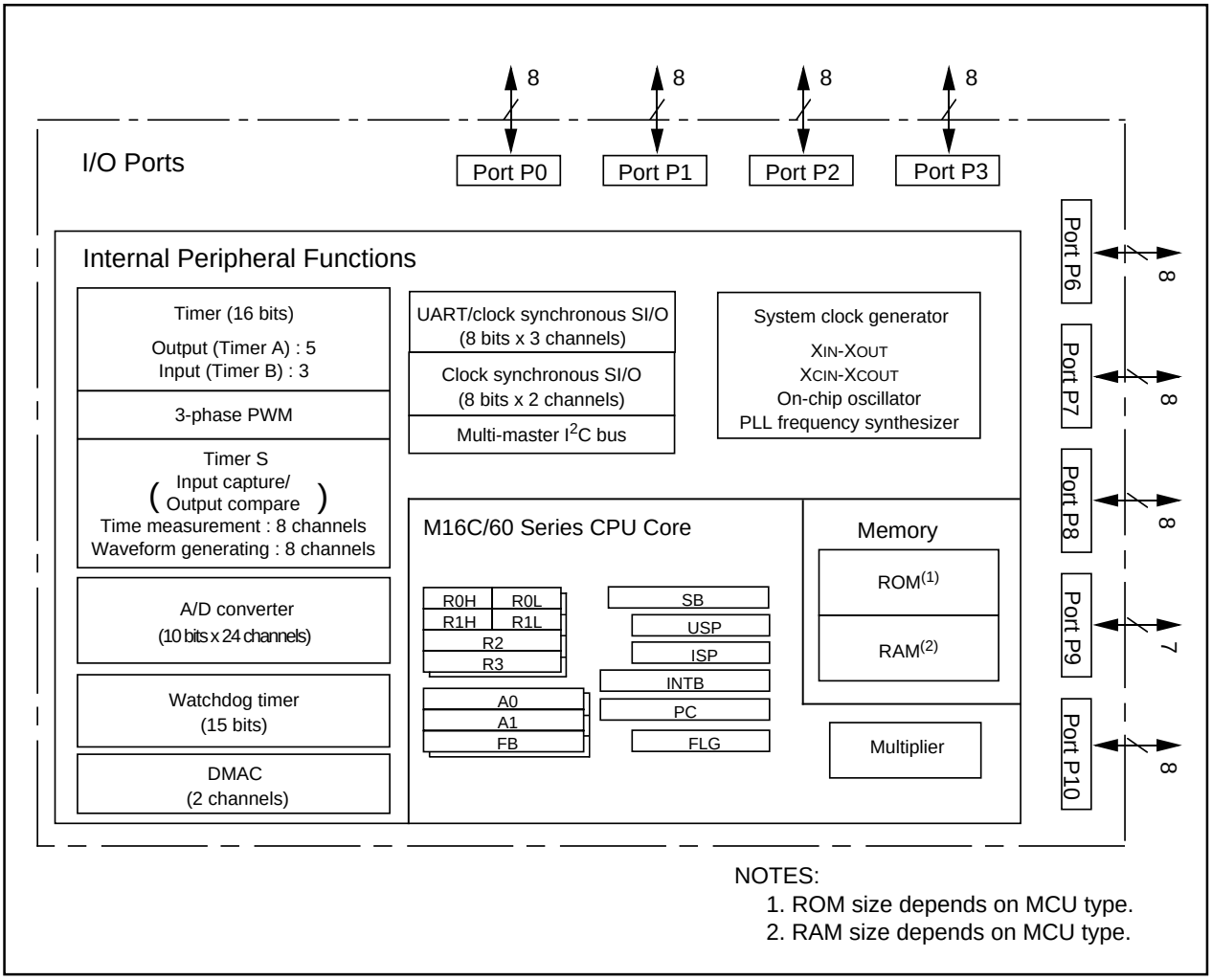


Figure 1.1 M16C/28 Group (M16C/28, M16C/28B), 80-Pin/85-Pin Block Diagram

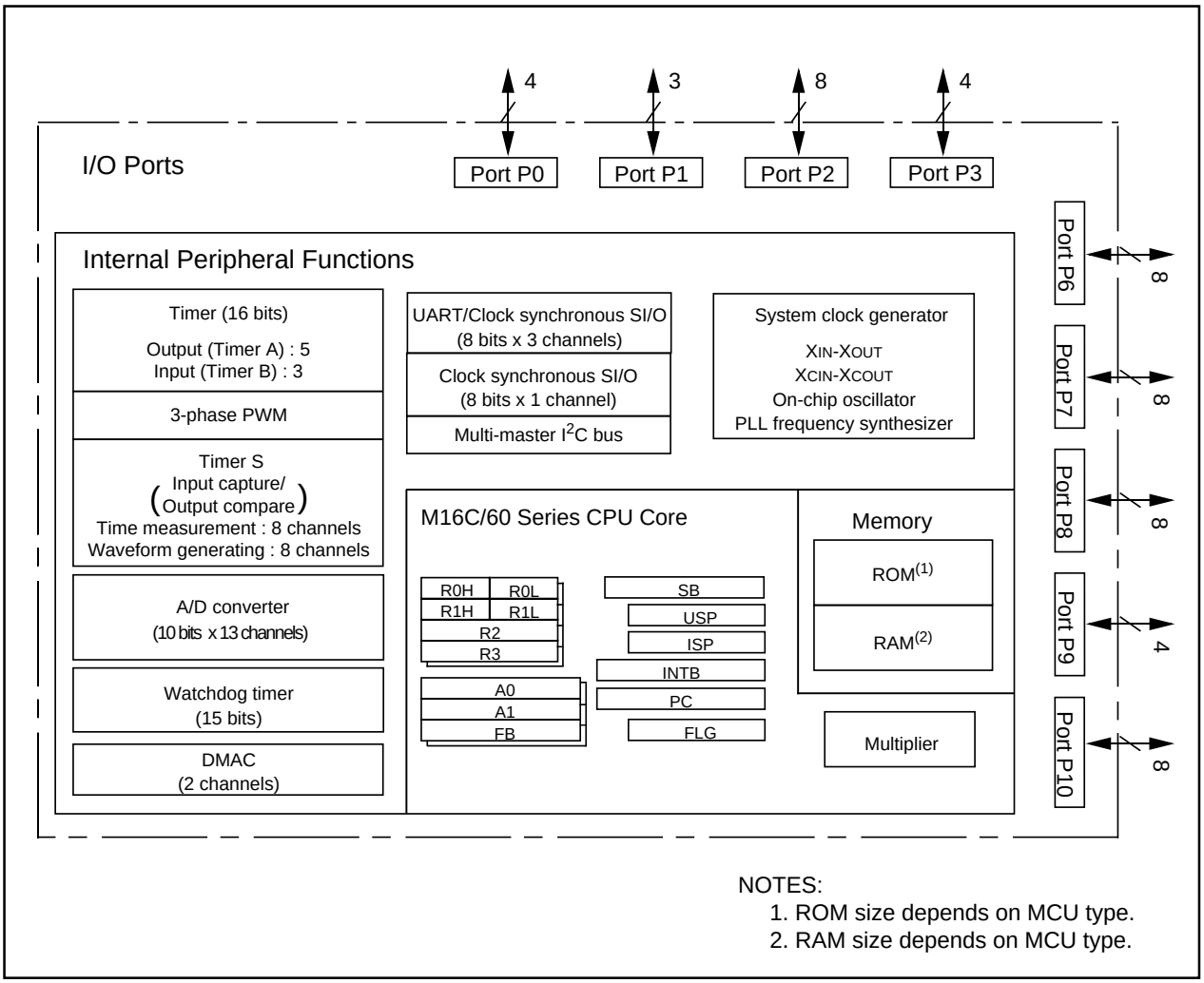
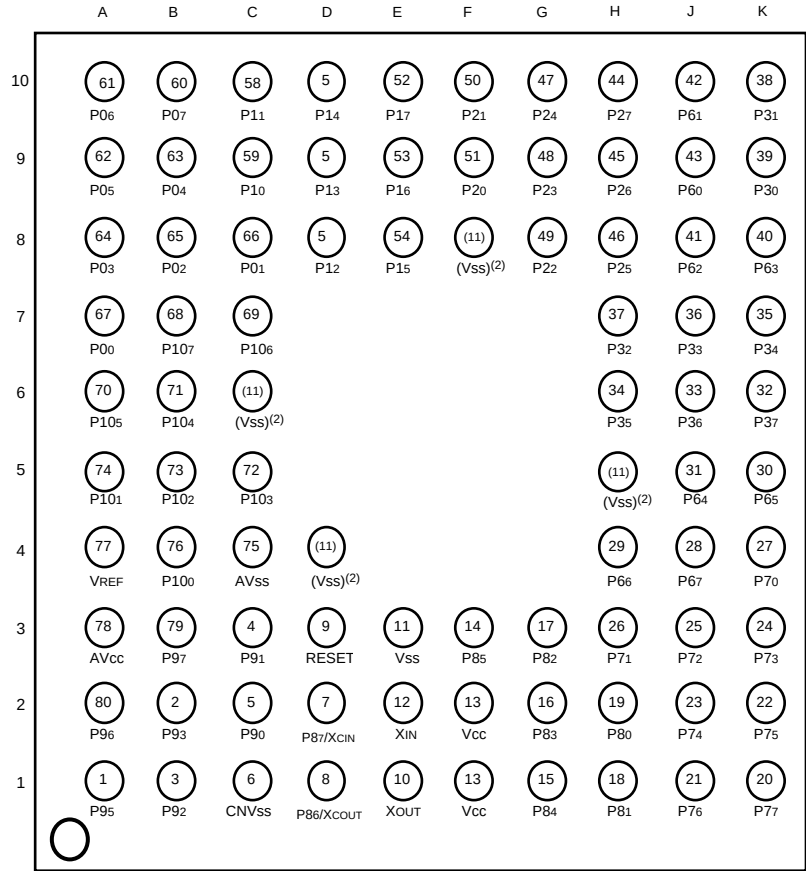


Figure 1.2 M16C/28 Group (M16C/28, M16C/28B), 64-Pin Block Diagram

1.5 Pin Assignment

Figures 1.5 to 1.7 show the pin Assignments (top view).



NOTES :
1. The numbers in each grid (circle) show the pin numbers of the M30280FAHP (80P6Q-A package)
2. Connect grids written as (Vss) to Vss(GND) or leave them open.
3. Set PACR2 to PACR0 bits in the PACR register to "0112" before you input and output it after resetting to each pin. When the PACR register is not set, the input and output function of some pins are disabled.

Package: PTLG0085JB-A(85F0G)

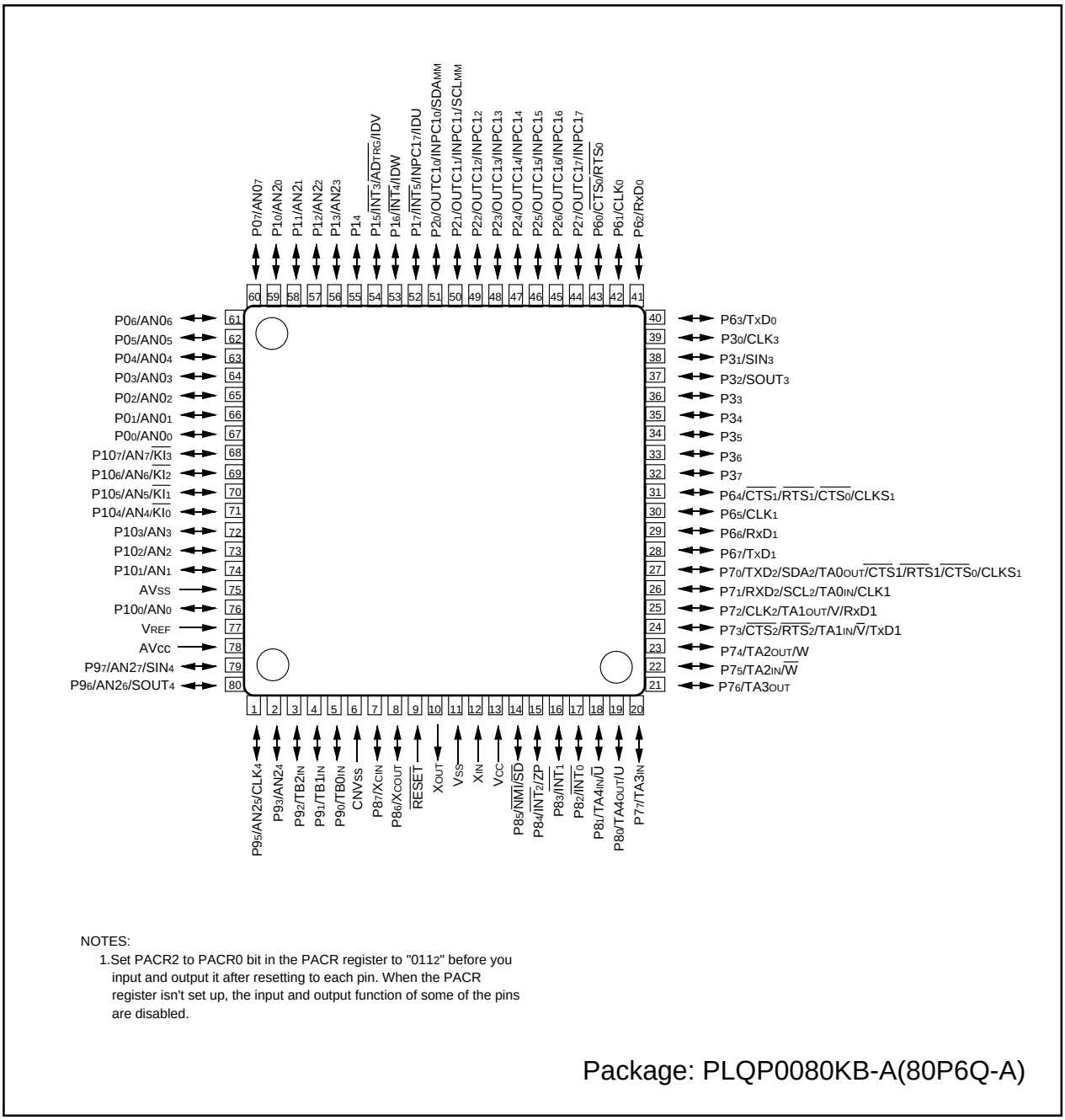
Figure 1.5 Pin Assignment (Top View) of 85-pin Package

Table 1.8 Pin Characteristics for 85-pin Package

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	Timer S Pin	UART Pin	Multi-master I^2C bus Pin	Analog Pin	PLQP0080KB-A Pin Number
A1		$P9_5$				CLK_4		$AN2_5$	1
A2		$P9_6$				$SOUT_4$		$AN2_6$	80
A3	AVcc								78
A4	V_{REF}								77
A5		$P10_1$						AN_1	74
A6		$P10_5$	$\overline{KI}_1$					AN_5	70
A7		$P0_0$						$AN0_0$	67
A8		$P0_3$						$AN0_3$	64
A9		$P0_5$						$AN0_5$	62
A10		$P0_6$						$AN0_6$	61
B1		$P9_2$		TB_{2IN}					3
B2		$P9_3$						$AN2_4$	2
B3		$P9_7$				SIN_4		$AN2_7$	79
B4		$P10_0$						AN_0	76
B5		$P10_2$						AN_2	73
B6		$P10_4$	$\overline{KI}_0$					AN_4	71
B7		$P10_7$	$\overline{KI}_3$					AN_7	68
B8		$P0_2$						$AN0_2$	65
B9		$P0_4$						$AN0_4$	63
B10		$P0_7$						$AN0_7$	60
C1	CNVss								6
C2		$P9_0$		TB_{0IN}					5
C3		$P9_1$		TB_{1IN}					4
C4	AVss								75
C5		$P10_3$						AN_3	72
C6	V_{SS}(1)								(11)
C7		$P10_6$	$\overline{KI}_2$					AN_6	69
C8		$P0_1$						$AN0_1$	66
C9		$P1_0$						$AN2_0$	59
C10		$P1_1$						$AN2_1$	58
D1	X_{COUT}	$P8_6$							8
D2	X_{CIN}	$P8_7$							7
D3	$\overline{RESET}$								9
D4	V_{SS}(1)								(11)
D8		$P1_2$						$AN2_2$	57
D9		$P1_3$						$AN2_3$	56
D10		$P1_4$							55
E1	X_{OUT}								10
E2	X_{IN}								12
E3	Vss								11

Table 1.8 Pin Characteristics for 85-pin Package (continued)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	Timer S Pin	UART Pin	Multi-master I²C bus Pin	Analog Pin	PLQP0080KB-A Pin Number
E8		P15	$\overline{INT_3}$	IDV				$\overline{ADTRG}$	54
E9		P16	$\overline{INT_4}$	IDW					53
E10		P17	$\overline{INT_5}$	IDU	INPC17				52
F1	Vcc								13
F2	Vcc								13
F3		P85	$\overline{NMI}$	$\overline{SD}$					14
F8	Vss(1)								(11)
F9		P20			OUTC10 / INPC10		SDAMM		51
F10		P21			OUTC11 / INPC11		SCLMM		50
G1		P84	$\overline{INT_2}$	ZP					15
G2		P83	$\overline{INT_1}$						16
G3		P82	$\overline{INT_0}$						17
G8		P22			OUTC12 / INPC12				49
G9		P23			OUTC13 / INPC13				48
G10		P24			OUTC14 / INPC14				47
H1		P81		TA4IN / $\overline{U}$					18
H2		P80		TA4OUT / U					19
H3		P71		TA0IN		RXD2 / SCL2 / CLK1			26
H4		P66				RXD1			29
H5	Vss(1)								(11)
H6		P35							34
H7		P32				SOUT3			37
H8		P25			OUTC15 / INPC15				46
H9		P26			OUTC16 / INPC16				45
H10		P27			OUTC17 / INPC17				44
J1		P76		TA3OUT					21
J2		P74		TA2OUT / W					23
J3		P72		TA1OUT / V		CLK2 / RXD1			25
J4		P67				TXD1			28
J5		P64				$\overline{RTS_1}$ / $\overline{CTS_1}$/ $\overline{CTS_0}$ / CLKS1			31
J6		P36							33
J7		P33							36
J8		P62				RXD0			41
J9		P60				$\overline{RTS_0}$ / $\overline{CTS_0}$			43
J10		P61				CLK0			42
K1		P77		TA3IN					20
K2		P75		TA2IN / $\overline{W}$					22
K3		P73		TA1IN / $\overline{V}$		$\overline{CTS_2}$ / $\overline{RTS_2}$ / $\overline{TXD_1}$			24
K4		P70		TA0OUT		TXD2 / SDA2 / $\overline{RTS_1}$ / $\overline{CTS_1}$ / $\overline{CTS_0}$ / $\overline{CLKS_1}$			27
K5		P65				CLK1			30
K6		P37							32
K7		P34							35
K8		P63				TXD0			40
K9		P30				CLK3			39
K10		P31				SIN3			38



NOTES:
1. Set PACR2 to PACR0 bit in the PACR register to "011₂" before you input and output it after resetting to each pin. When the PACR register isn't set up, the input and output function of some of the pins are disabled.

Package: PLQP0080KB-A(80P6Q-A)

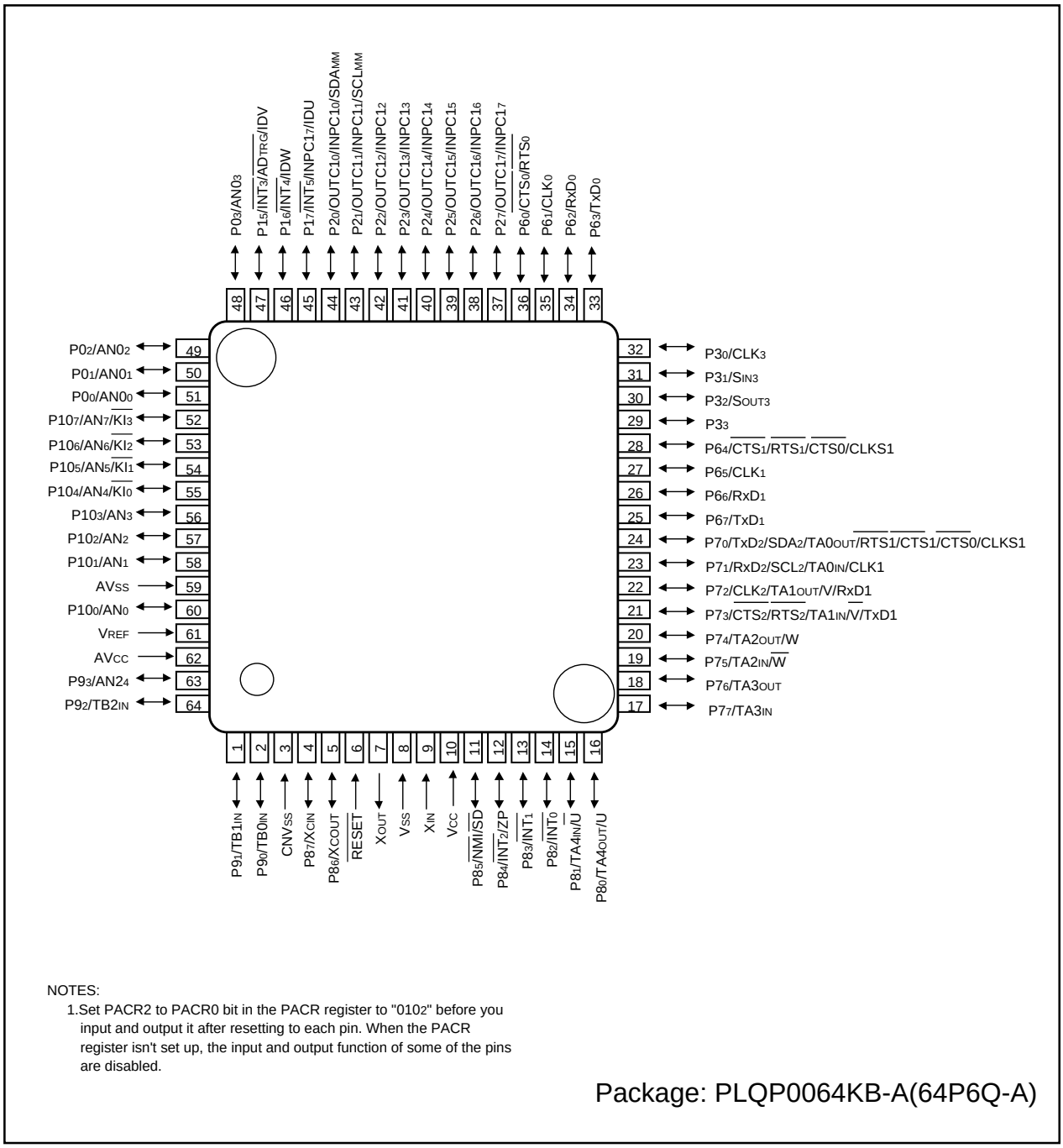
Figure 1.5 Pin Assignment (Top View) of 80-Pin Package

Table 1.9 Pin Characteristics for 80-Pin Package

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	Timer S Pin	UART Pin	Multi-master I^2C bus Pin	Analog Pin
1		$P9_5$				CLK_4		$AN2_5$
2		$P9_3$						$AN2_4$
3		$P9_2$		TB_{2IN}				
4		$P9_1$		TB_{1IN}				
5		$P9_0$		TB_{0IN}				
6	CNVss							
7	X_{CIN}	$P8_7$						
8	X_{COUT}	$P8_6$						
9	$\overline{RESET}$							
10	X_{OUT}							
11	Vss							
12	X_{IN}							
13	Vcc							
14		$P8_5$	$\overline{NMI}$	$\overline{SD}$				
15		$P8_4$	$\overline{INT_2}$	ZP				
16		$P8_3$	$\overline{INT_1}$					
17		$P8_2$	$\overline{INT_0}$					
18		$P8_1$		TA_{4IN} / $\overline{U}$				
19		$P8_0$		TA_{4OUT} / U				
20		$P7_7$		TA_{3IN}				
21		$P7_6$		TA_{3OUT}				
22		$P7_5$		TA_{2IN} / $\overline{W}$				
23		$P7_4$		TA_{2OUT} / W				
24		$P7_3$		TA_{1IN} / $\overline{V}$		$\overline{CTS_2}$ / $\overline{RTS_2}$ / TxD_1		
25		$P7_2$		TA_{1OUT} / V		CLK_2 / RxD_1		
26		$P7_1$		TA_{0IN}		RxD_2 / SCL_2 / CLK_1		
27		$P7_0$		TA_{0OUT}		TxD_2 / SDA_2 / $\overline{RTS_1}$ / $\overline{CTS_1}$ / $\overline{CTS_0}$ / $CLKS_1$		
28		$P6_7$				TxD_1		
29		$P6_6$				RxD_1		
30		$P6_5$				CLK_1		
31		$P6_4$				RTS_1 / $\overline{CTS_1}$/ $\overline{CTS_0}$ / $CLKS_1$		
32		$P3_7$						
33		$P3_6$						
34		$P3_5$						
35		$P3_4$						
36		$P3_3$						
37		$P3_2$				$SOUT_3$		
38		$P3_1$				SIN_3		
39		$P3_0$				CLK_3		
40		$P6_3$				TxD_0		

Table 1.9 Pin Characteristics for 80-Pin Package (Continued)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	Timer S Pin	UART Pin	Multi-master I^2C bus Pin	Analog Pin
41		$P6_2$				RxD_0		
42		$P6_1$				CLK_0		
43		$P6_0$				$\overline{RTS_0}$ / $\overline{CTS_0}$		
44		$P2_7$			$OUTC1_7$ / $INPC1_7$			
45		$P2_6$			$OUTC1_6$ / $INPC1_6$			
46		$P2_5$			$OUTC1_5$ / $INPC1_5$			
47		$P2_4$			$OUTC1_4$ / $INPC1_4$			
48		$P2_3$			$OUTC1_3$ / $INPC1_3$			
49		$P2_2$			$OUTC1_2$ / $INPC1_2$			
50		$P2_1$			$OUTC1_1$ / $INPC1_1$		SCL_{MM}	
51		$P2_0$			$OUTC1_0$ / $INPC1_0$		SDA_{MM}	
52		$P1_7$	$\overline{INT_5}$	IDU	$INPC1_7$			
53		$P1_6$	$\overline{INT_4}$	IDW				
54		$P1_5$	$\overline{INT_3}$	IDV				$\overline{ADTRG}$
55		$P1_4$						
56		$P1_3$						$AN2_3$
57		$P1_2$						$AN2_2$
58		$P1_1$						$AN2_1$
59		$P1_0$						$AN2_0$
60		$P0_7$						$AN0_7$
61		$P0_6$						$AN0_6$
62		$P0_5$						$AN0_5$
63		$P0_4$						$AN0_4$
64		$P0_3$						$AN0_3$
65		$P0_2$						$AN0_2$
66		$P0_1$						$AN0_1$
67		$P0_0$						$AN0_0$
68		$P10_7$	$\overline{KI_3}$					AN_7
69		$P10_6$	$\overline{KI_2}$					AN_6
70		$P10_5$	$\overline{KI_1}$					AN_5
71		$P10_4$	$\overline{KI_0}$					AN_4
72		$P10_3$						AN_3
73		$P10_2$						AN_2
74		$P10_1$						AN_1
75	AVss							
76		$P10_0$						AN_0
77	V_{REF}							
78	AVcc							
79		$P9_7$				SIN_4		$AN2_7$
80		$P9_6$				$SOUT_4$		$AN2_6$



NOTES:
1. Set PACR2 to PACR0 bit in the PACR register to "010₂" before you input and output it after resetting to each pin. When the PACR register isn't set up, the input and output function of some of the pins are disabled.

Package: PLQP0064KB-A(64P6Q-A)

Figure 1.6 Pin Assignment (Top View) of 64-Pin Package

1.6 Pin Description

Table 1.10 Pin Description (64-Pin, 80-Pin and 85-Pin Packages)

Classification	Symbol	I/O Type	Function
Power Supply	VCC, VSS	I	Apply 2.7 to 5.5V to the Vcc pin. Apply 0V to the Vss pin.
Analog Power Supply	AVCC AVSS	I	Supplies power to the A/D converter. Connect the AVCC pin to VCC and the AVSS pin to VSS.
Reset Input	$\overline{\text{RESET}}$	I	The MCU is in a reset state when "L" is applied to the $\overline{\text{RESET}}$ pin
CNVSS	CNVSS	I	Connect the CNVSS pin to VSS.
Main Clock Input	XIN	I	I/O pins for the main clock oscillation circuit. Connect a ceramic resonator or crystal oscillator between XIN and XOUT. To apply external clock, apply it to XIN and leave XOUT open. If XIN is not used (for external oscillator or external clock) connect XIN pin to VCC and leave XOUT open.
Main Clock Output	XOUT	O	
Sub Clock Input	XCIN	I	I/O pins for the sub clock oscillation circuit. Connect a crystal oscillator between XCIN and XCOUT.
Sub Clock Output	XCOUT	O	
$\overline{\text{INT}}$ Interrupt Input	$\overline{\text{INT0}}$ to $\overline{\text{INT5}}$	I	Input pins for the $\overline{\text{INT}}$ interrupt. $\overline{\text{INT2}}$ can be used for Timer A Z-phase function.
$\overline{\text{NMI}}$ Interrupt Input	$\overline{\text{NMI}}$	I	Input pin for the $\overline{\text{NMI}}$ interrupt. $\overline{\text{NMI}}$ cannot be used as I/O port while the three-phase motor control is enabled. Apply a stable "H" to $\overline{\text{NMI}}$ after setting it's direction register to "0" when the three-phase motor control is enabled.
Key Input Interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	Input pins for the key input interrupt
Timer A	TA0OUT to TA4OUT	I/O	I/O pins for the timer A0 to A4
	TA0IN to TA4IN	I	Input pins for the timer A0 to A4
	ZP	I	Input pin for Z-phase
Timer B	TB0IN to TB2IN	I	Input pins for the timer B0 to B2
Three-phase Motor Control Timer Output	U, $\overline{\text{U}}$, V, $\overline{\text{V}}$, W, $\overline{\text{W}}$	O	Output pins for the three-phase motor control timer
	IDU, IDW, IDV, $\overline{\text{SD}}$	I/O	Input and output pins for the three-phase motor control timer
Serial I/O	$\overline{\text{CTS0}}$ to $\overline{\text{CTS2}}$	I	Input pins for data transmission control
	$\overline{\text{RTS0}}$ to $\overline{\text{RTS2}}$	O	Output pins for data reception control
	CLK0 to CLK3	I/O	Inputs and outputs the transfer clock
	RxD0 to RxD2	I	Inputs serial data
	TxD0 to TxD2	O	Outputs serial data
	CLKS1	O	Output pin for transfer clock
I^2C Mode	SDA2	I/O	Inputs and outputs serial data
	SCL2		Inputs and outputs the transfer clock
Multi-master I^2C bus	SDAMM	I/O	Inputs and outputs serial data
	SCLMM		Inputs and outputs the transfer clock
Reference Voltage Input	VREF	I	Applies reference voltage to the A/D converter
A/D Converter	AN0 to AN7 AN00 to AN03 AN24	I	Analog input pins for the A/D converter
	$\overline{\text{ADTRG}}$		Input pin for an external A/D trigger

I : Input O : Output I/O : Input and output

Table 1.10 Pin Description (64-Pin, 80-Pin and 85-Pin Packages) (Continued)

Classification	Symbol	I/O Type	Function
Timer S	INPC10 to INPC17	I	Input pins for the time measurement function
	OUTC10 to OUTC17	O	Output pins for the waveform generating function
I/O Ports	P00 to P03 P15 to P17 P20 to P27 P30 to P33 P60 to P67 P70 to P77 P80 to P87 P100 to P107	I/O	I/O ports for CMOS. Each port can be programmed for input or output under the control of the direction register. An input port can be set, by program, for a pull-up resistor available or for no pull-up resister available in 4-bit units
	P90 to P93	I/O	I/O ports having equivalent functions to P0

I : Input O : Output I/O : Input and output

Table 1.10 Pin Description (80-Pin and 85-Pin Packages only) (Continued)

Classification	Symbol	I/O Type	Function
Serial I/O	CLK4	I/O	Inputs and outputs the transfer clock
	SIN4	I	Inputs serial data
	SOUT4	O	Outputs serial data
A/D Converter	AN04 to AN07 AN20 to AN23 AN25 to AN27	I	Analog input pins for the A/D converter
I/O Ports	P04 to P07 P10 to P14 P34 to P37	I/O	I/O ports for CMOS. Each port can be programmed for input or output under the control of the direction register. An input port can be set, by program, for a pull-up resistor available or for no pull-up resister available in 4-bit units
	P95 to P97	I/O	I/O ports having equivalent functions to P0

I : Input O : Output I/O : Input and output

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers. The register bank is comprised of 7 registers (R0, R1, R2, R3, A0, A1 and FB) out of 13 CPU registers. Two sets of register banks are provided.

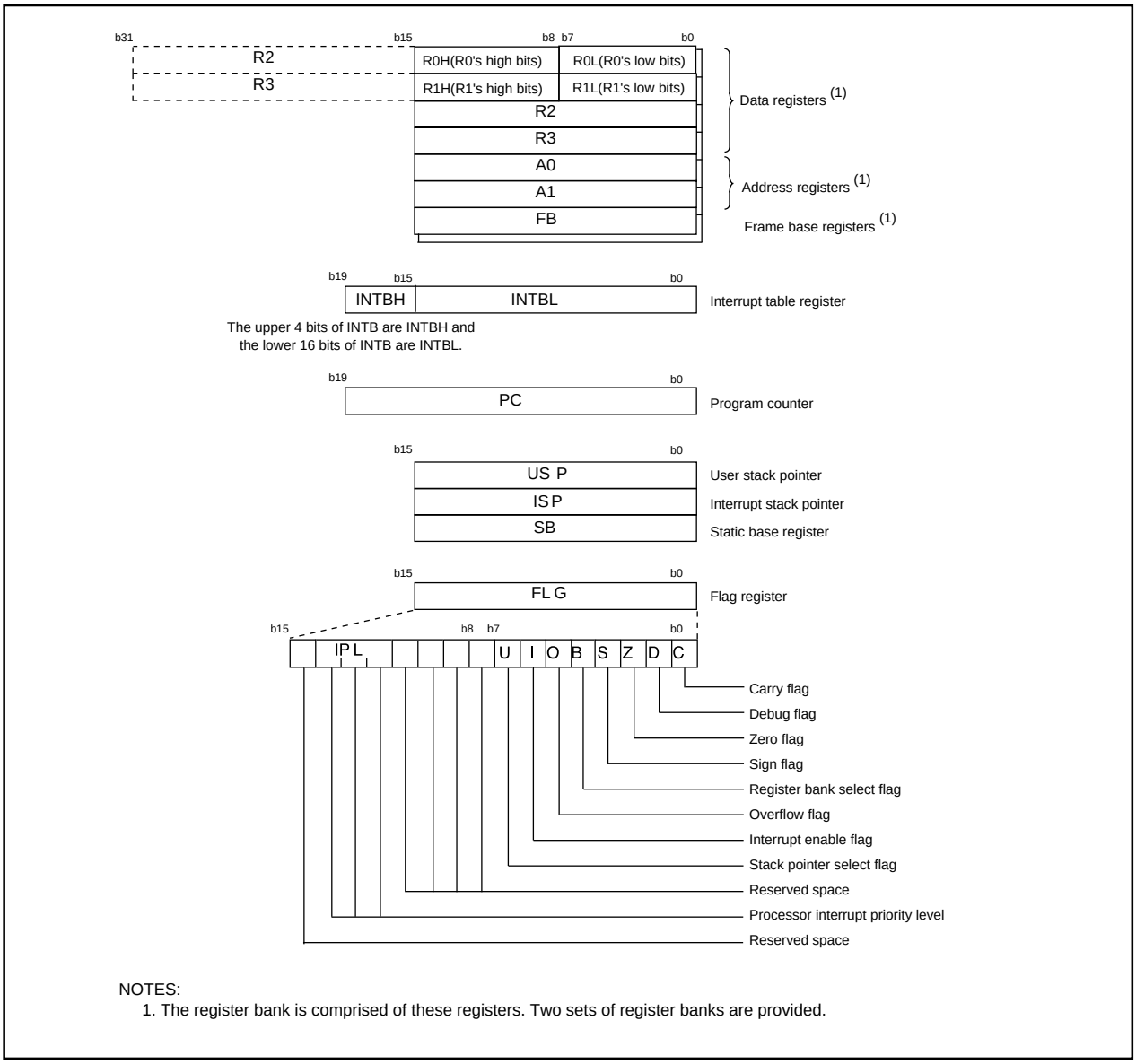


Figure 2.1 Central Processing Unit Register

2.1 Data Registers (R0, R1, R2 and R3)

The R0, R1, R2 and R3 registers are 16 bit registers for transfer and arithmetic/logic operations.

The R0 and R1 registers can be split into high-order bits(R0H, R1H) and low-order bits (R0L, R1L) to be used seperately as 8-bit data registers. Conversely, R2 and R0 can be combined with R2 to be used as a 32-bit data register (R2R0). The same applies to R1 and R2.

2.2 Address Registers (A0 and A1)

The register A0 consists of 16 bits, and is used for address register indirect addressing and address register relative addressing. They also are used for transfers and arithmetic/logic operations. A1 is the same as A0. In some instructions, registers A1 and A0 can be combined for use as a 32-bit address register (A1A0).

4. Special Function Register (SFR)

SFR (Special Function Register) is the control register of peripheral functions. **Tables 4.1** to **4.7** list the SFR information.

Table 4.1 SFR Information(1)[1]

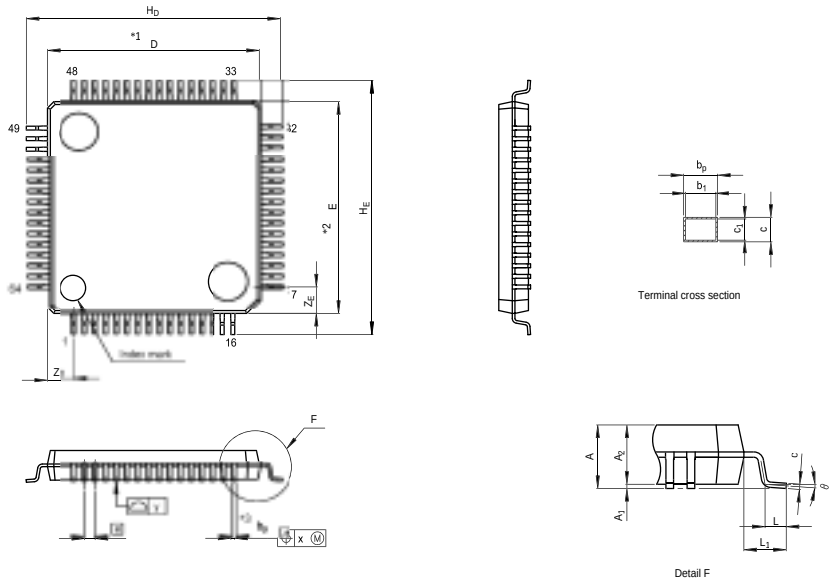
Address	Register	Symbol	After Reset
0000₁₆			
0001₁₆			
0002₁₆			
0003₁₆			
0004₁₆	Processor mode register 0	PM0	00₁₆
0005₁₆	Processor mode register 1	PM1	00001000₂
0006₁₆	System clock control register 0	CM0	01001000₂
0007₁₆	System clock control register 1	CM1	00100000₂
0008₁₆			
0009₁₆	Address match interrupt enable register	AIER	XXXXXX00₂
000A₁₆	Protect register	PRCR	XX000000₂
000B₁₆			
000C₁₆	Oscillation stop detection register [2]	CM2	0X000010₂
000D₁₆			
000E₁₆	Watchdog timer start register	WDTS	XX₁₆
000F₁₆	Watchdog timer control register	WDC	00XXXXXX₂
0010₁₆	Address match interrupt register 0	RMAD0	00₁₆
0011₁₆			00₁₆
0012₁₆			X0₁₆
0013₁₆			
0014₁₆	Address match interrupt register 1	RMAD1	00₁₆
0015₁₆			00₁₆
0016₁₆			X0₁₆
0017₁₆			
0018₁₆			
0019₁₆	Voltage detection register 1 [3]	VCR1	00001000₂
001A₁₆	Voltage detection register 2 [3]	VCR2	00₁₆
001B₁₆			
001C₁₆	PLL control register 0	PLC0	0001X010₂
001D₁₆			
001E₁₆	Processor mode register 2	PM2	XXX00000₂
001F₁₆	Low voltage detection interrupt register	D4INT	00₁₆
0020₁₆	DMA0 source pointer	SAR0	XX₁₆
0021₁₆			XX₁₆
0022₁₆			XX₁₆
0023₁₆			
0024₁₆	DMA0 destination pointer	DAR0	XX₁₆
0025₁₆			XX₁₆
0026₁₆			XX₁₆
0027₁₆			
0028₁₆	DMA0 transfer counter	TCR0	XX₁₆
0029₁₆			XX₁₆
002A₁₆			
002B₁₆			
002C₁₆	DMA0 control register	DM0CON	00000X00₂
002D₁₆			
002E₁₆			
002F₁₆			
0030₁₆	DMA1 source pointer	SAR1	XX₁₆
0031₁₆			XX₁₆
0032₁₆			XX₁₆
0033₁₆			
0034₁₆	DMA1 destination pointer	DAR1	XX₁₆
0035₁₆			XX₁₆
0036₁₆			XX₁₆
0037₁₆			
0038₁₆	DMA1 transfer counter	TCR1	XX₁₆
0039₁₆			XX₁₆
003A₁₆			
003B₁₆			
003C₁₆	DMA1 control register	DM1CON	00000X00₂
003D₁₆			
003E₁₆			
003F₁₆			

NOTES:
1. The blank spaces are reserved. No access is allowed.
2. The CM20, CM21, and CM27 bits do not change at oscillation stop detection reset.
3. This register does not change at software reset, watchdog timer reset and oscillation stop detection reset.

X : Undefined

Appendix 1. Package Dimensions

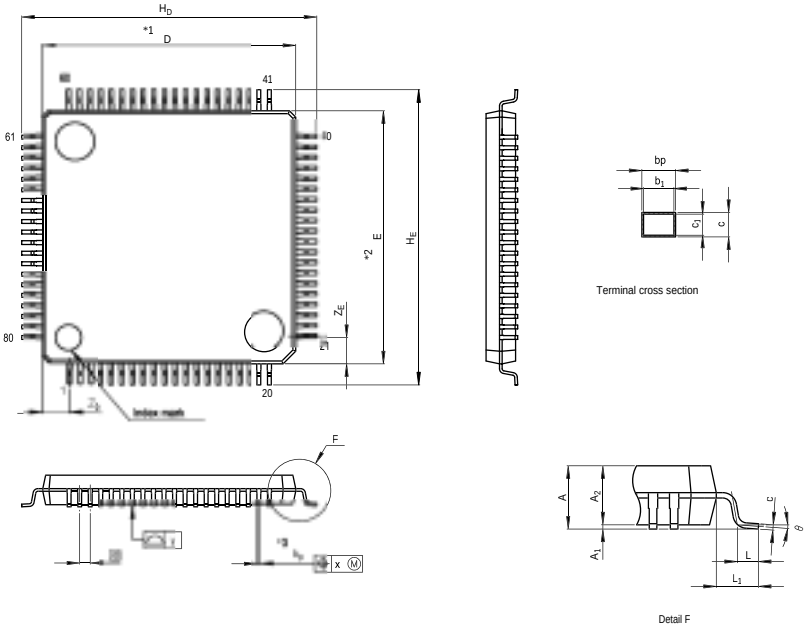
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP64-10x10-0.50	PLQP0064KB-A	64P6Q-A / FP-64K / FP-64KV	0.3g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP80-12x12-0.50	PLQP0080KB-A	80P6Q-A	0.5g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	11.9	12.0	12.1
E	11.9	12.0	12.1
A_2	—	1.4	—
H_D	13.8	14.0	14.2
H_E	13.8	14.0	14.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	10°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.3	0.5	0.7
L_1	—	1.0	—

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Rev.	Date	Description	
		Page	Summary
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