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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | - |
| Core Size | - |
| Speed | - |
| Connectivity | - |
| Peripherals | - |
| Number of I/O | - |
| Program Memory Size | - |
| Program Memory Type | - |
| EEPROM Size | - |
| RAM Size | - |
| Voltage - Supply (Vcc/Vdd) | - |
| Data Converters | - |
| Oscillator Type | - |
| Operating Temperature | - |
| Mounting Type | - |
| Package / Case | - |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/m30281f8hp |

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## 1.2 Performance Overview

**Table 1.1** and **1.2** outline performance overview of the M16C/28 Group (M16C/28, M16C/28B).

**Table 1.1 M16C/28 Group (M16C/28, M16C/28) Performance (80/85-Pin Package)**

| | Item | Performance |
|---|---|---|
| CPU | Number of basic instructions | 91 instructions |
| | Minimum instruction excution time | 41.7 ns (f(BCLK) = 24 MHz, Vcc = 4.2 V to 5.5 V) (M16C/28B)<br>50 ns (f(BCLK) = 20 MHz, Vcc = 3.0 V to 5.5 V) (M16C/28, M16C/28B)<br>100 ns (f(BCLK) = 10 MHz, Vcc= 2.7 V to 5.5 V) (M16C/28, M16C/28B) |
| | Operation mode | Single chip mode |
| | Address space | 1M bytes |
| | Memory capacity | See **Table 1.3** |
| Peripheral Function | I/O port | Input/Output : 71 lines |
| | Multifunction timer | TimerA:16 bits x 5 channels, TimerB:16 bits x 3 channels<br>Three-phase Motor Control Timer<br>TimerS (Input Capture/Output Compare)<br>: 16bit base timer x 1 channel (Input/Output x 8 channels) |
| | Serial I/O | 2 channels (UART0, UART1)<br>UART, clock synchronous<br>1 channel (UART2)<br>UART, clock synchronous, $I^2C$ bus(1), or IEbus(2)<br>2 channels (SI/O3, SI/O4)<br>Clock synchronous<br>1 channel (Multi-Master $I^2C$ bus(1)) |
| | A/D converter | 10 bits x 24 channels |
| | DMAC | 2 channels |
| | Watchdog timer | 15 bits x 1 (with prescaler) |
| | Interrupt | 25 internal and 8 external sources, 4 software sources, 7 levels |
| | Clock generation circuit | 4 circuits<br>• Main clock (*)<br>• Sub-clock (*)<br>• On-chip oscillator<br>• PLL frequency synthesizer<br>(*) Equipped with a built-in feedback resistor |
| | Oscillation Stop Detect Function | Main clock oscillation stop, re-oscillation detect function |
| | Voltage detection circuit | Available |
| Electrical Characteristics | Power supply voltage | Vcc = 4.2 V to 5.5 V (f(BCLK) = 24 MHz) (M16C/28B)<br>Vcc = 3.0 V to 5.5 V (f(BCLK) = 20 MHz) (M16C/28, M16C/28B)<br>Vcc = 2.7 V to 5.5 V (f(BCLK) = 10 MHz) (M16C/28, M16C/28B) |
| | Power consumption | 16 mA (Vcc = 5V, f(BCLK) = 20 MHz)<br>25 µA (f(XCIN) = 32 KHz on RAM)<br>3.0 µA (Vcc = 3V, f(XCIN) = 32 KHz, in wait mode)<br>0.7 µA (Vcc = 3V, in stop mode) |
| Flash Memory | Program/erase supply voltage | 2.7 V to 5.5 V |
| | Program and erase endurance | 100 times (all space) or 1,000 times (Blocks 0 to 5)<br>/10,000 times (Block A, Block B(3)) |
| Operating Ambient Temperature | | -20 to 85°C/-40 to 85°C(3) |
| Package | | 80-pin plastic mold LQFP, 85-pin plastic mold TFLGA |

NOTES:
1. $I^2C$ bus is a trademark of Koninklijke Philips Electronics N. V.
2. IEBus is a trademark of NEC Electronics Corporation.
3. Refer to **Table 1.5** to **1.7** for number of program/erase.
4. Use PLL frequency synthesizer to use M16C/28B at f(BCLK) = 24 MHz.

**Table 1.2 M16C/28 Group (M16C/28, M16C/28) (64-Pin Package)**

| | Item | Performance |
|---|---|---|
| CPU | Number of basic instructions | 91 instructions |
| | Minimum instruction excution time | 41.7 ns (f(BCLK) = 24 MHZ, VCC = 4.2 V to 5.5 V) (M16C/28B)<br>50 ns (f(BCLK) = 20 MHZ, VCC = 3.0V to 5.5V) (M16C/28, M16C/28B)<br>100 ns (f(BCLK) = 10 MHZ, VCC = 2.7V to 5.5V) (M16C/28, M16C/28B) |
| | Operation mode | Single chip mode |
| | Address space | 1M bytes |
| | Memory capacity | See **Table 1.3** |
| Peripheral Function | I/O Port | Input/Output : 55 lines |
| | Multifunction timer | TimerA:16 bits x 5 channels, TimerB:16 bits x 3 channels<br>Three-phase Motor Control Timer<br>TimerS (Input Capture/Output Compare)<br>: 16bit base timer x 1 channel (Input/Output x 8 channels ) |
| | Serial I/O | 2 channels (UART0, UART1)<br>UART, clock synchronous<br>1 channel (UART2)<br>UART, clock synchronous, $I^2C$ bus(1), or IEbus(2)<br>1 channels (SI/O3, SI/O4)<br>Clock synchronous<br>1 channel (Multi-Master $I^2C$ bus(1)) |
| | A/D converter | 10 bits x 13 channels |
| | DMAC | 2 channels |
| | Watchdog timer | 15 bits x 1 (with prescaler) |
| | Interrupt | 24 internal and 8 external sources, 4 software sources, 7 levels |
| | Clock generation circuit | 4 circuits<br>• Main clock(*)<br>• Sub-clock(*)<br>• On-chip oscillator<br>• PLL frequency synthesizer<br>(*) Equipped with a built-in feedback resistor |
| | Oscillation Stop Detect Function | Main clock oscillation stop, re-oscillation detect function |
| | Voltage detection circuit | Available |
| Electrical Characteristics | Power supply voltage | Vcc = 4.2 V to 5.5 V (f(BCLK) = 24 MHz) (M16C/28)<br>Vcc = 3.0 V to 5.5 V (f(BCLK) = 20 MHz) (M16C/28, M16C/28B)<br>Vcc = 2.7 V to 5.5 V (f(BCLK) = 10 MHz) (M16C/28, M16C/28B) |
| | Power consumption | 16 mA (Vcc = 5 V, f(BCLK) = 20 MHz)<br>25 µA (f(XCIN) = 32 KHz on RAM)<br>3.0 µA (Vcc = 3 V, f(XCIN) = 32 KHz, in wait mode)<br>0.7 µA (Vcc = 3 V, in stop mode) |
| Flash Memory | Program/erase supply voltage | 2.7 V to 5.5 V |
| | Program and erase endurance | 100 times (all space) or 1,000 times (Blocks 0 to 5)<br>/10,000 times (Block A, Block B(3)) |
| Operating Ambient Temperature | | -20 to 85C°/-40 to 85C°(3) |
| Package | | 64-pin plastic mold LQFP |

NOTES:
1. $I^2C$ bus is a trademark of Koninklijke Philips Electronics N. V.
2. IEBus is a trademark of NEC Electronics Corporation.
3. Refer to **Table 1.5** to **1.7** for number of program/erase.
4. Use PLL frequency synthesizer to use M16C/28B at f(BCLK) = 24 MHz.

## 1.3 Block Diagram

**Figure 1.1** is a block diagram of the M16C/28 Group (M16C/28, M16C/28B), 80-pin and 85-pin package.
**Figure 1.2** is a block diagram of the M16C/28 Group (M16C/28, M16C/28B), 64-pin package.

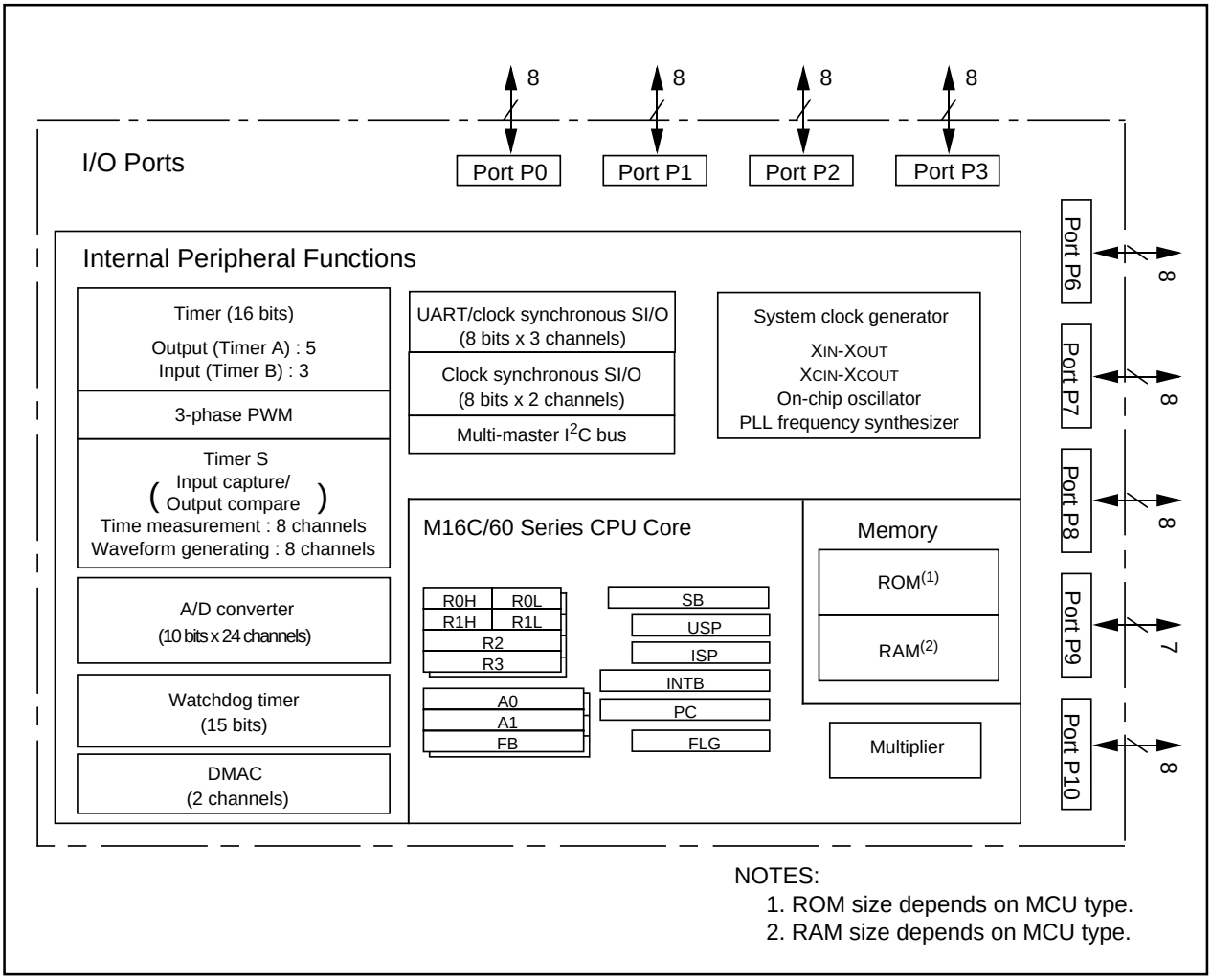



**Figure 1.1 M16C/28 Group (M16C/28, M16C/28B), 80-Pin/85-Pin Block Diagram**

## 1.4 Product Information

**Tables 1.3** and **1.4** list the M16C/28 Group product information and **Figure 1.3** shows the product numbering system. The specifications are partially different between normal-ver.and T/ V-ver..

**Table 1.3 M16C/28 Product List -Normal-ver.** **As of September, 2006**

| Type Number | ROM Capacity | RAM Capacity | Package Type | Remarks | Product Code |
|---|---|---|---|---|---|
| M30280F6WG (N) | 48 K + 4 K | 4 K | PTLG0085JB-A (85F0G) | Flash Memory | U3, U5, U7, U9 |
| M30280F8WG (N) | 64 K + 4 K | 4 K | | | |
| M30280FAWG (N) | 96 K + 4 K | 8 K | | | |
| M30280F6HP (N) | 48 K + 4 K | 4 K | PLQP0080KB-A (80P6Q-A) | | |
| M30280F8HP (N) | 64 K + 4 K | 4 K | | | |
| M30280FAHP (N) | 96 K + 4 K | 8 K | | | |
| M30280FCHP (N) | 128 K + 4 K | 12 K | | | |
| M30281F6HP (N) | 48 K + 4 K | 4 K | PLQP0064KB-A (64P6Q-A) | | |
| M30281F8HP (N) | 64 K + 4 K | 4 K | | | |
| M30281FAHP (N) | 96 K + 4 K | 8 K | | | |
| M30281FCHP (N) | 128 K + 4 K | 12 K | | | |
| M30280M8-XXXHP (N) | 64 K | 4 K | PLQP0080KB-A (80P6Q-A) | Mask ROM | U3, U5 |
| M30280MA-XXXHP (N) | 96 K | 8 K | | | |
| M30280MC-XXXHP (N) | 128 K | 12 K | | | |
| M30281M8-XXXHP (N) | 64 K | 4 K | PLQP0064KB-A (64P6Q-A) | | |
| M30281MA-XXXHP (N) | 96 K | 8 K | | | |
| M30281MC-XXXHP (N) | 128 K | 12 K | | | |

(N): New

**Table 1.4 M16C/28B Product List -Normal-ver.** **As of September, 2006**

| Type Number | ROM Capacity | RAM Capacity | Package Type | Remarks | Product Code |
|---|---|---|---|---|---|
| M30280FCBHP (D) | 128 K + 4 K | 12 K | PLQP0080KB-A (80P6Q-A) | Flash memory | U7 |
| M30281FCBHP (D) | 128 K + 4 K | 12 K | PLQP0064KB-A (64P6Q-A) | | |

(D): Under development

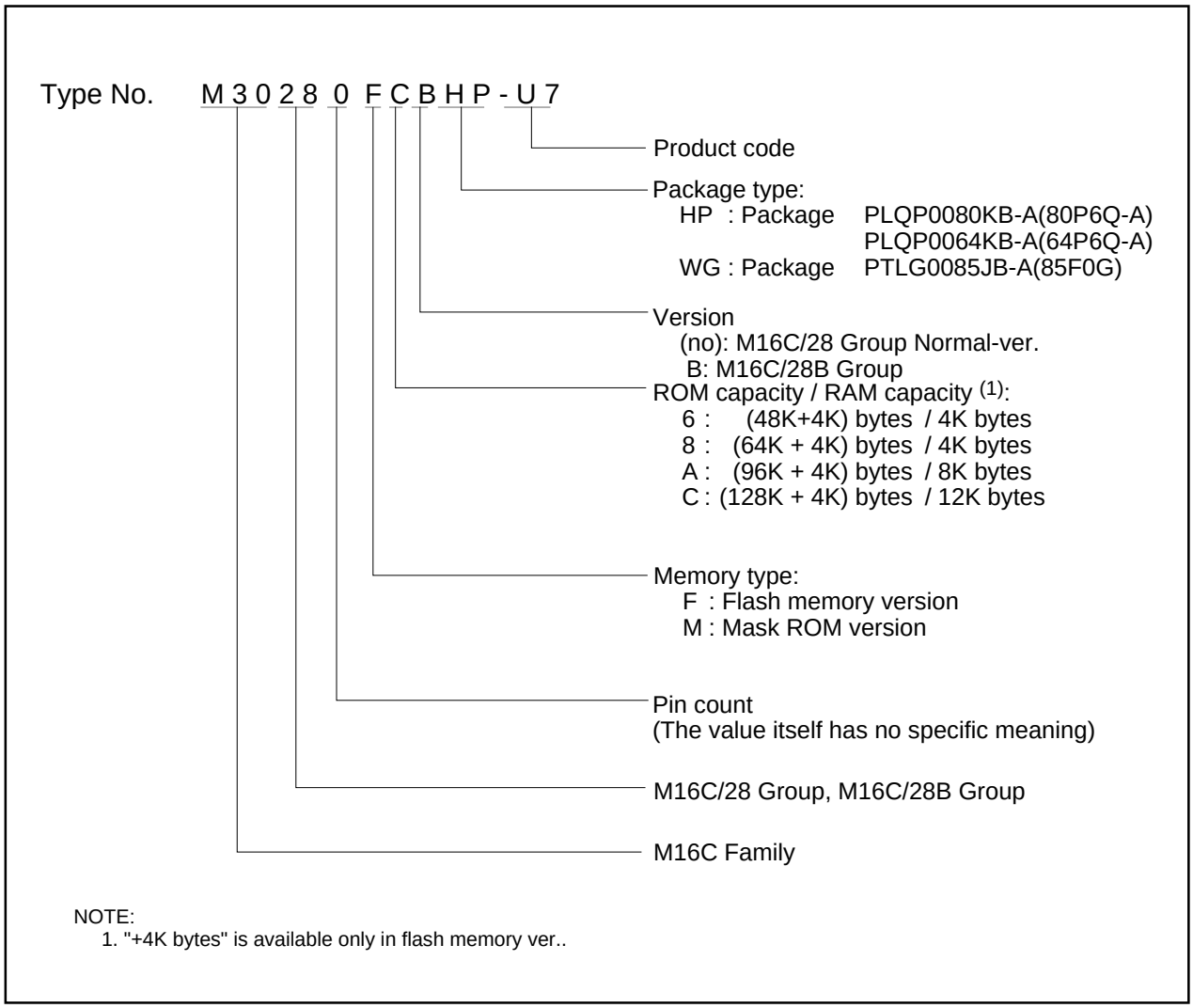



**Figure 1.3 Product Numbering System**

**Table 1.5 Product Code (Flash Memory-ver.) - M16C/28 Normal-ver., 64-Pin(1)/80-Pin(1)/85-Pin Package**

| Product Code | Package | Internal ROM (User Program Space) | | Internal ROM (Data Space) | | Operating Ambient Temperature |
|---|---|---|---|---|---|---|
| | | Program and Erase Endurance | Temperature Range | Program and Erase Endurance | Temperature Range | |
| U3 | Lead free | 100 | 0 to 60°C | 100 | 0 to 60°C | -40 to 85°C |
| U5 | | | | | | -20 to 85°C |
| U7 | | 1,000 | | 10,000 | -40 to 85°C | -40 to 85°C |
| U9 | | | | | -20 to 85°C | -20 to 85°C |

NOTE:
1. The lead contained products, D3, D5, D7 and D9, are put together with U3, U5, U7 and U9 respectively. Lead-free (Sn-Ag-Cu plating) products can be mounted by both conventional Sn-Pb paste and Lead-free paste.

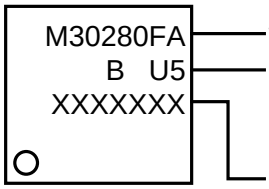
**Table 1.6 Product Code (Flash Memory-ver.) - M16C/28B Normal-ver., 64-Pin/85-Pin Package**

| Product Code | Package | Internal ROM (User Program Space) | | Internal ROM (Data Space) | | Operating Ambient Temperature |
|---|---|---|---|---|---|---|
| | | Program and Erase Endurance | Temperature Range | Program and Erase Endurance | Temperature Range | |
| U7 | Lead-free | 1,000 | 0 to 60°C | 10,000 | -40 to 85°C | -40 to 85°C |

**Table 1.7 Product Code (Mask ROM ver.) - M16C/28B Normal-ver., 64-Pin/80-Pin/85-Pin Package**

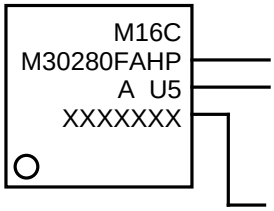
| Product Code | Package | Operating Ambient Temperature |
|---|---|---|
| U3 | Lead-free | -40 to 85°C |
| U5 | | -20 to 85°C |

(1) Flash Memory Version, PTLG0085JB-A (85F0G), Normal-ver.



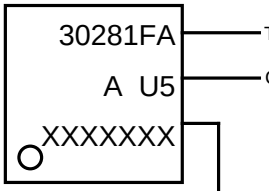

Type No. M30280FAWG
Chip version and product code
B : Chip version.
The first edition is shown to be blank and continues with A, B, and C.
U5 : Product code. (See **Table 1.5**)
Date code seven digits
Manufacturing management code

(2) Flash Memory Version, PLQP0080KB-A (80P6Q-A), Normal-ver.



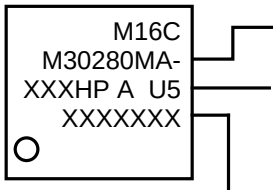

Type No. M30280FAHP
Chip version and product code
A : Chip version and product code(1)
The first edition is shown to be blank and continues with A, B and C.
U5 : Product code. (**Table 1.4**)
Date code seven digits
Manufacturing management code

(3) Flash Memory Version, PLQP0064KB-A (64P6Q-A), Normal-ver.



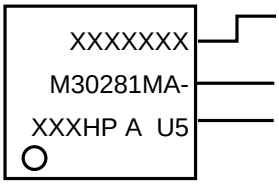

Type No. M30281FAHP
Chip version and product code
A : Chip version and product code(1)
The first edition is shown to be blank and continues with A, B and C.
U5 : Product code. (**Table 1.4**)
Date code seven digits
Manufacturing management code

(4) Mask ROM Version, PLQP0080KB-A (80P6Q-A), Normal-ver.




Type No. M30280MAHP
Chip version and product code
XXX : ROM No.
A : Chip version and product code(1)
The first edition is shown to be blank and continues with A, B and C.
U5 : Product code. (**Table 1.6**)
Date code seven digits
Manufacturing management code

(5) Mask ROM Version, PLQP0064-KB-A (64P6Q-A), Normal-ver.



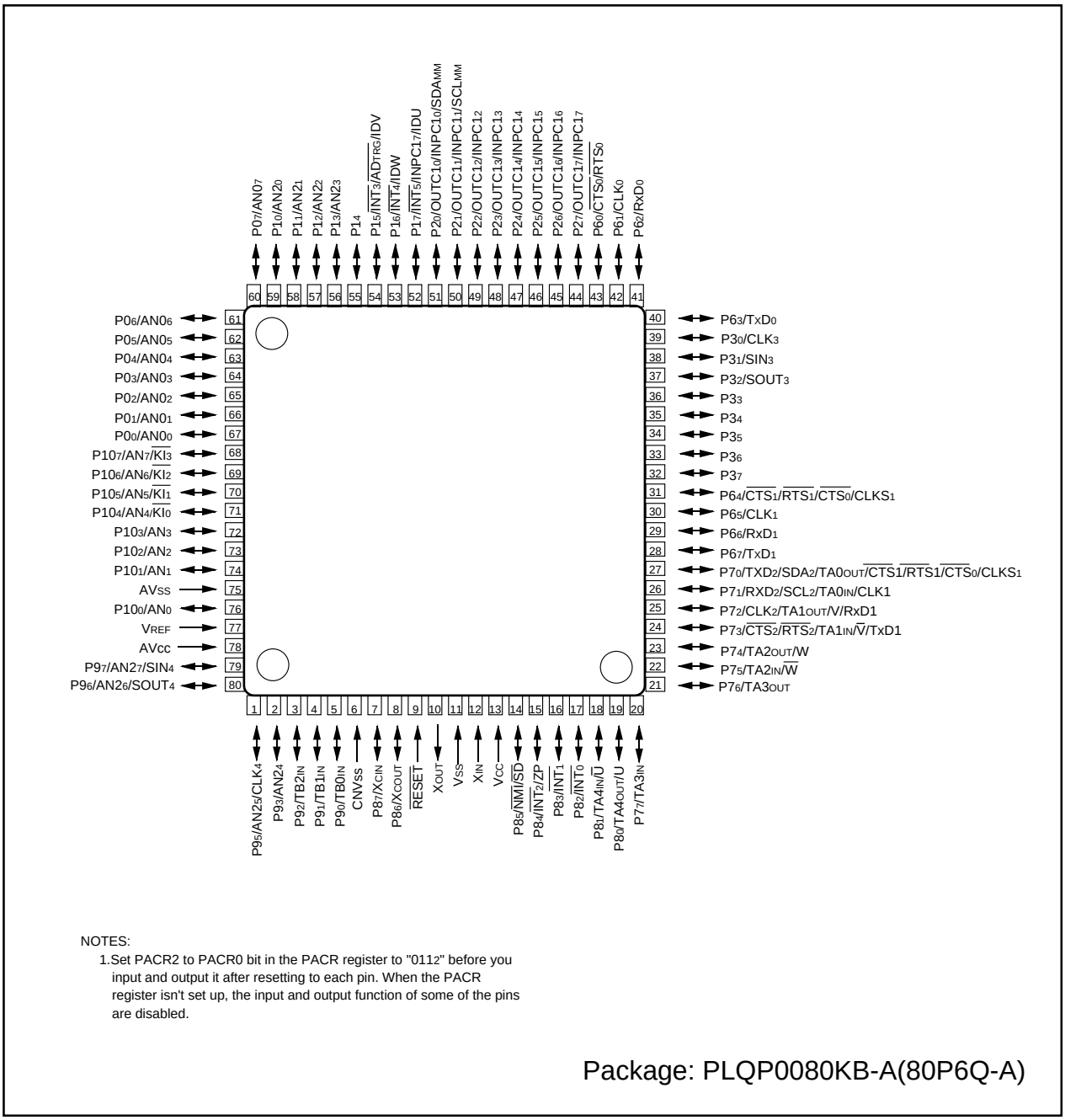

Date code seven digits
Manufacturing management code
Type No. M30281MAHP
Chip version and product code
XXX: ROM No.
A : Chip version and product code(1)
The first edition is shown to be blank and continues with A, B and C.
U5 : Product code. (**Table 1.6**)

NOTES:
1. The following functinos are not available in the first version and version A products.
-Delay trigger mode 0 of A/D conversion
-Delay trigger mode 1 of A/D conversion

**Figure 1.4 Marking Diagram-M16C/28 Normal-ver.**

**Table 1.8 Pin Characteristics for 85-pin Package (continued)**

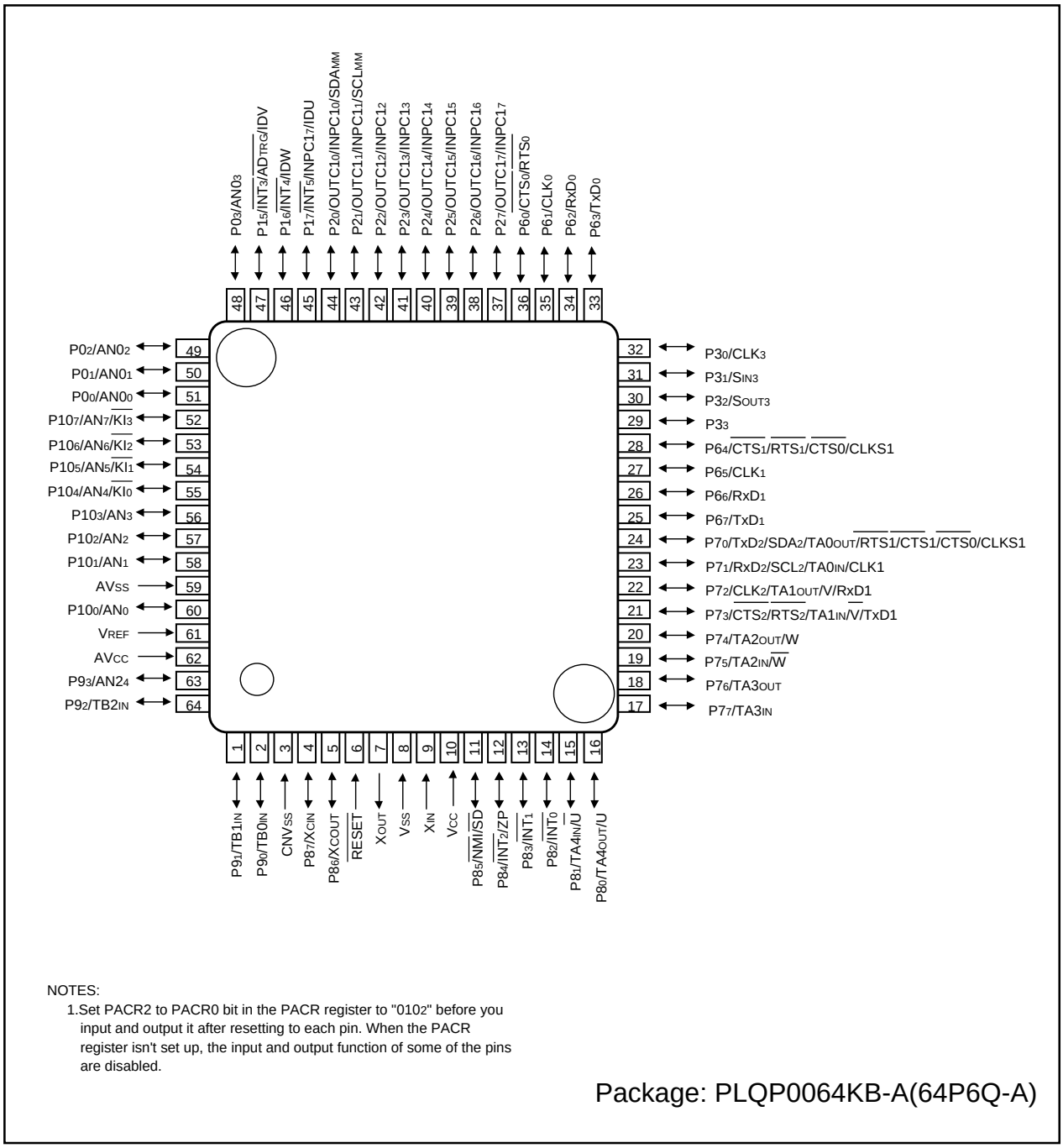
| Pin No. | Control Pin | Port | Interrupt Pin | Timer Pin | Timer S Pin | UART Pin | Multi-master I²C bus Pin | Analog Pin | PLQP0080KB-A Pin Number |
|---|---|---|---|---|---|---|---|---|---|
| E8 | | P15 | $\overline{INT_3}$ | IDV | | | | $\overline{ADTRG}$ | 54 |
| E9 | | P16 | $\overline{INT_4}$ | IDW | | | | | 53 |
| E10 | | P17 | $\overline{INT_5}$ | IDU | INPC17 | | | | 52 |
| F1 | Vcc | | | | | | | | 13 |
| F2 | Vcc | | | | | | | | 13 |
| F3 | | P85 | $\overline{NMI}$ | $\overline{SD}$ | | | | | 14 |
| F8 | Vss(1) | | | | | | | | (11) |
| F9 | | P20 | | | OUTC10 / INPC10 | | SDAMM | | 51 |
| F10 | | P21 | | | OUTC11 / INPC11 | | SCLMM | | 50 |
| G1 | | P84 | $\overline{INT_2}$ | ZP | | | | | 15 |
| G2 | | P83 | $\overline{INT_1}$ | | | | | | 16 |
| G3 | | P82 | $\overline{INT_0}$ | | | | | | 17 |
| G8 | | P22 | | | OUTC12 / INPC12 | | | | 49 |
| G9 | | P23 | | | OUTC13 / INPC13 | | | | 48 |
| G10 | | P24 | | | OUTC14 / INPC14 | | | | 47 |
| H1 | | P81 | | TA4IN / $\overline{U}$ | | | | | 18 |
| H2 | | P80 | | TA4OUT / U | | | | | 19 |
| H3 | | P71 | | TA0IN | | RXD2 / SCL2 / CLK1 | | | 26 |
| H4 | | P66 | | | | RXD1 | | | 29 |
| H5 | Vss(1) | | | | | | | | (11) |
| H6 | | P35 | | | | | | | 34 |
| H7 | | P32 | | | | SOUT3 | | | 37 |
| H8 | | P25 | | | OUTC15 / INPC15 | | | | 46 |
| H9 | | P26 | | | OUTC16 / INPC16 | | | | 45 |
| H10 | | P27 | | | OUTC17 / INPC17 | | | | 44 |
| J1 | | P76 | | TA3OUT | | | | | 21 |
| J2 | | P74 | | TA2OUT / W | | | | | 23 |
| J3 | | P72 | | TA1OUT / V | | CLK2 / RXD1 | | | 25 |
| J4 | | P67 | | | | TXD1 | | | 28 |
| J5 | | P64 | | | | $\overline{RTS_1}$ / $\overline{CTS_1}$/ $\overline{CTS_0}$ / CLKS1 | | | 31 |
| J6 | | P36 | | | | | | | 33 |
| J7 | | P33 | | | | | | | 36 |
| J8 | | P62 | | | | RXD0 | | | 41 |
| J9 | | P60 | | | | $\overline{RTS_0}$ / $\overline{CTS_0}$ | | | 43 |
| J10 | | P61 | | | | CLK0 | | | 42 |
| K1 | | P77 | | TA3IN | | | | | 20 |
| K2 | | P75 | | TA2IN / $\overline{W}$ | | | | | 22 |
| K3 | | P73 | | TA1IN / $\overline{V}$ | | $\overline{CTS_2}$ / $\overline{RTS_2}$ / $\overline{TXD_1}$ | | | 24 |
| K4 | | P70 | | TA0OUT | | TXD2 / SDA2 / $\overline{RTS_1}$ / $\overline{CTS_1}$ / $\overline{CTS_0}$ / $\overline{CLKS_1}$ | | | 27 |
| K5 | | P65 | | | | CLK1 | | | 30 |
| K6 | | P37 | | | | | | | 32 |
| K7 | | P34 | | | | | | | 35 |
| K8 | | P63 | | | | TXD0 | | | 40 |
| K9 | | P30 | | | | CLK3 | | | 39 |
| K10 | | P31 | | | | SIN3 | | | 38 |




NOTES:
1. Set PACR2 to PACR0 bit in the PACR register to "011₂" before you input and output it after resetting to each pin. When the PACR register isn't set up, the input and output function of some of the pins are disabled.

Package: PLQP0080KB-A(80P6Q-A)

**Figure 1.5 Pin Assignment (Top View) of 80-Pin Package**




NOTES:
1. Set PACR2 to PACR0 bit in the PACR register to "010₂" before you input and output it after resetting to each pin. When the PACR register isn't set up, the input and output function of some of the pins are disabled.

Package: PLQP0064KB-A(64P6Q-A)

**Figure 1.6 Pin Assignment (Top View) of 64-Pin Package**

## 1.6 Pin Description

**Table 1.10 Pin Description (64-Pin, 80-Pin and 85-Pin Packages)**

| Classification | Symbol | I/O Type | Function |
|---|---|---|---|
| Power Supply | VCC, VSS | I | Apply 2.7 to 5.5V to the Vcc pin. Apply 0V to the Vss pin. |
| Analog Power Supply | AVCC<br>AVSS | I | Supplies power to the A/D converter. Connect the AVCC pin to VCC and the AVSS pin to VSS. |
| Reset Input | $\overline{\text{RESET}}$ | I | The MCU is in a reset state when "L" is applied to the $\overline{\text{RESET}}$ pin |
| CNVSS | CNVSS | I | Connect the CNVSS pin to VSS. |
| Main Clock Input | XIN | I | I/O pins for the main clock oscillation circuit. Connect a ceramic resonator or crystal oscillator between XIN and XOUT. To apply external clock, apply it to XIN and leave XOUT open. If XIN is not used (for external oscillator or external clock) connect XIN pin to VCC and leave XOUT open. |
| Main Clock Output | XOUT | O | |
| Sub Clock Input | XCIN | I | I/O pins for the sub clock oscillation circuit. Connect a crystal oscillator between XCIN and XCOUT. |
| Sub Clock Output | XCOUT | O | |
| $\overline{\text{INT}}$ Interrupt Input | $\overline{\text{INT0}}$ to $\overline{\text{INT5}}$ | I | Input pins for the $\overline{\text{INT}}$ interrupt. $\overline{\text{INT2}}$ can be used for Timer A Z-phase function. |
| $\overline{\text{NMI}}$ Interrupt Input | $\overline{\text{NMI}}$ | I | Input pin for the $\overline{\text{NMI}}$ interrupt. $\overline{\text{NMI}}$ cannot be used as I/O port while the three-phase motor control is enabled. Apply a stable "H" to $\overline{\text{NMI}}$ after setting it's direction register to "0" when the three-phase motor control is enabled. |
| Key Input Interrupt | $\overline{\text{KI0}}$ to $\overline{\text{KI3}}$ | I | Input pins for the key input interrupt |
| Timer A | TA0OUT to TA4OUT | I/O | I/O pins for the timer A0 to A4 |
| | TA0IN to TA4IN | I | Input pins for the timer A0 to A4 |
| | ZP | I | Input pin for Z-phase |
| Timer B | TB0IN to TB2IN | I | Input pins for the timer B0 to B2 |
| Three-phase Motor Control Timer Output | U, $\overline{\text{U}}$, V, $\overline{\text{V}}$, W, $\overline{\text{W}}$ | O | Output pins for the three-phase motor control timer |
| | IDU, IDW, IDV, $\overline{\text{SD}}$ | I/O | Input and output pins for the three-phase motor control timer |
| Serial I/O | $\overline{\text{CTS0}}$ to $\overline{\text{CTS2}}$ | I | Input pins for data transmission control |
| | $\overline{\text{RTS0}}$ to $\overline{\text{RTS2}}$ | O | Output pins for data reception control |
| | CLK0 to CLK3 | I/O | Inputs and outputs the transfer clock |
| | RxD0 to RxD2 | I | Inputs serial data |
| | TxD0 to TxD2 | O | Outputs serial data |
| | CLKS1 | O | Output pin for transfer clock |
| $I^2C$ Mode | SDA2 | I/O | Inputs and outputs serial data |
| | SCL2 | | Inputs and outputs the transfer clock |
| Multi-master $I^2C$ bus | SDAMM | I/O | Inputs and outputs serial data |
| | SCLMM | | Inputs and outputs the transfer clock |
| Reference Voltage Input | VREF | I | Applies reference voltage to the A/D converter |
| A/D Converter | AN0 to AN7<br>AN00 to AN03<br>AN24 | I | Analog input pins for the A/D converter |
| | $\overline{\text{ADTRG}}$ | | Input pin for an external A/D trigger |

I : Input O : Output I/O : Input and output

**Table 1.10 Pin Description (64-Pin, 80-Pin and 85-Pin Packages) (Continued)**

| Classification | Symbol | I/O Type | Function |
|---|---|---|---|
| Timer S | INPC10 to INPC17 | I | Input pins for the time measurement function |
| | OUTC10 to OUTC17 | O | Output pins for the waveform generating function |
| I/O Ports | P00 to P03<br>P15 to P17<br>P20 to P27<br>P30 to P33<br>P60 to P67<br>P70 to P77<br>P80 to P87<br>P100 to P107 | I/O | I/O ports for CMOS. Each port can be programmed for input or output under the control of the direction register. An input port can be set, by program, for a pull-up resistor available or for no pull-up resister available in 4-bit units |
| | P90 to P93 | I/O | I/O ports having equivalent functions to P0 |

I : Input O : Output I/O : Input and output

**Table 1.10 Pin Description (80-Pin and 85-Pin Packages only) (Continued)**

| Classification | Symbol | I/O Type | Function |
|---|---|---|---|
| Serial I/O | CLK4 | I/O | Inputs and outputs the transfer clock |
| | SIN4 | I | Inputs serial data |
| | SOUT4 | O | Outputs serial data |
| A/D Converter | AN04 to AN07<br>AN20 to AN23<br>AN25 to AN27 | I | Analog input pins for the A/D converter |
| I/O Ports | P04 to P07<br>P10 to P14<br>P34 to P37 | I/O | I/O ports for CMOS. Each port can be programmed for input or output under the control of the direction register. An input port can be set, by program, for a pull-up resistor available or for no pull-up resister available in 4-bit units |
| | P95 to P97 | I/O | I/O ports having equivalent functions to P0 |

I : Input O : Output I/O : Input and output

# 2. Central Processing Unit (CPU)

**Figure 2.1** shows the CPU registers. The register bank is comprised of 7 registers (R0, R1, R2, R3, A0, A1 and FB) out of 13 CPU registers. Two sets of register banks are provided.

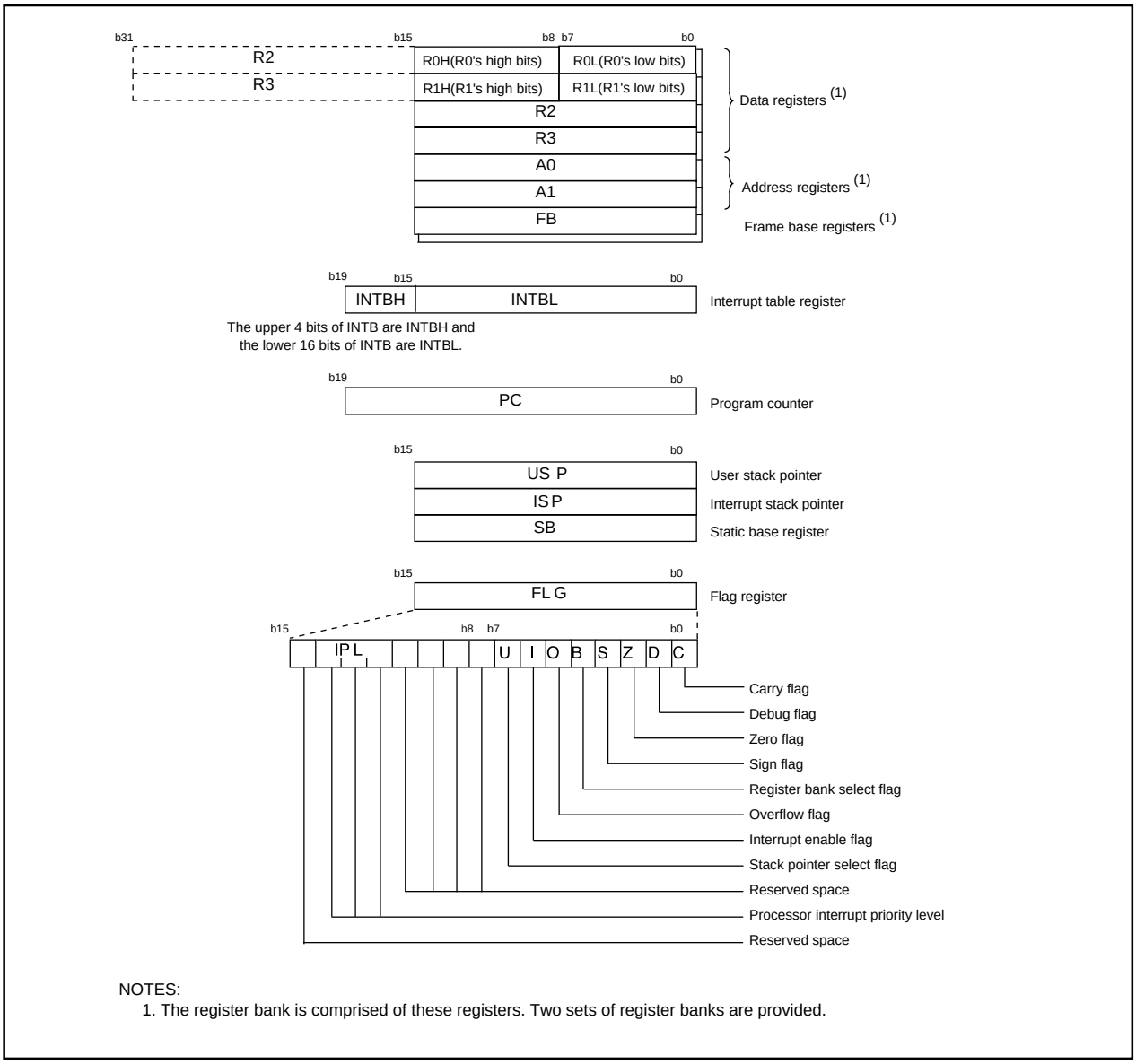



**Figure 2.1 Central Processing Unit Register**

## 2.1 Data Registers (R0, R1, R2 and R3)

The R0, R1, R2 and R3 registers are 16 bit registers for transfer and arithmetic/logic operations.

The R0 and R1 registers can be split into high-order bits(R0H, R1H) and low-order bits (R0L, R1L) to be used seperately as 8-bit data registers. Conversely, R2 and R0 can be combined with R2 to be used as a 32-bit data register (R2R0). The same applies to R1 and R2.

## 2.2 Address Registers (A0 and A1)

The register A0 consists of 16 bits, and is used for address register indirect addressing and address register relative addressing. They also are used for transfers and arithmetic/logic operations. A1 is the same as A0. In some instructions, registers A1 and A0 can be combined for use as a 32-bit address register (A1A0).

**Table 4.5 SFR Information(5)(1)**

| Address | Register | Symbol | After Reset |
|---|---|---|---|
| 034016 | | | |
| 034116 | | | |
| 034216 | Timer A1-1 register | TA11 | XX16 |
| 034316 | | | XX16 |
| 034416 | Timer A2-1 register | TA21 | XX16 |
| 034516 | | | XX16 |
| 034616 | Timer A4-1 register | TA41 | XX16 |
| 034716 | | | XX16 |
| 034816 | Three-phase PWM control register 0 | INVC0 | 0016 |
| 034916 | Three-phase PWM control register 1 | INVC1 | 0016 |
| 034A16 | Three-phase output buffer register 0 | IDB0 | 001111112 |
| 034B16 | Three-phase output buffer register 1 | IDB1 | 001111112 |
| 034C16 | Dead time timer | DTT | XX16 |
| 034D16 | Timer B2 interrupt occurrence frequency set counter | ICTB2 | XX16 |
| 034E16 | Position-data-retain function control register | PDRF | XXXX00002 |
| 034F16 | | | |
| 035016 | | | |
| 035116 | | | |
| 035216 | | | |
| 035316 | | | |
| 035416 | | | |
| 035516 | | | |
| 035616 | | | |
| 035716 | | | |
| 035816 | | | |
| 035916 | | | |
| 035A16 | | | |
| 035B16 | | | |
| 035C16 | | | |
| 035D16 | | | |
| 035E16 | Interrupt request cause select register 2 | IFSR2A | 00XXXXX02(2) |
| 035F16 | Interrupt request cause select register | IFSR | 0016 |
| 036016 | SI/O3 transmit/receive register | S3TRR | XX16 |
| 036116 | | | |
| 036216 | SI/O3 control register | S3C | 010000002 |
| 036316 | SI/O3 bit rate generator | S3BRG | XX16 |
| 036416 | SI/O4 transmit/receive register | S4TRR | XX16 |
| 036516 | | | |
| 036616 | SI/O4 control register | S4C | 010000002 |
| 036716 | SI/O4 bit rate generator | S4BRG | XX16 |
| 036816 | | | |
| 036916 | | | |
| 036A16 | | | |
| 036B16 | | | |
| 036C16 | | | |
| 036D16 | | | |
| 036E16 | | | |
| 036F16 | | | |
| 037016 | | | |
| 037116 | | | |
| 037216 | | | |
| 037316 | | | |
| 037416 | UART2 special mode register 4 | U2SMR4 | 0016 |
| 037516 | UART2 special mode register 3 | U2SMR3 | 000X0X0X2 |
| 037616 | UART2 special mode register 2 | U2SMR2 | X0000000 2 |
| 037716 | UART2 special mode register | U2SMR | X0000000 2 |
| 037816 | UART2 transmit/receive mode register | U2MR | 0016 |
| 037916 | UART2 bit rate generator | U2BRG | XX16 |
| 037A16 | UART2 transmit buffer register | U2TB | XX16 |
| 037B16 | | | XX16 |
| 037C16 | UART2 transmit/receive control register 0 | U2C0 | 000010002 |
| 037D16 | UART2 transmit/receive control register 1 | U2C1 | 000000102 |
| 037E16 | UART2 receive buffer register | U2RB | XX16 |
| 037F16 | | | XX16 |

Note 1: The blank spaces are reserved. No access is allowed.
Note 2: Write 1 to bit 0 after reset.

X : Undefined

**Table 4.6 SFR Information(6)(1)**

| Address | Register | Symbol | After Reset |
|---|---|---|---|
| 038016 | Count start flag | TABSR | 0016 |
| 038116 | Clock prescaler reset flag | CPSRF | 0XXXXXXX2 |
| 038216 | One-shot start flag | ONSF | 0016 |
| 038316 | Trigger select register | TRGSR | 0016 |
| 038416 | Up-down flag | UDF | 0016 |
| 038516 | | | |
| 038616 | Timer A0 register | TA0 | XX16 |
| 038716 | | | XX16 |
| 038816 | Timer A1 register | TA1 | XX16 |
| 038916 | | | XX16 |
| 038A16 | Timer A2 register | TA2 | XX16 |
| 038B16 | | | XX16 |
| 038C16 | Timer A3 register | TA3 | XX16 |
| 038D16 | | | XX16 |
| 038E16 | Timer A4 register | TA4 | XX16 |
| 038F16 | | | XX16 |
| 039016 | Timer B0 register | TB0 | XX16 |
| 039116 | | | XX16 |
| 039216 | Timer B1 register | TB1 | XX16 |
| 039316 | | | XX16 |
| 039416 | Timer B2 register | TB2 | XX16 |
| 039516 | | | XX16 |
| 039616 | Timer A0 mode register | TA0MR | 0016 |
| 039716 | Timer A1 mode register | TA1MR | 0016 |
| 039816 | Timer A2 mode register | TA2MR | 0016 |
| 039916 | Timer A3 mode register | TA3MR | 0016 |
| 039A16 | Timer A4 mode register | TA4MR | 0016 |
| 039B16 | Timer B0 mode register | TB0MR | 00XX00002 |
| 039C16 | Timer B1 mode register | TB1MR | 00XX00002 |
| 039D16 | Timer B2 mode register | TB2MR | 00XX00002 |
| 039E16 | Timer B2 special mode register | TB2SC | X00000002 |
| 039F16 | | | |
| 03A016 | UART0 transmit/receive mode register | U0MR | 0016 |
| 03A116 | UART0 bit rate generator | U0BRG | XX16 |
| 03A216 | UART0 transmit buffer register | U0TB | XX16 |
| 03A316 | | | XX16 |
| 03A416 | UART0 transmit/receive control register 0 | U0C0 | 000010002 |
| 03A516 | UART0 transmit/receive control register 1 | U0C1 | 000000102 |
| 03A616 | UART0 receive buffer register | U0RB | XX16 |
| 03A716 | | | XX16 |
| 03A816 | UART1 transmit/receive mode register | U1MR | 0016 |
| 03A916 | UART1 bit rate generator | U1BRG | XX16 |
| 03AA16 | UART1 transmit buffer register | U1TB | XX16 |
| 03AB16 | | | XX16 |
| 03AC16 | UART1 transmit/receive control register 0 | U1C0 | 000010002 |
| 03AD16 | UART1 transmit/receive control register 1 | U1C1 | 000000102 |
| 03AE16 | UART1 receive buffer register | U1RB | XX16 |
| 03AF16 | | | XX16 |
| 03B016 | UART transmit/receive control register 2 | UCON | X00000002 |
| 03B116 | | | |
| 03B216 | | | |
| 03B316 | | | |
| 03B416 | | | |
| 03B516 | | | |
| 03B616 | | | |
| 03B716 | | | |
| 03B816 | DMA0 request cause select register | DM0SL | 0016 |
| 03B916 | | | |
| 03BA16 | DMA1 request cause select register | DM1SL | 0016 |
| 03BB16 | | | |
| 03BC16 | | | |
| 03BD16 | | | |
| 03BE16 | | | |
| 03BF16 | | | |

Note 1:The blank spaces are reserved. No access is allowed.

X : Undefined

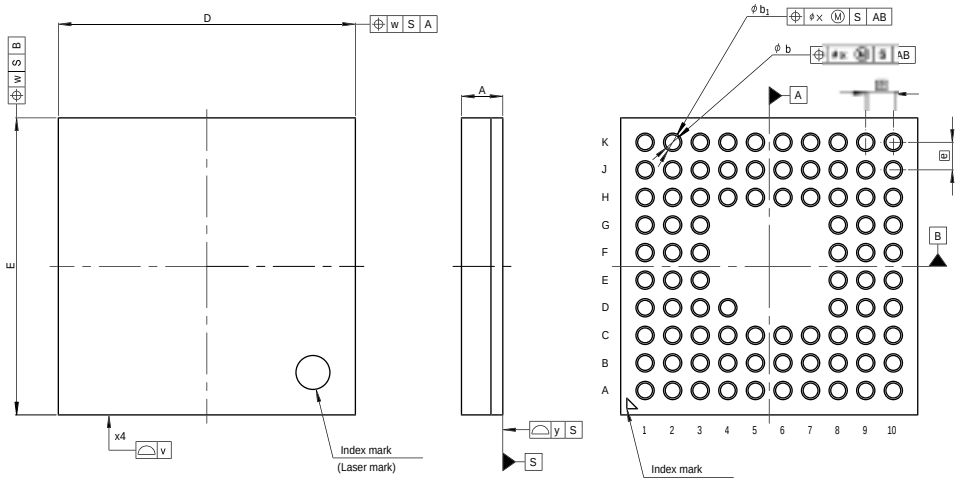
**Table 4.7 SFR Information(7)(1)**

| Address | Register | Symbol | After Reset |
|---|---|---|---|
| 03C0₁₆ | A/D register 0 | AD0 | XX₁₆ |
| 03C1₁₆ | | | XX₁₆ |
| 03C2₁₆ | A/D register 1 | AD1 | XX₁₆ |
| 03C3₁₆ | | | XX₁₆ |
| 03C4₁₆ | A/D register 2 | AD2 | XX₁₆ |
| 03C5₁₆ | | | XX₁₆ |
| 03C6₁₆ | A/D register 3 | AD3 | XX₁₆ |
| 03C7₁₆ | | | XX₁₆ |
| 03C8₁₆ | A/D register 4 | AD4 | XX₁₆ |
| 03C9₁₆ | | | XX₁₆ |
| 03CA₁₆ | A/D register 5 | AD5 | XX₁₆ |
| 03CB₁₆ | | | XX₁₆ |
| 03CC₁₆ | A/D register 6 | AD6 | XX₁₆ |
| 03CD₁₆ | | | XX₁₆ |
| 03CE₁₆ | A/D register 7 | AD7 | XX₁₆ |
| 03CF₁₆ | | | XX₁₆ |
| 03D0₁₆ | | | |
| 03D1₁₆ | | | |
| 03D2₁₆ | A/D trigger control register | ADTRGCON | 00₁₆ |
| 03D3₁₆ | A/D convert status register 0 | ADSTAT0 | 00000X00₂ |
| 03D4₁₆ | A/D control register 2 | ADCON2 | 00₁₆ |
| 03D5₁₆ | | | |
| 03D6₁₆ | A/D control register 0 | ADCON0 | 00000XXX₂ |
| 03D7₁₆ | A/D control register 1 | ADCON1 | 00₁₆ |
| 03D8₁₆ | | | |
| 03D9₁₆ | | | |
| 03DA₁₆ | | | |
| 03DB₁₆ | | | |
| 03DC₁₆ | | | |
| 03DD₁₆ | | | |
| 03DE₁₆ | | | |
| 03DF₁₆ | | | |
| 03E0₁₆ | Port P0 register | P0 | XX₁₆ |
| 03E1₁₆ | Port P1 register | P1 | XX₁₆ |
| 03E2₁₆ | Port P0 direction register | PD0 | 00₁₆ |
| 03E3₁₆ | Port P1 direction register | PD1 | 00₁₆ |
| 03E4₁₆ | Port P2 register | P2 | XX₁₆ |
| 03E5₁₆ | Port P3 register | P3 | XX₁₆ |
| 03E6₁₆ | Port P2 direction register | PD2 | 00₁₆ |
| 03E7₁₆ | Port P3 direction register | PD3 | 00₁₆ |
| 03E8₁₆ | | | |
| 03E9₁₆ | | | |
| 03EA₁₆ | | | |
| 03EB₁₆ | | | |
| 03EC₁₆ | Port P6 register | P6 | XX₁₆ |
| 03ED₁₆ | Port P7 register | P7 | XX₁₆ |
| 03EE₁₆ | Port P6 direction register | PD6 | 00₁₆ |
| 03EF₁₆ | Port P7 direction register | PD7 | 00₁₆ |
| 03F0₁₆ | Port P8 register | P8 | XX₁₆ |
| 03F1₁₆ | Port P9 register | P9 | XX₁₆ |
| 03F2₁₆ | Port P8 direction register | PD8 | 00₁₆ |
| 03F3₁₆ | Port P9 direction register | PD9 | 000X0000₂ |
| 03F4₁₆ | Port P10 register | P10 | XX₁₆ |
| 03F5₁₆ | | | |
| 03F6₁₆ | Port P10 direction register | PD10 | 00₁₆ |
| 03F7₁₆ | | | |
| 03F8₁₆ | | | |
| 03F9₁₆ | | | |
| 03FA₁₆ | | | |
| 03FB₁₆ | | | |
| 03FC₁₆ | Pull-up control register 0 | PUR0 | 00₁₆ |
| 03FD₁₆ | Pull-up control register 1 | PUR1 | 00₁₆ |
| 03FE₁₆ | Pull-up control register 2 | PUR2 | 00₁₆ |
| 03FF₁₆ | Port control register | PCR | 00₁₆ |

Note 1:The blank spaces are reserved. No access is allowed.

X : Undefined

| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-TFLGA85-7x7-0.65 | PTLG0085JB-A | 85F0G | 0.1g |




| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | — | 7.0 | — |
| E | — | 7.0 | — |
| v | — | — | 0.15 |
| w | — | — | 0.20 |
| A | — | — | 1.05 |
| e | — | 0.65 | — |
| b | 0.31 | 0.35 | 0.39 |
| $b_1$ | 0.39 | 0.43 | 0.47 |
| x | — | — | 0.08 |
| y | — | — | 0.10 |

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