Renesas Electronics America Inc - R4F2153VBR25KDV Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	H8S/2600
Core Size	16-Bit
Speed	25MHz
Connectivity	I²C, LPC, SCI
Peripherals	POR, PWM, WDT
Number of I/O	53
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	40K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LFBGA
Supplier Device Package	112-LFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r4f2153vbr25kdv

(2) DTC

The DTC sends the bus arbiter a request for the bus mastership when a request for DTC activation occurs. The DTC releases the bus mastership after a series of processes has completed.

7.9 Usage Notes

7.9.1 Module Stop Mode Setting

DTC operation can be enabled or disabled by the module stop control register (MSTPCR). In the initial state, DTC operation is enabled. Access to DTC registers is disabled when module stop mode is set. Note that when the DTC is being activated, module stop mode cannot be specified. For details, refer to section 22, Power-Down Modes.

7.9.2 On-Chip RAM

MRA, MRB, SAR, DAR, CRA, and CRB are all located in on-chip RAM. When the DTC is used, the RAME bit in SYSCR should not be cleared to 0.

7.9.3 DTCE Bit Setting

For DTCE bit setting, use bit manipulation instructions such as BSET and BCLR, for reading and writing. Multiple DTC activation sources can be set at one time (only at the initial setting) by masking all interrupts and writing data after executing a dummy read on the relevant register.

7.9.4 DTC Activation by Interrupt Sources of SCI, IIC, or A/D Converter

Interrupt sources of the SCI, IIC, or A/D converter which activate the DTC are cleared when DTC reads from or writes to the respective registers, and they cannot be cleared by the DISEL bit.

- TCSR_1

Bit	Bit Name	Initial Value	R/W	Description
7	CMFB	0	R/(W)*	Compare-Match Flag B [Setting condition] When the values of TCNT_1 and TCORB_1 match [Clearing condition] Read CMFB when CMFB = 1, then write 0 in CMFB
6	CMFA	0	R/(W)*	Compare-Match Flag A [Setting condition] When the values of TCNT_1 and TCORA_1 match [Clearing condition] Read CMFA when CMFA = 1, then write 0 in CMFA
5	OVF	0	R/(W)*	Timer Overflow Flag [Setting condition] When TCNT_1 overflows from H′FF to H′00 [Clearing condition] Read OVF when OVF = 1, then write 0 in OVF
4 to 0	—	All 1	R	Reserved These bits are always read as 1 and cannot be modified.

Note: * Only 0 can be written to clear the flag.

- TCSR_1

Bit	Bit Name	Initial Value	R/W	Description
7	OVF	0	R/(W)*[1]	Overflow Flag Indicates that TCNT has overflowed (changes from H'FF to H'00). [Setting conditions] • When TCNT overflows (changes from H'FF to H'00) • When internal reset request generation is selected in watchdog timer mode, OVF is cleared automatically by the internal reset. [Clearing conditions] • When TCSR is read when OVF = 1*[2], then 0 is written to OVF • When 0 is written to TME
6	WT/$\overline{IT}$	0	R/W	Timer Mode Select Selects whether the WDT is used as a watchdog timer or interval timer. 0: Interval timer mode 1: Watchdog timer mode
5	TME	0	R/W	Timer Enable When this bit is set to 1, TCNT starts counting. When this bit is cleared, TCNT stops counting and is initialized to H'00. When the PSS bit is 1, TCNT is not initialized. Write H'00 to initialize TCNT.
4	PSS	0	R/W	Prescaler Select Selects the clock source to be input to TCNT. 0: Counts the divided cycle of ϕ–based prescaler (PSM) 1: Counts the divided cycle of ϕSUB–based prescaler (PSS)
3	RST/$\overline{NMI}$	0	R/W	Reset or NMI Selects to request an internal reset or an NMI interrupt when TCNT has overflowed. 0: An NMI interrupt is requested 1: An internal reset is requested

15.4.7 IRIC Setting Timing and SCL Control

The interrupt request flag (IRIC) is set at different times depending on the WAIT bit in ICMR, the FS bit in SAR, and the FSX bit in SARX. If the ICDRE or ICDRF flag is set to 1, SCL is automatically held low after one frame has been transferred; this timing is synchronized with the internal clock. Figures 15.25 to 15.27 show the IRIC set timing and SCL control.

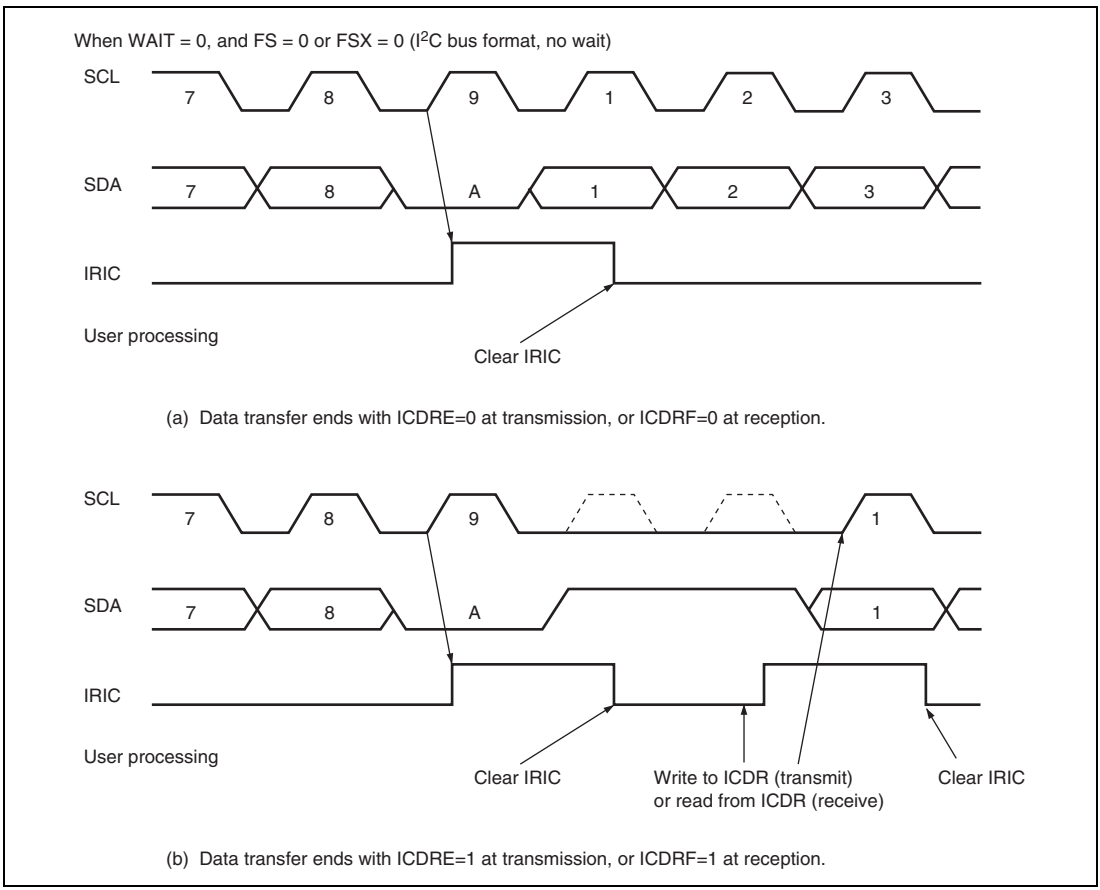

Figure 15.25 IRIC Setting Timing and SCL Control (1)

Bit	Bit Name	Initial Value	R/W Slave	R/W Host	Description
1	IBF1	0	R	R	Input Data Register Full Indicates whether or not there is receive data in IDR1. This bit is an internal interrupt source to the slave processor (this LSI). 0: There is not receive data in IDR1 [Clearing condition] When the slave processor reads IDR 1: There is receive data in IDR1 [Setting condition] When the host processor writes to IDR using I/O write cycle
0	OBF1	0	R/(W)*	R	Output Data Register Full Indicates whether or not there is transmit data in ODR1. 0: There is not transmit data in ODR1 [Clearing condition] When the host processor reads ODR1 using I/O read cycle, or the slave processor writes 0 to the OBF1 bit 1: There is transmit data in ODR1 [Setting condition] When the slave processor writes to ODR1

Note: * Only 0 can be written to clear the flag.

16.3.21 BT Status Register 0 (BTSR0)

BTSR0 is one of the registers used to implement BT mode. This register includes flags that control interrupts to the slave (this LSI).

Bit	Bit Name	Initial Value	R/W Slave	R/W Host	Description
7 to 5	—	All 0	R/W	—	Reserved The initial value should not be changed.
4	FRDI	0	R/(W)*	—	FIFO Read Request Interrupt This status flag indicates that host writes the data to BTDTR buffer with FIFO full state at the host write transfer. When the IBFIE3 bit and FRDIE bit are set to 1, IBFI3 interrupt is requested to the slave. The slave must clear the flag after creating an unused area by reading the data in FIFO. 0: FIFO read is not requested [Clearing condition] After the slave reads FRDI = 1, writes 0 to this bit. 1: FIFO read is requested. [Setting condition] After the host processor transfers data, the host writes the data with FIFO Full state.
3	HRDI	0	R/(W)*	—	BT Host Read Interrupt This status flag indicates that the host reads 1 byte from BTDTR buffer. When the IBFIE3 bit and HRDIE bit are set to 1, IBFI3 interrupt is requested to the slave. 0: Host BTDTR read wait state [Clearing condition] After the slave reads HRDI = 1, writes 0 to this bit. 1: The host reads from BTDTR. [Setting condition] The host reads one byte from BTDTR.

Bit	Bit Name	Initial Value	R/W Slave	R/W Host	Description
2	HWRI	0	R/(W)*	—	BT Host Write Interrupt This status flag indicates that the host writes 1byte to BTDTR buffer. When the IBFIE3 bit and HWRIE bit are set to 1, IBFI3 interrupt is requested to the slave. 0: Host BTDTR write wait state [Clearing condition] After the slave reads HWRI = 1, writes 0 to this bit. 1: The host writes to BTDTR [Setting condition] The host writes one byte to BTDTR.
1	HBTWI	0	R/(W)*	—	BTDTR Host Write Start Interrupt This status flag indicates that the host writes the first byte of valid data to BTDTR buffer. When the IBFIE3 bit and HBTWIE bit are set to 1, IBFI3 interrupt is requested to the slave. 0: BTDTR host write start wait state [Clearing condition] After the slave reads HBTWI = 1 and writes 0 to this bit. 1: BTDTR host write start [Setting condition] The host starts writing valid data to BTDTR.

16.3.28 BT FIFO Valid Size Register 0 (BTFVSR0)

BTFVSR0 is one of the registers used to implement BT mode. BTFVSR0 indicates a valid data size in the FIFO for host write transfer.

			R/W		
Bit	**Bit Name**	**Initial Value**	**Slave**	**Host**	**Description**
7 to 0	N7 to N0	All 0	R	—	These bits indicate the number of valid bytes in the FIFO (the number of bytes which the slave can read) for host write transfer. When data is written from the host, the value in BTFVSR0 is incremented by the number of bytes that have been written to. Further, when data is read from the slave, the value is decremented by only the number of bytes that have been read.

16.3.29 BT FIFO Valid Size Register 1 (BTFVSR1)

BTFVSR1 is one of the registers used to implement BT mode. BTFVSR1 indicates a valid data size in the FIFO for host read transfer.

			R/W		
Bit	**Bit Name**	**Initial Value**	**Slave**	**Host**	**Description**
7 to 0	N7 to N0	All 0	R	—	These bits indicate the number of valid bytes in the FIFO (the number of bytes which the host can read) for host read transfer. When data is written from the slave, the value in BTFVSR1 is incremented by the number of bytes that have been written to. Further, when data is read from the host, the value is decremented by only the number of bytes that have been read.

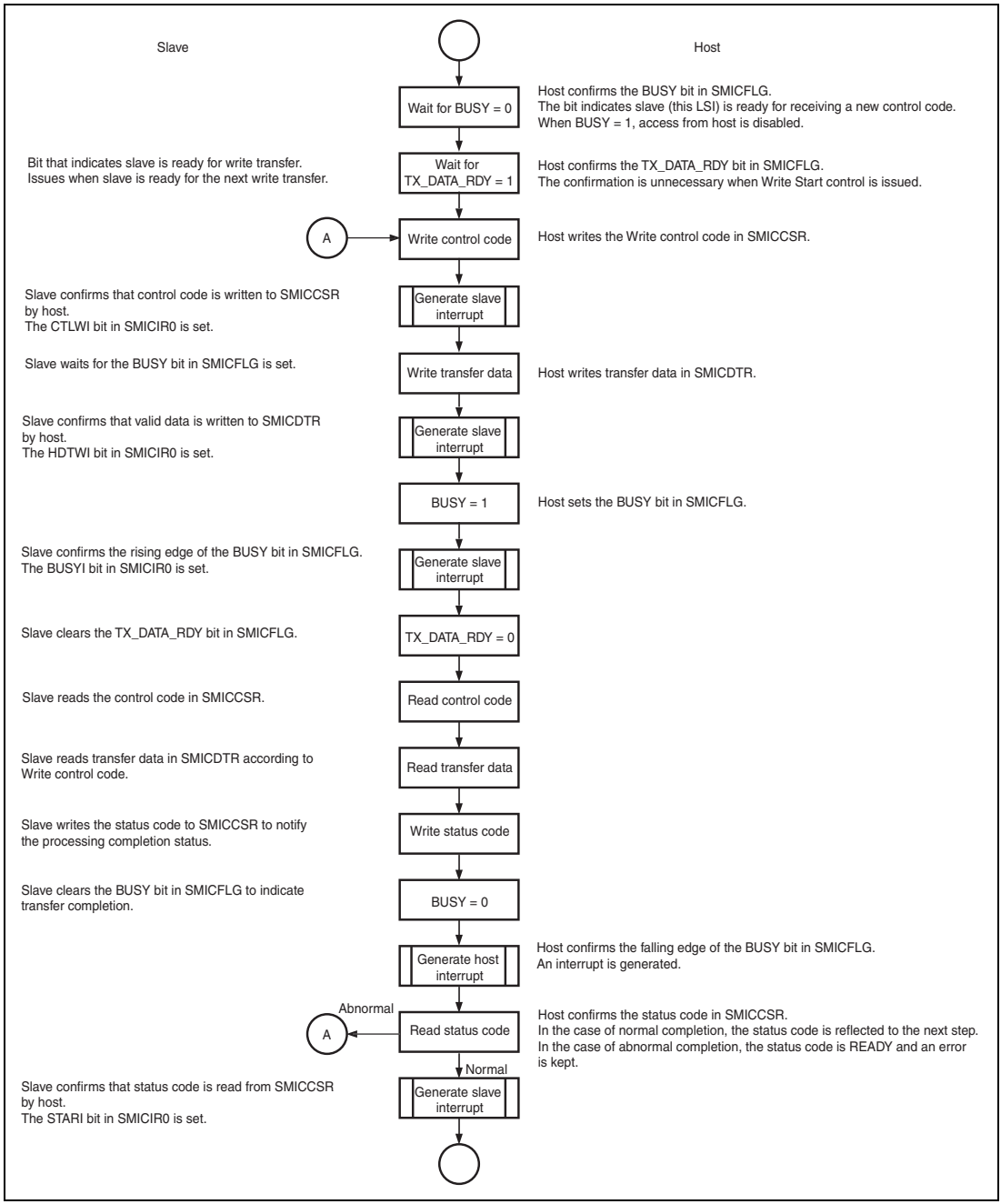

Figure 16.4 SMIC Write Transfer Flow

Section 18 RAM

This LSI has 40 kbytes of on-chip high-speed static RAM. The RAM is connected to the CPU by a 16-bit data bus, enabling one-state access by the CPU to both byte data and word data.

The on-chip RAM can be enabled or disabled by means of the RAME bit in the system control register (SYSCR). For details on SYSCR, see section 3.2.2, System Control Register (SYSCR).

(2) Programming/Erasing Initialization

The on-chip programming/erasing program to be downloaded includes the initialization program.

The specified period pulse must be applied when programming or erasing. The specified pulse width is made by the method in which wait loop is configured by the CPU instruction. The operating frequency of the CPU must be set.

The initial program is set as a parameter of the programming/erasing program which has downloaded these settings.

(a) Flash programming/erasing frequency parameter (FPEFEQ: general register ER0 of CPU)

This parameter sets the operating frequency of the CPU. The settable range of the operating frequency in this LSI is 20 to 25 MHz.

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	—	—	Unused This bit should be cleared to 0.
15 to 0	F15 to F0	—	R/W	Frequency Set Set the operating frequency of the CPU. With the PLL multiplication function, set the frequency multiplied. The setting value must be calculated as the following methods. 1. The operating frequency which is shown in MHz units must be rounded in a number to three decimal places and be shown in a number of two decimal places. 2. The value multiplied by 100 is converted to the binary digit and is written to the FPEFEQ parameter (general register ER0). For example, when the operating frequency of the CPU is 25.000 MHz, the value is as follows. 1. The number to three decimal places of 25.000 is rounded and the value is thus 25.00. 2. The formula that 25.00 × 100 = 2500 is converted to the binary digit and B'0000,1001,1101,0100 (H'09C4) is set to ER0.

Bit	Bit Name	Initial Value	R/W	Description
2	WD	—	R/W	Write Data Address Detect When the address in the flash memory area is specified as the start address of the storage destination of the program data, an error occurs. 0: Setting of write data address is normal 1: Setting of write data address is abnormal
1	WA	—	R/W	Write Address Error Detect When the following items are specified as the start address of the programming destination, an error occurs. • When the programming destination address in the area other than flash memory is specified • When the specified address is not in a 128-byte boundary. (The lower eight bits of the address are other than H'00 and H'80.) 0: Setting of programming destination address is normal 1: Setting of programming destination address is abnormal
0	SF	—	R/W	Success/Fail Indicates whether the program processing is ended normally or not. 0: Programming is ended normally (no error) 1: Programming is ended abnormally (error occurs)

19.5.2 Software Protection

Software protection is set up in any of two ways: by disabling the downloading of on-chip programs for programming and erasing and by means of a key code.

Table 19.10 Software Protection

		Function to be Protected	
Item	**Description**	**Download**	**Program/Erase**
Protection by the SCO bit	• The program/erase-protected state is entered by clearing the SCO bit in FCCS which disables the downloading of the programming/erasing programs.	○	○
Protection by the FKEY register	• Downloading and programming/erasing are disabled unless the required key code is written in FKEY. Different key codes are used for downloading and for programming/erasing.	○	○

19.5.3 Error Protection

Error protection is a mechanism for aborting programming or erasure when an error occurs, in the form of the microcomputer entering runaway during programming/erasing of the flash memory or operations that are not according to the established procedures for programming/erasing. Aborting programming or erasure in such cases prevents damage to the flash memory due to excessive programming or erasing.

If the microcomputer malfunctions during programming/erasing of the flash memory, the FLER bit in the FCCS register is set to 1 and the error-protection state is entered, and this aborts the programming or erasure.

The FLER bit is set in the following conditions:

1. When an interrupt such as NMI occurs during programming/erasing.
2. When the flash memory is read during programming/erasing (including a vector read or an instruction fetch).
3. When a SLEEP instruction (including software-standby mode) is executed during programming/erasing.

4. When a bus master other than the CPU, such as the DTC, gets bus mastership during programming/erasing.

Error protection is cancelled only by a reset or by hardware-standby mode. Note that the reset should be released after the reset period of 100 μs which is longer than normal. Since high voltages are applied during programming/erasing of the flash memory, some voltage may remain after the error-protection state has been entered. For this reason, it is necessary to reduce the risk of damage to the flash memory by extending the reset period so that the charge is released.

The state-transition diagram in figure 19.16 shows transitions to and from the error-protection state.

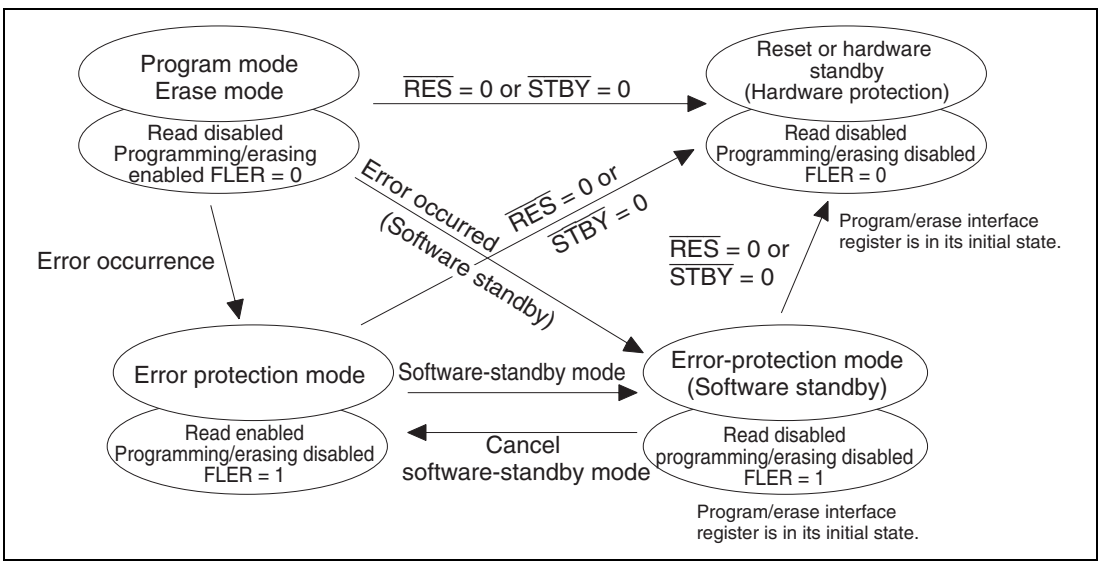

Figure 19.16 Transitions to Error-Protection State

11. If data other than H'FFFFFFFF is written to the key code area (H'00003C to H'00003F) of flash memory, only H'00 can be read in programmer mode. (In this case, data is read as H'00. Rewrite is possible after erasing the data.) For reading in programmer mode, make sure to write H'FFFFFFFF to the entire key code area. If data other than H'FF is to be written to the key code area in programmer mode, a verification error will occur unless a software countermeasure is taken for the PROM programmer and the version of its program.
12. The programming program that includes the initialization routine and the erasing program that includes the initialization routine are each 3 Kbytes or less. Accordingly, when the CPU clock frequency is 25 MHz, the download for each program takes approximately 256 μs at the maximum.
13. While an instruction in on-chip RAM is being executed, the DTC can write to the SCO bit in FCCS that is used for a download request or FMATS that is used for MAT switching. Make sure that these registers are not accidentally written to, otherwise an on-chip program may be downloaded and damage RAM or a MAT switchover may occur and the CPU get out of control. Do not use DTC to program flash related registers.
14. A programming/erasing program for flash memory used in the conventional H8S F-ZTAT microcomputer which does not support download of the on-chip program by a SCO transfer request cannot run in this LSI. Be sure to download the on-chip program to execute programming/erasing of flash memory in this LSI.
15. Unlike the conventional H8S F-ZTAT microcomputer, no countermeasures are available for a runaway by WDT during programming/erasing. Prepare countermeasures (e.g. use of the periodic timer interrupts) for WDT with taking the programming/erasing time into consideration as required.

- MSTPCRA

Bit	Bit Name	Initial Value	R/W	Corresponding Module
7 to 3	MSTPA7 to MSTPA3	All 0	R/W	Reserved The initial values should not be changed.
2	MSTPA2	0	R/W	14-bit PWM timer (PWMX_1)
1	MSTPA1	0	R/W	14-bit PWM timer (PWMX_0)
0	MSTPA0	0	R/W	Reserved The initial value should not be changed.

MSTPCR sets operation and stop by the combination of bits as follows:

MSTPCRH (bit 3) MSTP11	MSTPCRA (bit 2) MSTPA2	Function
0	0	14-bit PWM timer (PWMX_1) operates.
0	1	14-bit PWM timer (PWMX_1) stops.
1	x	

MSTPCRH (bit 3) MSTP11	MSTPCRA (bit 1) MSTPA1	Function
0	0	14-bit PWM timer (PWMX_0) operates.
0	1	14-bit PWM timer (PWMX_0) stops.
1	x	

Note: Bit 3 of MSTPCRH is the module stop bit for PWMX_0 and PWMX_1.

[Legend] x: Don't care

22.5 Software Standby Mode

The CPU makes a transition to software standby mode when the SLEEP instruction is executed with the SSBY bit in SBYCR set to 1, and the PSS bit in TCSR (WDT_1) cleared to 0.

In software standby mode, the CPU, on-chip peripheral modules, and clock pulse generator all stop. However, the contents of the CPU registers, on-chip RAM data, I/O ports, and the states of on-chip peripheral modules other than the PWMX, A/D converter, and part of the SCI are retained as long as the prescribed voltage is supplied.

Software standby mode is cleared by an external interrupt (NMI, IRQ0 to IRQ15), the $\overline{\text{RES}}$ pin input, or $\overline{\text{STBY}}$ pin input.

When an external interrupt request signal is input, system clock oscillation starts, and after the elapse of the time set in bits STS2 to STS0 in SBYCR, software standby mode is cleared, and interrupt exception handling is started. When exiting software standby mode by IRQ0 to IRQ15 interrupt, set the corresponding enable bit to 1 and ensure that any interrupt with a higher priority than IRQ0 to IRQ15 is not generated. Software standby mode is not exited if the corresponding enable bit is cleared to 0 or if the interrupt has been masked by the CPU.

When the $\overline{\text{RES}}$ pin is driven low, system clock oscillation is started. At the same time as system clock oscillation starts, the system clock is supplied to the entire LSI. Note that the $\overline{\text{RES}}$ pin must be held low until clock oscillation settles. When the $\overline{\text{RES}}$ pin goes high after clock oscillation settles, the CPU begins reset exception handling.

When the $\overline{\text{STBY}}$ pin is driven low, software standby mode is cancelled and a transition is made to hardware standby mode.

Figure 22.3 shows an example in which a transition is made to software standby mode at the falling edge of the NMI pin, and software standby mode is cleared at the rising edge of the NMI pin.

In this example, an NMI interrupt is accepted with the NMIEG bit in SYSCR cleared to 0 (falling edge specification), then the NMIEG bit is set to 1 (rising edge specification), the SSBY bit is set to 1, and a SLEEP instruction is executed, causing a transition to software standby mode.

Software standby mode is then cleared at the rising edge of the NMI pin.

Register Name	Abbreviation	Number of Bits	Address	Module	Data Bus Width	Number of Access States
Interrupt control register D	ICRD	8	H'FEE7	INT	8	2
Interrupt control register A	ICRA	8	H'FEE8	INT	8	2
Interrupt control register B	ICRB	8	H'FEE9	INT	8	2
Interrupt control register C	ICRC	8	H'FEEA	INT	8	2
IRQ status register	ISR	8	H'FEEB	INT	8	2
IRQ sense control register H	ISCRH	8	H'FEEC	INT	8	2
IRQ sense control register L	ISCRL	8	H'FEED	INT	8	2
DTC enable register A	DTCERA	8	H'FEEE	DTD	8	2
DTC enable register B	DTCERB	8	H'FEEF	DTC	8	2
DTC enable register C	DTCERC	8	H'FEF0	DTC	8	2
DTC enable register D	DTCERD	8	H'FEF1	DTC	8	2
DTC enable register E	DTCERE	8	H'FEF2	DTC	8	2
DTC vector register	DTVECR	8	H'FEF3	DTC	8	2
Address break control register	ABRKCR	8	H'FEF4	INT	8	2
Break address register A	BARA	8	H'FEF5	INT	8	2
Break address register B	BARB	8	H'FEF6	INT	8	2
Break address register C	BARC	8	H'FEF7	INT	8	2
IRQ enable register 16	IER16	8	H'FEF8	INT	8	2
IRQ status register 16	ISR16	8	H'FEF9	INT	8	2
IRQ sense control register 16H	ISCR16H	8	H'FEEA	INT	8	2
IRQ sense control register 16L	ISCR16L	8	H'FEFB	INT	8	2
IRQ sense port select register 16	ISSR16	8	H'FEFC	PORT	8	2
IRQ sense port select register	ISSR	8	H'FEFD	PORT	8	2
Peripheral clock select register	PCSR	8	H'FF82	PWM	8	2
Standby control register	SBYCR	8	H'FF84	SYSTEM	8	2
Low power control register	LPWRCR	8	H'FF85	SYSTEM	8	2
Module stop control register H	MSTPCRH	8	H'FF86	SYSTEM	8	2
Module stop control register L	MSTPCRL	8	H'FF87	SYSTEM	8	2
I^2C bus control register_1	ICCR_1	8	H'FF88	IIC_1	8	2
I^2C bus status register_1	ICSR_1	8	H'FF89	IIC_1	8	2
I^2C bus data register_1	ICDR_1	8	H'FF8E	IIC_1	8	2

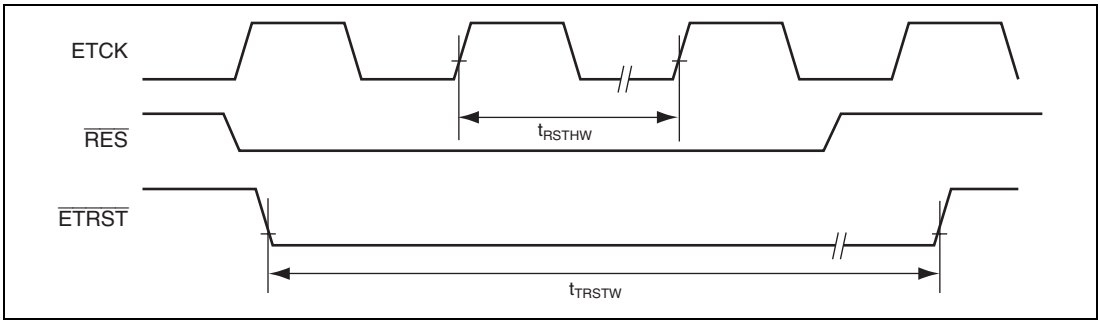

Figure 24.21 Reset Hold Timing

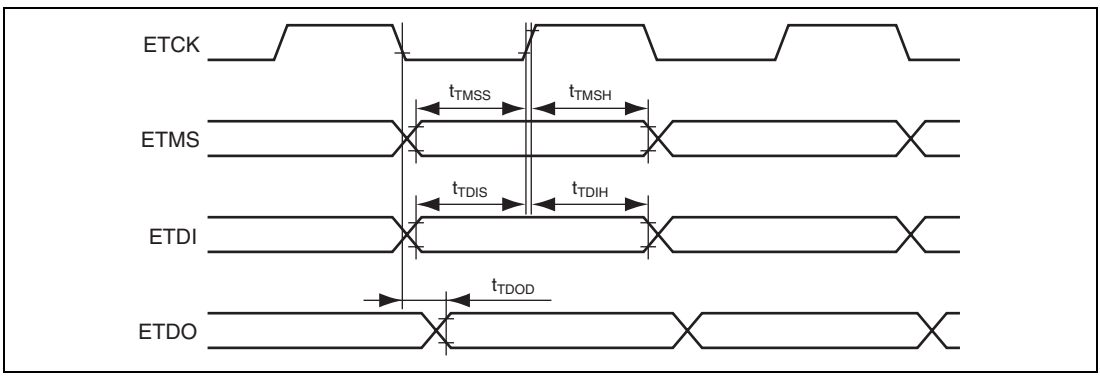

Figure 24.22 JTAG Input/Output Timing