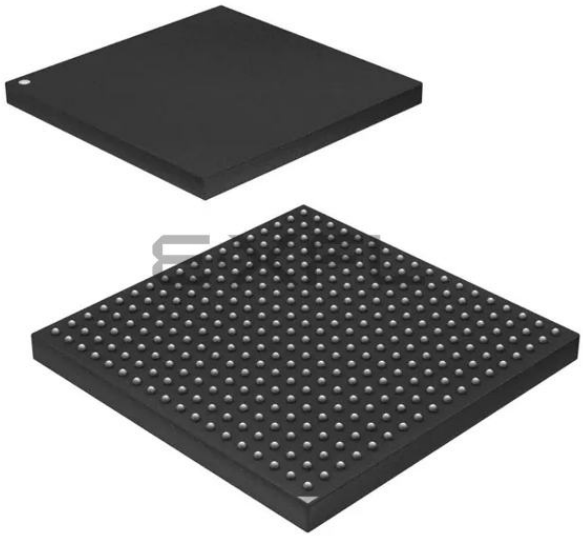
Microchip Technology - AT91SAM9263B-CU-100 Datasheet



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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM926EJ-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	200MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM, SRAM
Graphics Acceleration	Yes
Display & Interface Controllers	LCD
Ethernet	10/100Mbps
SATA	-
USB	USB 2.0 (2)
Voltage - I/O	1.8V, 2.0V, 2.5V, 2.7V, 3.0V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	-
Package / Case	324-TFBGA
Supplier Device Package	324-TFBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at91sam9263b-cu-100

1. Features

- Incorporates the ARM926EJ-S™ ARM® Thumb® Processor
  - DSP Instruction Extensions, Jazelle® Technology for Java® Acceleration
  - 16 Kbyte Data Cache, 16 Kbyte Instruction Cache, Write Buffer
  - 220 MIPS at 200 MHz
  - Memory Management Unit
  - EmbeddedICE™, Debug Communication Channel Support
  - Mid-level Implementation Embedded Trace Macrocell™
- Bus Matrix
  - Nine 32-bit-layer Matrix, Allowing a Total of 28.8 Gbps of On-chip Bus Bandwidth
  - Boot Mode Select Option, Remap Command
- Embedded Memories
  - One 128 Kbyte Internal ROM, Single-cycle Access at Maximum Bus Matrix Speed
  - One 80 Kbyte Internal SRAM, Single-cycle Access at Maximum Processor or Bus Matrix Speed
  - One 16 Kbyte Internal SRAM, Single-cycle Access at Maximum Bus Matrix Speed
- Dual External Bus Interface (EBI0 and EBI1)
  - EBI0 Supports SDRAM, Static Memory, ECC-enabled NAND Flash and CompactFlash®
  - EBI1 Supports SDRAM, Static Memory and ECC-enabled NAND Flash
- DMA Controller (DMAC)
  - Acts as one Bus Matrix Master
  - Embeds 2 Unidirectional Channels with Programmable Priority, Address Generation, Channel Buffering and Control
- Twenty Peripheral DMA Controller Channels (PDC)
- LCD Controller
  - Supports Passive or Active Displays
  - Up to 24 bits per Pixel in TFT Mode, Up to 16 bits per Pixel in STN Color Mode
  - Up to 16M Colors in TFT Mode, Resolution Up to 2048x2048, Supports Virtual Screen Buffers
- Two D Graphics Accelerator
  - Line Draw, Block Transfer, Clipping, Commands Queuing
- Image Sensor Interface
  - ITU-R BT. 601/656 External Interface, Programmable Frame Capture Rate
  - 12-bit Data Interface for Support of High Sensibility Sensors
  - SAV and EAV Synchronization, Preview Path with Scaler, YCbCr Format
- USB 2.0 Full Speed (12 Mbits per second) Host Double Port
  - Dual On-chip Transceivers
  - Integrated FIFOs and Dedicated DMA Channels
- USB 2.0 Full Speed (12 Mbits per second) Device Port
  - On-chip Transceiver, 2,432-byte Configurable Integrated DPRAM
- Ethernet MAC 10/100 Base-T
  - Media Independent Interface or Reduced Media Independent Interface
  - 28-byte FIFOs and Dedicated DMA Channels for Receive and Transmit
- Fully-featured System Controller, including
  - Reset Controller, Shutdown Controller
  - Twenty 32-bit Battery Backup Registers for a Total of 80 Bytes
  - Clock Generator and Power Management Controller
  - Advanced Interrupt Controller and Debug Unit
  - Periodic Interval Timer, Watchdog Timer and Double Real-time Timer
- Reset Controller (RSTC)
  - Based on Two Power-on Reset Cells, Reset Source Identification and Reset Output Control
- Shutdown Controller (SHDWC)
  - Programmable Shutdown Pin Control and Wake-up Circuitry
- Clock Generator (CKGR)
  - 32768Hz Low-power Oscillator on Battery Backup Power Supply, Providing a Permanent Slow Clock

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Comments
CompactFlash Support				
EBI0_CFCE1 - EBI0_CFCE2	CompactFlash Chip Enable	Output	Low	
EBI0_CFOE	CompactFlash Output Enable	Output	Low	
EBI0_CFWE	CompactFlash Write Enable	Output	Low	
EBI0_CFIOR	CompactFlash IO Read	Output	Low	
EBI0_CFIOW	CompactFlash IO Write	Output	Low	
EBI0_CFRNW	CompactFlash Read Not Write	Output		
EBI0_CFCS0 - EBI0_CFCS1	CompactFlash Chip Select Lines	Output	Low	
NAND Flash Support				
EBIx_NANDCS	NAND Flash Chip Select	Output	Low	
EBIx_NANDOE	NAND Flash Output Enable	Output	Low	
EBIx_NANDWE	NAND Flash Write Enable	Output	Low	
SDRAM Controller				
EBIx_SDCK	SDRAM Clock	Output		
EBIx_SDCKE	SDRAM Clock Enable	Output	High	
EBIx_SDCS	SDRAM Controller Chip Select	Output	Low	
EBIx_BA0 - EBIx_BA1	Bank Select	Output		
EBIx_SDWE	SDRAM Write Enable	Output	Low	
EBIx_RAS - EBIx_CAS	Row and Column Signal	Output	Low	
EBIx_SDA10	SDRAM Address 10 Line	Output		
Multimedia Card Interface				
MCIx_CK	Multimedia Card Clock	Output		
MCIx_CDA	Multimedia Card Slot A Command	I/O		
MCIx_CDB	Multimedia Card Slot B Command	I/O		
MCIx_DA0 - MCIx_DA3	Multimedia Card Slot A Data	I/O		
MCIx_DB0 - MCIx_DB3	Multimedia Card Slot B Data	I/O		
Universal Synchronous Asynchronous Receiver Transmitter USART				
SCKx	USARTx Serial Clock	I/O		
TXDx	USARTx Transmit Data	I/O		
RXDx	USARTx Receive Data	Input		
RTSx	USARTx Request To Send	Output		
CTSx	USARTx Clear To Send	Input		
Synchronous Serial Controller SSC				
TDx	SSCx Transmit Data	Output		
RDx	SSCx Receive Data	Input		
TKx	SSCx Transmit Clock	I/O		

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Comments
Ethernet 10/100				
ETXCK	Transmit Clock or Reference Clock	Input		MII only, REFCK in RMII
ERXCK	Receive Clock	Input		MII only
ETXEN	Transmit Enable	Output		
ETX0-ETX3	Transmit Data	Output		ETX0-ETX1 only in RMII
ETXER	Transmit Coding Error	Output		MII only
ERXDV	Receive Data Valid	Input		RXDV in MII, CRSDV in RMII
ERX0-ERX3	Receive Data	Input		ERX0-ERX1 only in RMII
ERXER	Receive Error	Input		
ECRS	Carrier Sense and Data Valid	Input		MII only
ECOL	Collision Detect	Input		MII only
EMDC	Management Data Clock	Output		
EMDIO	Management Data Input/Output	I/O		
EF100	Force 100Mbit/sec.	Output	High	RMII only
USB Device Port				
DDM	USB Device Port Data -	Analog		
DDP	USB Device Port Data +	Analog		
USB Host Port				
HDPA	USB Host Port A Data +	Analog		
HDMA	USB Host Port A Data -	Analog		
HDPB	USB Host Port B Data +	Analog		
HDMB	USB Host Port B Data -	Analog		
Image Sensor Interface - ISI				
ISI_D0-ISI_D11	Image Sensor Data	Input		
ISI_MCK	Image Sensor Reference Clock	Output		Provided by PCK3
ISI_HSYNC	Image Sensor Horizontal Synchro	Input		
ISI_VSYNC	Image Sensor Vertical Synchro	Input		
ISI_PCK	Image Sensor Data Clock	Input		

4. Package and Pinout

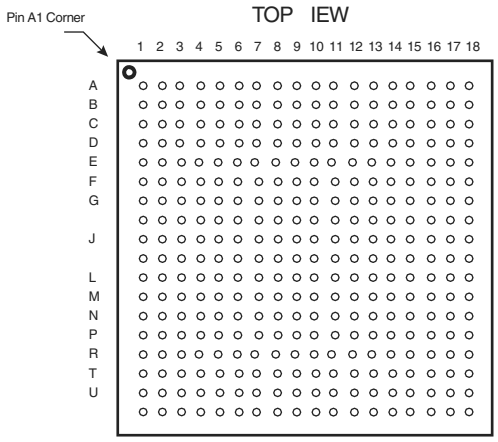
The AT91SAM9263 is available in a 324-ball TFBGA Green package, 15 x 15 mm, 0.8mm ball pitch.

4.1 324-ball TFBGA Package Outline

Figure 4-1 shows the orientation of the 324-ball TFBGA package.

A detailed mechanical description is given in the section “AT91SAM9263 Mechanical Characteristics” in the product datasheet.

Figure 4-1. 324-ball TFBGA Pinout (Top View)



4.2 324-ball TFBGA Package Pinout

Table 4-1. AT91SAM9263 Pinout for 324-ball TFBGA Package

Pin	Signal Name
A1	EBI0_D2
A2	EBI0_SDCKE
A3	EBI0_NWE_NWR0
A4	EBI0_NCS1_SDCS
A5	EBI0_A19
A6	EBI0_A11
A7	EBI0_A10
A8	EBI0_A5
A9	EBI0_A1_NBS2_NWR2
A10	PD4
A11	PC30
A12	PC26
A13	PC24
A14	PC19
A15	PC12
A16	VDDCORE
A17	VDDIOP0
A18	DDP
B1	EBI0_D4
B2	EBI0_NANDOE
B3	EBI0_CAS
B4	EBI0_RAS
B5	EBI0_NBS3_NWR3
B6	EBI0_A22
B7	EBI0_A15
B8	EBI0_A7
B9	EBI0_A4
B10	PD0
B11	PC28
B12	PC21
B13	PC17
B14	PC9
B15	PC7
B16	PC5
B17	PB16
B18	DDM
C1	EBI0_D6
C2	EBI0_D0
C3	EBI0_NANDWE
C4	EBI0_SDWE
C5	EBI0_SDCK
C6	EBI0_A21
C7	EBI0_A13
C8	EBI0_A8
C9	EBI0_A3
C10	PD2
C11	PC29
C12	PC23
C13	PC14
C14	PC8
C15	PC3
E10	PC31
E11	PC22
E12	PC15
E13	PC11
E14	PC4
E15	PB30
E16	PC0
E17	PB31
E18	HDPA
F1	PD7
F2	EBI0_D13
F3	EBI0_D9
F4	EBI0_D11
F5	EBI0_D12
F6	EBI0_NCS0
F7	EBI0_A16_BA0
F8	EBI0_A12
F9	EBI0_A6
F10	PD3
F11	PC27
F12	PC18
F13	PC13
F14	PB26
F15	PB25
F16	PB29
F17	PB27
F18	HDMA
G1	PD17
G2	PD12
G3	PD6
G4	EBI0_D14
G5	PD5
G6	PD8
G7	PD10
G8	GND
G9	NC(1)
G10	GND
G11	GND
G12	GND
G13	PB21
G14	PB20
G15	PB23
G16	PB28
G17	PB22
G18	PB18
H1	PD24
H2	PD13
H3	PD15
H4	PD9
H5	PD11
H6	PD14
K1	PE6
K2	PD28
K3	PE0
K4	PE1
K5	PD27
K6	PD31
K7	PD29
K8	PD25
K9	GND
K10	VDDIOM0
K11	GND
K12	VDDIOM0
K13	PB3/BMS
K14	PA14
K15	PA15
K16	PB1
K17	PB0
K18	PB2
L1	PE10
L2	PE4
L3	PE9
L4	PE7
L5	PE5
L6	PE2
L7	PE3
L8	VDDIOP1
L9	VDDIOM1
L10	VDDIOM0
L11	VDDIOP0
L12	GNDBU
L13	PA13
L14	PB4
L15	PA9
L16	PA12
L17	PA10
L18	PA11
M1	PE18
M2	PE14
M3	PE15
M4	PE11
M5	PE13
M6	PE12
M7	PE8
M8	VDDBU
M9	EBI1_A21
M10	VDDIOM1
M11	GND
M12	GND
M13	VDDIOM1
M14	PA6
M15	PA4
P10	EBI1_NCS0
P11	EBI1_NWE_NWR0
P12	EBI1_D4
P13	EBI1_D10
P14	PA3
P15	PA2
P16	PE28
P17	TDI
P18	PLLRCB
R1	XOUT32
R2	TST
R3	PA18
R4	PA25
R5	PA30
R6	EBI1_A2
R7	EBI1_A14
R8	EBI1_A13
R9	EBI1_A17_BA1
R10	EBI1_D1
R11	EBI1_D8
R12	EBI1_D12
R13	EBI1_D15
R14	PE26
R15	EBI1_SDCK
R16	PE30
R17	TCK
R18	XOUT
T1	VDDOSC
T2	VDDIOM1
T3	PA19
T4	PA21
T5	PA26
T6	PA31
T7	EBI1_A7
T8	EBI1_A12
T9	EBI1_A18
T10	EBI1_D0
T11	EBI1_D7
T12	EBI1_D14
T13	PE23
T14	PE25
T15	PE29
T16	PE31
T17	GNDPLL
T18	XIN
U1	PA17
U2	PA20
U3	PA23
U4	PA24
U5	PA28
U6	EBI1_A0_NBS0

5. Power Considerations

5.1 Power Supplies

AT91SAM9263 has several types of power supply pins:

- VDDCORE pins: Power the core, including the processor, the embedded memories and the peripherals; voltage ranges from 1.08V to 1.32V, 1.2V nominal.
- VDDIOM0 and VDDIOM1 pins: Power the External Bus Interface 0 I/O lines and the External Bus Interface 1 I/O lines, respectively; voltage ranges between 1.65V and 1.95V (1.8V nominal) or between 3.0V and 3.6V (3.3V nominal).
- VDDIOP0 pins: Power the Peripheral I/O lines and the USB transceivers; voltage ranges from 2.7V to 3.6V, 3.3V nominal.
- VDDIOP1 pins: Power the Peripheral I/O lines involving the Image Sensor Interface; voltage ranges from 1.65V to 3.6V, 1.8V, 2.5V, 3V or 3.3V nominal.
- VDDBU pin: Powers the Slow Clock oscillator and a part of the System Controller; voltage ranges from 1.08V to 1.32V, 1.2V nominal.
- VDDPLL pin: Powers the PLL cells; voltage ranges from 3.0V to 3.6V, 3.3V nominal.
- VDDOSC pin: Powers the Main Oscillator cells; voltage ranges from 3.0V to 3.6V, L3.3V nominal.

The power supplies VDDIOM0, VDDIOM1 and VDDIOP0, VDDIOP1 are identified in the pinout table and the multiplexing tables. These supplies enable the user to power the device differently for interfacing with memories and for interfacing with peripherals.

Ground pins GND are common to VDDOSC, VDDCORE, VDDIOM0, VDDIOM1, VDDIOP0 and VDDIOP1 pins power supplies. Separated ground pins are provided for VDDBU and VDDPLL. These ground pins are respectively GNDBU and GNDPLL.

5.2 Power Consumption

The AT91SAM9263 consumes about 700 µA (worst case) of static current on VDDCORE at 25°C. This static current rises at up to 7 mA if the temperature increases to 85°C.

On VDDBU, the current does not exceed 3 µA @25°C, but can rise at up to 20 µA @85°C. An automatic switch to VDDCORE guarantees low power consumption on the battery when the system is on.

For dynamic power consumption, the AT91SAM9263 consumes a maximum of 70 mA on VDDCORE at maximum conditions (1.2V, 25°C, processor running full-performance algorithm).

5.3 Programmable I/O Lines Power Supplies

The power supply pins VDDIOM0 and VDDIOM1 accept two voltage ranges. This allows the device to reach its maximum speed, either out of 1.8V or 3.0V external memories.

The maximum speed is 100 MHz on the pin SDCK (SDRAM Clock) loaded with 10 pF. The other signals (control, address and data signals) do not go over 50 MHz, loaded with 30 pF for power supply at 1.8V and 50 pF for power supply at 3.3V.

The voltage ranges are determined by programming registers in the Chip Configuration registers located in the Matrix User Interface.

At reset, the selected voltage defaults to 3.3V nominal and power supply pins can accept either 1.8V or 3.3V. However, the device cannot reach its maximum speed if the voltage supplied to the pins is only 1.8V without reprogramming the EBI0 voltage range. The user must be sure to program the EBI0 voltage range before getting the device out of its Slow Clock Mode.

6. I/O Line Considerations

6.1 JTAG Port Pins

TMS, TDI and TCK are Schmitt trigger inputs and have no pull-up resistors.

TDO and RTCK are outputs, driven at up to VDDIOP0, and have no pull-up resistors.

The JTAGSEL pin is used to select the JTAG boundary scan when asserted at a high level (VDDBU). It integrates a permanent pull-down resistor of about 15 kΩ to GNDBU, so that it can be left unconnected for normal operations.

The NTRST signal is described in Section 6.3.

All JTAG signals except JTAGSEL (VDDBU) are supplied with VDDIOP0.

6.2 Test Pin

The TST pin is used for manufacturing test purposes when asserted high. It integrates a permanent pull-down resistor of about 15 kΩ to GNDBU, so that it can be left unconnected for normal operations. Driving this line at a high level leads to unpredictable results.

This pin is supplied with VDDBU.

6.3 Reset Pins

NRST is an open-drain output integrating a non-programmable pull-up resistor. It can be driven with voltage at up to VDDIOP0.

NTRST is an input which allows reset of the JTAG Test Access port. It has no action on the processor.

As the product integrates power-on reset cells, which manage the processor and the JTAG reset, the NRST and NTRST pins can be left unconnected.

The NRST and NTRST pins both integrate a permanent pull-up resistor of 100 kΩ minimum to VDDIOP0.

The NRST signal is inserted in the Boundary Scan.

6.4 PIO Controllers

All the I/O lines managed by the PIO Controllers integrate a programmable pull-up resistor of 100 kΩ typical. Programming of this pull-up resistor is performed independently for each I/O line through the PIO Controllers.

After reset, all the I/O lines default as inputs with pull-up resistors enabled, except those which are multiplexed with the External Bus Interface signals that require to be enabled as Peripheral at reset. This is explicitly indicated in the column “Reset State” of the PIO Controller multiplexing tables on page 33 and following.

6.5 Shutdown Logic Pins

The SHDN pin is a tri-state output only pin, which is driven by the Shutdown Controller. There is no internal pull-up. An external pull-up to VDDBU is needed and its value must be higher than 1 MΩ. The resistor value is calculated according to the regulator enable implementation and the SHDN level.

The pin WKUP is an input-only. It can accept voltages only between 0V and VDDBU.

- SPI1 Transmit Channel
- SPI0 Transmit Channel
- SSC1 Transmit Channel
- SSC0 Transmit Channel
- DBGU Receive Channel
- USART2 Receive Channel
- USART1 Receive Channel
- USART0 Receive Channel
- AC97 Receive Channel
- SPI1 Receive Channel
- SPI0 Receive Channel
- SSC1 Receive Channel
- SSC0 Receive Channel
- MCI1 Transmit/Receive Channel
- MCI0 Transmit/Receive Channel

7.7 DMA Controller

- Acts as one Matrix Master
- Embeds 2 unidirectional channels with programmable priority
- Address Generation
  - Source/destination address programming
  - Address increment, decrement or no change
  - DMA chaining support for multiple non-contiguous data blocks through use of linked lists
  - Scatter support for placing fields into a system memory area from a contiguous transfer. Writing a stream of data into non-contiguous fields in system memory.
  - Gather support for extracting fields from a system memory area into a contiguous transfer
  - User enabled auto-reloading of source, destination and control registers from initially programmed values at the end of a block transfer
  - Auto-loading of source, destination and control registers from system memory at end of block transfer in block chaining mode
  - Unaligned system address to data transfer width supported in hardware
- Channel Buffering
  - Two 8-word FIFOs
  - Automatic packing/unpacking of data to fit FIFO width
- Channel Control
  - Programmable multiple transaction size for each channel
  - Support for cleanly disabling a channel without data loss
  - Suspend DMA operation
  - Programmable DMA lock transfer support.
- Transfer Initiation
  - Supports four external DMA Requests
  - Support for software handshaking interface. Memory mapped registers can be used to control the flow of a DMA transfer in place of a hardware handshaking interface
- Interrupt
  - Programmable interrupt generation on DMA transfer completion, Block transfer completion, Single/Multiple transaction completion or Error condition

7.8 Debug and Test Features

- ARM926 Real-time In-circuit Emulator
  - Two real-time Watchpoint Units
  - Two Independent Registers: Debug Control Register and Debug Status Register
  - Test Access Port Accessible through JTAG Protocol
  - Debug Communications Channel
- Debug Unit
  - Two-pin UART
  - Debug Communication Channel Interrupt Handling
  - Chip ID Register
- Embedded Trace Macrocell: ETM9™
  - Medium+ Level Implementation
  - Half-rate Clock Mode
  - Four Pairs of Address Comparators
  - Two Data Comparators
  - Eight Memory Map Decoder Inputs
  - Two 16-bit Counters
  - One 3-stage Sequencer
  - One 45-byte FIFO
- IEEE1149.1 JTAG Boundary-scan on All Digital Pins

REMAP allows the user to layout the internal SRAM bank to 0x0. This is done by software once the system has booted. Refer to the section “AT91SAM9263 Bus Matrix” in the product datasheet for more details.

When REMAP = 0, BMS allows the user to layout at address 0x0 either the ROM or an external memory. This is done via hardware at reset.

Note: Memory blocks not affected by these parameters can always be seen at their specified base addresses. See the complete memory map presented in Figure 8-1 on page 20.

The AT91SAM9263 Bus Matrix manages a boot memory that depends on the level on the pin BMS at reset. The internal memory area mapped between address 0x0 and 0x000F FFFF is reserved to this effect.

If BMS is detected at 1, the boot memory is the embedded ROM.

If BMS is detected at 0, the boot memory is the memory connected on the Chip Select 0 of the External Bus Interface.

8.1.2.1 BMS = 1, Boot on Embedded ROM

The system boots on Boot Program.

- Boot at slow clock
- Auto baudrate detection
- Downloads and runs an application from external storage media into internal SRAM
- Downloaded code size depends on embedded SRAM size
- Automatic detection of valid application
- Bootloader on a non-volatile memory
  - SD Card
  - NAND Flash
  - SPI DataFlash® and Serial Flash connected on NPCS0 of the SPI0
- Interface with SAM-BA® Graphic User Interface to enable code loading via:
  - Serial communication on a DBGU
  - USB Bulk Device Port

8.1.2.2 BMS = 0, Boot on External Memory

- Boot at slow clock
- Boot with the default configuration for the Static Memory Controller, byte select mode, 16-bit data bus, Read/Write controlled by Chip Select, allows boot on 16-bit non-volatile memory.

The customer-programmed software must perform a complete configuration.

To speed up the boot sequence when booting at 32 kHz EBI0 CS0 (BMS=0) the user must:

1. Program the PMC (main oscillator enable or bypass mode).
2. Program and Start the PLL.
3. Reprogram the SMC setup, cycle, hold, mode timings registers for CS0 to adapt them to the new clock.
4. Switch the main clock to the new value.

8.2 External Memories

The external memories are accessed through the External Bus Interfaces 0 and 1. Each Chip Select line has a 256 Mbyte memory area assigned.

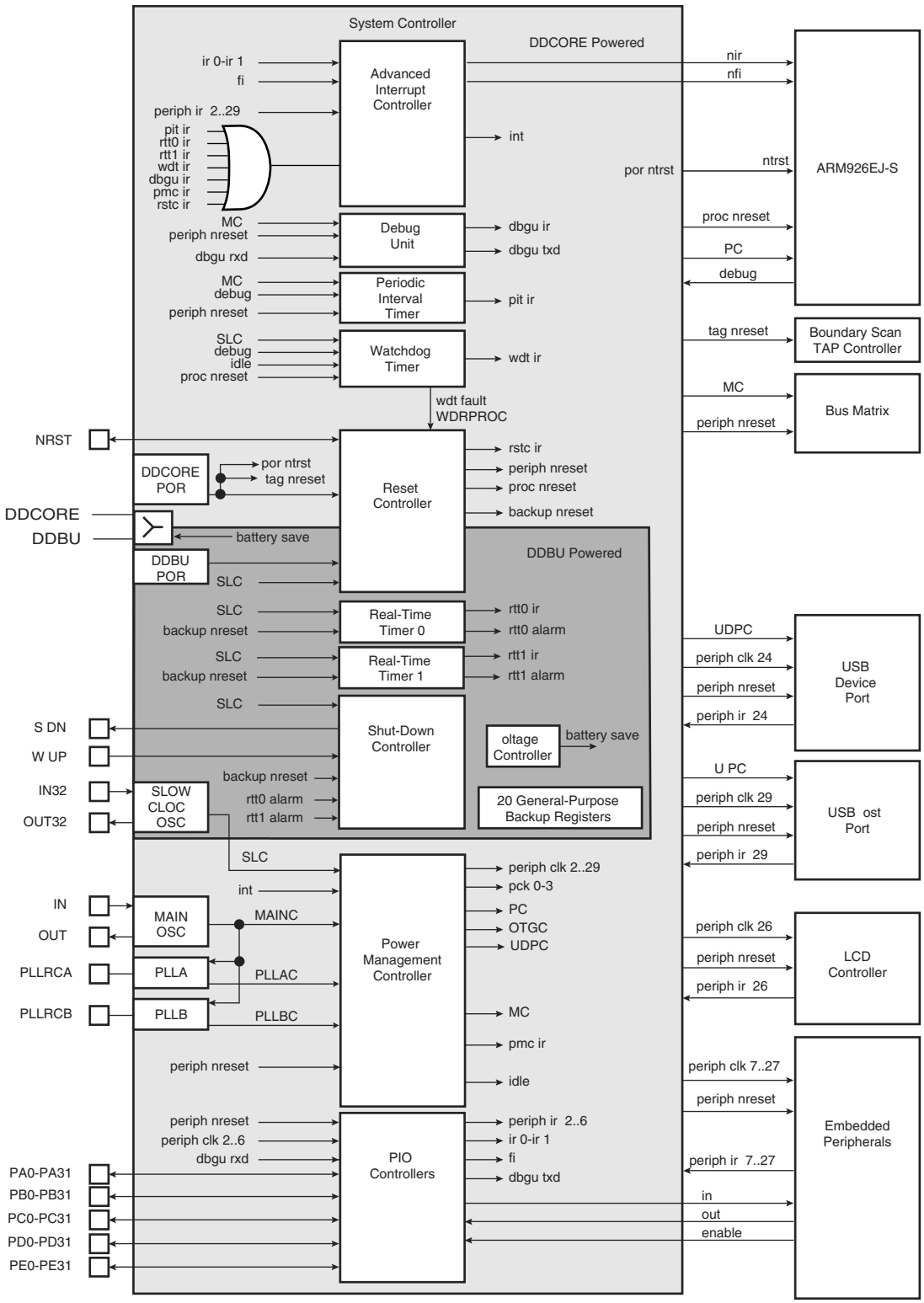
Refer to Figure 8-1 on page 20.

8.2.1 External Bus Interfaces

The AT91SAM9263 features two External Bus Interfaces to offer more bandwidth to the system and to prevent bottlenecks while accessing external memories.

9.1 System Controller Block Diagram

Figure 9-1. AT91SAM9263 System Controller Block Diagram



10.2.1 Peripheral Interrupts and Clock Control

10.2.1.1 System Interrupt

The System Interrupt in Source 1 is the wired-OR of the interrupt signals coming from:

- the SDRAM Controller
- the Debug Unit
- the Periodic Interval Timer
- the Real-Time Timer
- the Watchdog Timer
- the Reset Controller
- the Power Management Controller

The clock of these peripherals cannot be deactivated and Peripheral ID 1 can only be used within the Advanced Interrupt Controller.

10.2.1.2 External Interrupts

All external interrupt signals, i.e., the Fast Interrupt signal FIQ or the Interrupt signals IRQ0 to IRQ1, use a dedicated Peripheral ID. However, there is no clock control associated with these peripheral IDs.

10.2.1.3 Timer Counter Interrupts

The three Timer Counter channels interrupt signals are OR-wired together to provide the interrupt source 19 of the Advanced Interrupt Controller. This forces the programmer to read all Timer Counter status registers before branching the right Interrupt Service Routine.

The Timer Counter channels clocks cannot be deactivated independently. Switching off the clock of the Peripheral 19 disables the clock of the 3 channels.

10.3 Peripherals Signals Multiplexing on I/O Lines

The AT91SAM9263 device features 5 PIO controllers, PIOA, PIOB, PIOC, PIOD and PIOE, which multiplex the I/O lines of the peripheral set.

Each PIO Controller controls up to 32 lines. Each line can be assigned to one of two peripheral functions, A or B. The multiplexing tables define how the I/O lines of the peripherals A and B are multiplexed on the PIO Controllers. The two columns “Function” and “Comments” have been inserted in this table for the user’s own comments; they may be used to track how pins are defined in an application.

Note that some peripheral functions which are output only may be duplicated within both tables.

The column “Reset State” indicates whether the PIO Line resets in I/O mode or in peripheral mode. If I/O is specified, the PIO Line resets in input with the pull-up enabled, so that the device is maintained in a static state as soon as the reset is released. As a result, the bit corresponding to the PIO Line in the register PIO_PSR (Peripheral Status Register) resets low.

If a signal name is specified in the “Reset State” column, the PIO Line is assigned to this function and the corresponding bit in PIO_PSR resets high. This is the case of pins controlling memories, in particular the address lines, which require the pin to be driven as soon as the reset is released. Note that the pull-up resistor is also enabled in this case.

10.3.2 PIO Controller B Multiplexing

Table 10-3. Multiplexing on PIO Controller B

PIO Controller B					Application Usage	
I/O Line	Peripheral A	Peripheral B	Reset State	Power Supply	Function	Comments
PB0	AC97FS	TF0	I/O	VDDIOP0		
PB1	AC97CK	TK0	I/O	VDDIOP0		
PB2	AC97TX	TD0	I/O	VDDIOP0		
PB3	AC97RX	RD0	I/O	VDDIOP0		
PB4	TWD	RK0	I/O	VDDIOP0		
PB5	TWCK	RF0	I/O	VDDIOP0		
PB6	TF1	DMARQ1	I/O	VDDIOP0		
PB7	TK1	PWM0	I/O	VDDIOP0		
PB8	TD1	PWM1	I/O	VDDIOP0		
PB9	RD1	LCDCC	I/O	VDDIOP0		
PB10	RK1	PCK1	I/O	VDDIOP0		
PB11	RF1	SPI0_NPCS3	I/O	VDDIOP0		
PB12	SPI1_MISO		I/O	VDDIOP0		
PB13	SPI1_MOSI		I/O	VDDIOP0		
PB14	SPI1_SPCK		I/O	VDDIOP0		
PB15	SPI1_NPCS0		I/O	VDDIOP0		
PB16	SPI1_NPCS1	PCK1	I/O	VDDIOP0		
PB17	SPI1_NPCS2	TIOA2	I/O	VDDIOP0		
PB18	SPI1_NPCS3	TIOB2	I/O	VDDIOP0		
PB19			I/O	VDDIOP0		
PB20			I/O	VDDIOP0		
PB21			I/O	VDDIOP0		
PB22			I/O	VDDIOP0		
PB23			I/O	VDDIOP0		
PB24		DMARQ3	I/O	VDDIOP0		
PB25			I/O	VDDIOP0		
PB26			I/O	VDDIOP0		
PB27		PWM2	I/O	VDDIOP0		
PB28		TCLK0	I/O	VDDIOP0		
PB29		PWM3	I/O	VDDIOP0		
PB30			I/O	VDDIOP0		
PB31			I/O	VDDIOP0		

10.3.4 PIO Controller D Multiplexing

Table 10-5. Multiplexing on PIO Controller D

PIO Controller D					Application Usage	
I/O Line	Peripheral A	Peripheral B	Reset State	Power Supply	Function	Comments
PD0	TXD1	SPI0_NPCS2	I/O	VDDIOP0		
PD1	RXD1	SPI0_NPCS3	I/O	VDDIOP0		
PD2	TXD2	SPI1_NPCS2	I/O	VDDIOP0		
PD3	RXD2	SPI1_NPCS3	I/O	VDDIOP0		
PD4	FIQ	DMARQ2	I/O	VDDIOP0		
PD5	EBI0_NWAIT	RTS2	I/O	VDDIOM0		
PD6	EBI0_NCS4/CFCS0	CTS2	I/O	VDDIOM0		
PD7	EBI0_NCS5/CFCS1	RTS1	I/O	VDDIOM0		
PD8	EBI0_CFCE1	CTS1	I/O	VDDIOM0		
PD9	EBI0_CFCE2	SCK2	I/O	VDDIOM0		
PD10		SCK1	I/O	VDDIOM0		
PD11	EBI0_NCS2	TSYNC	I/O	VDDIOM0		
PD12	EBI0_A23	TCLK	A23	VDDIOM0		
PD13	EBI0_A24	TPS0	A24	VDDIOM0		
PD14	EBI0_A25_CFRNW	TPS1	A25	VDDIOM0		
PD15	EBI0_NCS3/NANDCS	TPS2	I/O	VDDIOM0		
PD16	EBI0_D16	TPK0	I/O	VDDIOM0		
PD17	EBI0_D17	TPK1	I/O	VDDIOM0		
PD18	EBI0_D18	TPK2	I/O	VDDIOM0		
PD19	EBI0_D19	TPK3	I/O	VDDIOM0		
PD20	EBI0_D20	TPK4	I/O	VDDIOM0		
PD21	EBI0_D21	TPK5	I/O	VDDIOM0		
PD22	EBI0_D22	TPK6	I/O	VDDIOM0		
PD23	EBI0_D23	TPK7	I/O	VDDIOM0		
PD24	EBI0_D24	TPK8	I/O	VDDIOM0		
PD25	EBI0_D25	TPK9	I/O	VDDIOM0		
PD26	EBI0_D26	TPK10	I/O	VDDIOM0		
PD27	EBI0_D27	TPK11	I/O	VDDIOM0		
PD28	EBI0_D28	TPK12	I/O	VDDIOM0		
PD29	EBI0_D29	TPK13	I/O	VDDIOM0		
PD30	EBI0_D30	TPK14	I/O	VDDIOM0		
PD31	EBI0_D31	TPK15	I/O	VDDIOM0		

10.4 System Resource Multiplexing

10.4.1 LCD Controller

The LCD Controller can interface with several LCD panels. It supports 4 bits per pixel (bpp), 8 bpp or 16 bpp without limitation. Interfacing 24 bpp TFT panels prevents using the Ethernet MAC. 16 bpp TFT panels are interfaced through peripheral B functions, as color data is output on LCDD3 to LCDD7, LCDD11 to LCDD15 and LCDD19 to LCDD23. Intensity bit is output on LCDD10. Using the peripheral B does not prevent using MAC lines. 16 bpp STN panels are interfaced through peripheral A and color data is output on LCDD0 to LCDD15, thus MAC lines can be used on peripheral B.

Mapping the LCD signals on peripheral A and peripheral B makes is possible to use 24 bpp TFT panels in 24 bits (peripheral A) or 16 bits (peripheral B) by reprogramming the PIO controller and thus without hardware modification.

10.4.2 ETM™

Using the ETM prevents the use of the EBI0 in 32-bit mode. Only 16-bit mode (EBI0_D0 to EBI0_D15) is available, makes EBI0 unable to interface CompactFlash and NAND Flash cards, reduces EBI0's address bus width which makes it unable to address memory ranges bigger than 0x7FFFFF and finally it makes impossible to use EBI0_NCS2 and EBI0_NCS3.

10.4.3 EBI1

Using the following features prevents using EBI1 in 32-bit mode:

- the second slots of MCI0 and/or MCI1
- USART0
- DMA request 0 (DMARQ0)

10.4.4 Ethernet 10/100MAC

Using the following features of EBI1 prevents using Ethernet 10/100MAC:

- SDRAM
- NAND (unless NANDCS, NANDOE and NANDWE are managed by PIO)
- SMC 32 bits (SMC 16 bits is still available)
- NCS1, NCS2 are not available in SMC mode

10.4.5 SSC

Using SSC0 prevents using the AC97 Controller and Two-wire Interface.

Using SSC1 prevents using DMA Request 1, PWM0, PWM1, LCDCC and PCK1.

10.4.6 USART

Using USART2 prevents using EBI0's NWAIT signal, Chip Select 4 and CompactFlash Chip Enable 2.

Using USART1 prevents using EBI0's Chip Select 5 and CompactFlash Chip Enable1.

10.4.7 NAND Flash

Using the NAND Flash interface on EBI1 prevents using Ethernet MAC.

10.4.8 CompactFlash

Using the CompactFlash interface prevents using NCS4 and/or NCS5 to access other parallel devices.

- Two global registers that act on all three TC Channels

10.5.7 Pulse Width Modulation Controller

- 4 channels, one 16-bit counter per channel
- Common clock generator, providing thirteen different clocks
  - Modulo n counter providing eleven clocks
  - Two independent Linear Dividers working on modulo n counter outputs
- Independent channel programming
  - Independent Enable Disable commands
  - Independent clock selection
  - Independent period and duty cycle, with double bufferization
  - Programmable selection of the output waveform polarity
  - Programmable center or left aligned output waveform

10.5.8 Multimedia Card Interface

- Two double-channel Multimedia Card Interfaces, allowing concurrent transfers with 2 cards
- Compatibility with MultiMediaCard Specification Version 3.31
- Compatibility with SD Memory Card Specification Version 1.0
- Compatibility with SDIO Specification Version V1.1
- Cards clock rate up to Master Clock divided by 2
- Embedded power management to slow down clock rate when not used
- Each MCI has two slots, each supporting
  - One slot for one MultiMediaCard bus (up to 30 cards) or
  - One SD Memory Card
- Support for stream, block and multi-block data read and write

10.5.9 CAN Controller

- Fully compliant with 16-mailbox CAN 2.0A and 2.0B CAN Controllers
- Bit rates up to 1Mbit/s.
- Object-oriented mailboxes, each with the following properties:
  - CAN Specification 2.0 Part A or 2.0 Part B programmable for each message
  - Object Configurable as receive (with overwrite or not) or transmit
  - Local Tag and Mask Filters up to 29-bit Identifier/Channel
  - 32 bits access to Data registers for each mailbox data object
  - Uses a 16-bit time stamp on receive and transmit message
  - Hardware concatenation of ID unmasked bitfields to speedup family ID processing
  - 16-bit internal timer for Time Stamping and Network synchronization
  - Programmable reception buffer length up to 16 mailbox object
  - Priority Management between transmission mailboxes
  - Autobaud and listening mode
  - Low power mode and programmable wake-up on bus activity or by the application
  - Data, Remote, Error and Overload Frame handling

10.5.10 USB Host Port

- Compliant with Open HCI Rev 1.0 Specification
- Compliant with USB V2.0 full-speed and low-speed specification

- Supports both low-speed 1.5 Mbps and full-speed 12 Mbps devices
- Root hub integrated with two downstream USB ports
- Two embedded USB transceivers
- Supports power management
- Operates as a master on the matrix

10.5.11 USB Device Port

- USB V2.0 full-speed compliant, 12 Mbits per second
- Embedded USB V2.0 full-speed transceiver
- Embedded 2,432-byte dual-port RAM for endpoints
- Suspend/Resume logic
- Ping-pong mode (two memory banks) for isochronous and bulk endpoints
- Six general-purpose endpoints
    - Endpoint 0 and 3: 64 bytes, no ping-pong mode
    - Endpoint 1 and 2: 64 bytes, ping-pong mode
    - Endpoint 4 and 5: 512 bytes, ping-pong mode

10.5.12 LCD Controller

- Single and Dual scan color and monochrome passive STN LCD panels supported
- Single scan active TFT LCD panels supported
- 4-bit single scan, 8-bit single or dual scan, 16-bit dual scan STN interfaces supported
- Up to 24-bit single scan TFT interfaces supported
- Up to 16 gray levels for mono STN and up to 4096 colors for color STN displays
- 1, 2 bits per pixel (palletized), 4 bits per pixel (non-palletized) for mono STN
- 1, 2, 4, 8 bits per pixel (palletized), 16 bits per pixel (non-palletized) for color STN
- 1, 2, 4, 8 bits per pixel (palletized), 16, 24 bits per pixel (non-palletized) for TFT
- Single clock domain architecture
- Resolution supported up to 2048x2048
- 2D DMA Controller for management of virtual Frame Buffer
    - Allows management of frame buffer larger than the screen size and moving the view over this virtual frame buffer
- Automatic resynchronization of the frame buffer pointer to prevent flickering

10.5.13 Two D Graphics Controller

- Acts as one Matrix Master
- Commands are passed through the APB User Interface
- Operates directly in the frame buffer of the LCD Controller
    - Line draw
    - Block transfer
    - Clipping
- Commands queuing through a FIFO

10.5.14 Ethernet 10/100 MAC

- Compatibility with IEEE Standard 802.3
- 10 and 100 Mbits per second data throughput capability
- Full- and half-duplex operations
- MII or RMII interface to the physical layer

12. AT91SAM9263 Ordering Information

Table 12-1. AT91SAM9263 Ordering Information

Marketing Revision Level B Ordering Code	Package	Package Type	Temperature Operating Range
AT91SAM9263B-CU	TFBGA 324	Green	Industrial -40°C to 85°C
AT91SAM9263B-CU-100	TFBGA 324	Green	Industrial -40°C to 85°C

Table 13-1. Revision History

Document Ref.	Comments	Change Request Ref.
6249CS	In Section 4.1 “324-ball TFBGA Package Outline” on page 10 corrected package top view.	4463
	All new information for Table 7-1, “List of Bus Matrix Masters,” on page 16, Table 7-2, “List of Bus Matrix Slaves,” on page 16 and Table 7-3, “Masters to Slaves Access,” on page 17.	4466
	In Section 9.3 “Shutdown Controller” on page 27, corrected reference to shutdown pin.	3870
	In Section 5.2 “Power Consumption” on page 13, specified static current consumption as worst case. Corrected Section 10.4.7 “NAND Flash” on page 38, with information on EMAC.	3825
	In Section 10.4.3 “EBI1” on page 38, added Ethernet 10/100 MAC to the System Resource Multiplexing list of EBI1.	4064
	In Section 10.4.11 “Image Sensor Interface” on page 39 and Section 10.4.12 “Timers” on page 39, removed mention of keyboard interfaces.	4407
6249BS	Corrected typo to IDE hard disk in Section “Description” on page 1.	3804
	Corrected ordering code in Section “” on page 46.	3805
6249AS	First issue.	

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