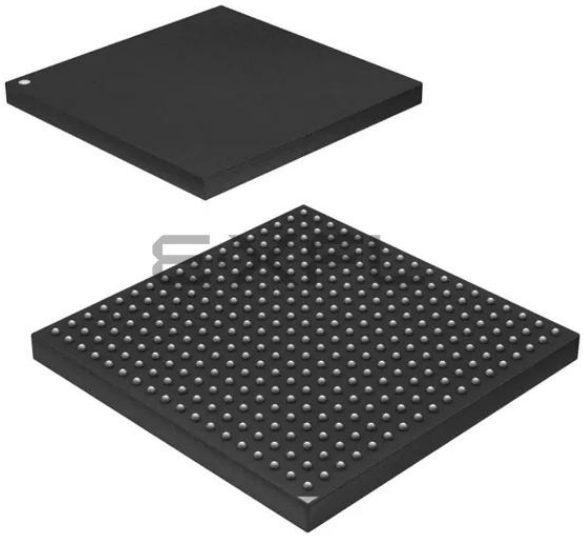
Microchip Technology - AT91SAM9263B-CU-999 Datasheet



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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM926EJ-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	200MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM, SRAM
Graphics Acceleration	Yes
Display & Interface Controllers	LCD
Ethernet	10/100Mbps
SATA	-
USB	USB 2.0 (2)
Voltage - I/O	1.8V, 2.0V, 2.5V, 2.7V, 3.0V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	-
Package / Case	324-TFBGA
Supplier Device Package	324-TFBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at91sam9263b-cu-999

1. Features

- Incorporates the ARM926EJ-S™ ARM® Thumb® Processor
  - DSP Instruction Extensions, Jazelle® Technology for Java® Acceleration
  - 16 Kbyte Data Cache, 16 Kbyte Instruction Cache, Write Buffer
  - 220 MIPS at 200 MHz
  - Memory Management Unit
  - EmbeddedICE™, Debug Communication Channel Support
  - Mid-level Implementation Embedded Trace Macrocell™
- Bus Matrix
  - Nine 32-bit-layer Matrix, Allowing a Total of 28.8 Gbps of On-chip Bus Bandwidth
  - Boot Mode Select Option, Remap Command
- Embedded Memories
  - One 128 Kbyte Internal ROM, Single-cycle Access at Maximum Bus Matrix Speed
  - One 80 Kbyte Internal SRAM, Single-cycle Access at Maximum Processor or Bus Matrix Speed
  - One 16 Kbyte Internal SRAM, Single-cycle Access at Maximum Bus Matrix Speed
- Dual External Bus Interface (EBI0 and EBI1)
  - EBI0 Supports SDRAM, Static Memory, ECC-enabled NAND Flash and CompactFlash®
  - EBI1 Supports SDRAM, Static Memory and ECC-enabled NAND Flash
- DMA Controller (DMAC)
  - Acts as one Bus Matrix Master
  - Embeds 2 Unidirectional Channels with Programmable Priority, Address Generation, Channel Buffering and Control
- Twenty Peripheral DMA Controller Channels (PDC)
- LCD Controller
  - Supports Passive or Active Displays
  - Up to 24 bits per Pixel in TFT Mode, Up to 16 bits per Pixel in STN Color Mode
  - Up to 16M Colors in TFT Mode, Resolution Up to 2048x2048, Supports Virtual Screen Buffers
- Two D Graphics Accelerator
  - Line Draw, Block Transfer, Clipping, Commands Queuing
- Image Sensor Interface
  - ITU-R BT. 601/656 External Interface, Programmable Frame Capture Rate
  - 12-bit Data Interface for Support of High Sensibility Sensors
  - SAV and EAV Synchronization, Preview Path with Scaler, YCbCr Format
- USB 2.0 Full Speed (12 Mbits per second) Host Double Port
  - Dual On-chip Transceivers
  - Integrated FIFOs and Dedicated DMA Channels
- USB 2.0 Full Speed (12 Mbits per second) Device Port
  - On-chip Transceiver, 2,432-byte Configurable Integrated DPRAM
- Ethernet MAC 10/100 Base-T
  - Media Independent Interface or Reduced Media Independent Interface
  - 28-byte FIFOs and Dedicated DMA Channels for Receive and Transmit
- Fully-featured System Controller, including
  - Reset Controller, Shutdown Controller
  - Twenty 32-bit Battery Backup Registers for a Total of 80 Bytes
  - Clock Generator and Power Management Controller
  - Advanced Interrupt Controller and Debug Unit
  - Periodic Interval Timer, Watchdog Timer and Double Real-time Timer
- Reset Controller (RSTC)
  - Based on Two Power-on Reset Cells, Reset Source Identification and Reset Output Control
- Shutdown Controller (SHDWC)
  - Programmable Shutdown Pin Control and Wake-up Circuitry
- Clock Generator (CKGR)
  - 32768Hz Low-power Oscillator on Battery Backup Power Supply, Providing a Permanent Slow Clock

  - 3 to 20 MHz On-chip Oscillator and Two Up to 240 MHz PLLs
- Power Management Controller (PMC)
  - Very Slow Clock Operating Mode, Software Programmable Power Optimization Capabilities
  - Four Programmable External Clock Signals
- Advanced Interrupt Controller (AIC)
  - Individually Maskable, Eight-level Priority, Vectored Interrupt Sources
  - Two External Interrupt Sources and One Fast Interrupt Source, Spurious Interrupt Protected
- Debug Unit (DBGU)
  - 2-wire UART and Support for Debug Communication Channel, Programmable ICE Access Prevention
  - Mode for General Purpose Two-wire UART Serial Communication
- Periodic Interval Timer (PIT)
  - 20-bit Interval Timer plus 12-bit Interval Counter
- Watchdog Timer (WDT)
  - Key-protected, Programmable Only Once, Windowed 16-bit Counter Running at Slow Clock
- Two Real-time Timers (RTT)
  - 32-bit Free-running Backup Counter Running at Slow Clock with 16-bit Prescaler
- Five 32-bit Parallel Input/Output Controllers (PIOA, PIOB, PIOC, PIOD and PIOE)
  - 160 Programmable I/O Lines Multiplexed with Up to Two Peripheral I/Os
  - Input Change Interrupt Capability on Each I/O Line
  - Individually Programmable Open-drain, Pull-up Resistor and Synchronous Output
- One Part 2.0A and Part 2.0B-compliant CAN Controller
  - 16 Fully-programmable Message Object Mailboxes, 16-bit Time Stamp Counter
- Two Multimedia Card Interface (MCI)
  - SDCard/SDIO and MultiMediaCard™ Compliant
  - Automatic Protocol Control and Fast Automatic Data Transfers with PDC
  - Two SDCard Slots Support on eAch Controller
- Two Synchronous Serial Controllers (SSC)
  - Independent Clock and Frame Sync Signals for Each Receiver and Transmitter
  - I²S Analog Interface Support, Time Division Multiplex Support
  - High-speed Continuous Data Stream Capabilities with 32-bit Data Transfer
- One AC97 Controller (AC97C)
  - 6-channel Single AC97 Analog Front End Interface, Slot Assigner
- Three Universal Synchronous/Asynchronous Receiver Transmitters (USART)
  - Individual Baud Rate Generator, IrDA® Infrared Modulation/Demodulation, Manchester Encoding/Decoding
  - Support for ISO7816 T0/T1 Smart Card, Hardware Handshaking, RS485 Support
- Two Master/Slave Serial Peripheral Interface (SPI)
  - 8- to 16-bit Programmable Data Length, Four External Peripheral Chip Selects
- One Three-channel 16-bit Timer/Counters (TC)
  - Three External Clock Inputs, Two Multi-purpose I/O Pins per Channel
  - Double PWM Generation, Capture/Waveform Mode, Up/Down Capability
- One Four-channel 16-bit PWM Controller (PWMC)
- One Two-wire Interface (TWI)
  - Master Mode Support, All Two-wire Atmel® EEPROMs Supported
- IEEE® 1149.1 JTAG Boundary Scan on All Digital Pins
- Required Power Supplies
  - 1.08V to 1.32V for VDDCORE and VDDBU
  - 3.0V to 3.6V for VDDOSC and VDDPLL
  - 2.7V to 3.6V for VDDIOP0 (Peripheral I/Os)
  - 1.65V to 3.6V for VDDIOP1 (Peripheral I/Os)
  - Programmable 1.65V to 1.95V or 3.0V to 3.6V for VDDIOM0/VDDIOM1 (Memory I/Os)
- Available in a 324-ball TFBGA Green Package

3. Signal Description

Table 3-1 gives details on the signal name classified by peripheral.

Table 3-1. Signal Description List

Signal Name	Function	Type	Active Level	Comments
Power Supplies				
VDDIOM0	EBI0 I/O Lines Power Supply	Power		1.65V to 3.6V
VDDIOM1	EBI1 I/O Lines Power Supply	Power		1.65V to 3.6V
VDDIOP0	Peripherals I/O Lines Power Supply	Power		2.7V to 3.6V
VDDIOP1	Peripherals I/O Lines Power Supply	Power		1.65V to 3.6V
VDDBU	Backup I/O Lines Power Supply	Power		1.08V to 1.32V
VDDPLL	PLL Power Supply	Power		3.0V to 3.6V
VDDOSC	Oscillator Power Supply	Power		3.0V to 3.6V
VDDCORE	Core Chip Power Supply	Power		1.08V to 1.32V
GND	Ground	Ground		
GNDPLL	PLL Ground	Ground		
GNDBU	Backup Ground	Ground		
Clocks, Oscillators and PLLs				
XIN	Main Oscillator Input	Input		
XOUT	Main Oscillator Output	Output		
XIN32	Slow Clock Oscillator Input	Input		
XOUT32	Slow Clock Oscillator Output	Output		
PLLRCA	PLL A Filter	Input		
PLLRCB	PLL B Filter	Input		
PCK0 - PCK3	Programmable Clock Output	Output		
Shutdown, Wakeup Logic				
SHDN	Shutdown Control	Output		Driven at 0V only. Do not tie over VDDBU.
WKUP	Wake-up Input	Input		Accepts between 0V and VDDBU.
ICE and JTAG				
NTRST	Test Reset Signal	Input	Low	Pull-up resistor
TCK	Test Clock	Input		No pull-up resistor
TDI	Test Data In	Input		No pull-up resistor
TDO	Test Data Out	Output		
TMS	Test Mode Select	Input		No pull-up resistor
JTAGSEL	JTAG Selection	Input		Pull-down resistor. Accepts between 0V and VDDBU.
RTCK	Return Test Clock	Output		

Table 4-1. AT91SAM9263 Pinout for 324-ball TFBGA Package (Continued)

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
C16	GND	H7	PD16	M16	PA7	U7	EBI1_A5
C17	VDDIOP0	H8	VDDIOM0	M17	PA5	U8	EBI1_A10
C18	HDPB	H9	GND	M18	PA8	U9	EBI1_A16_BA0
D1	EBI0_D10	H10	VDDCORE	N1	NC	U10	EBI1_NRD
D2	EBI0_D3	H11	GND	N2	NC	U11	EBI1_D3
D3	NC(1)	H12	PB19	N3	PE19	U12	EBI1_D13
D4	EBI0_D1	H13	PB17	N4	NC(1)	U13	PE22
D5	EBI0_A20	H14	PB15	N5	PE17	U14	PE27
D6	EBI0_A17_BA1	H15	PB13	N6	PE16	U15	RTCK
D7	EBI0_A18	H16	PB24	N7	EBI1_A6	U16	NTRST
D8	EBI0_A9	H17	PB14	N8	EBI1_A11	U17	VDDPLLA
D9	EBI0_A2	H18	PB12	N9	EBI1_A22	U18	PLLRCA
D10	PD1	J1	PD30	N10	EBI1_D2	V1	VDDCORE
D11	PC25	J2	PD26	N11	EBI1_D6	V2	PA22
D12	PC20	J3	PD22	N12	EBI1_D9	V3	PA27
D13	PC6	J4	PD19	N13	GND	V4	PA29
D14	PC16	J5	PD18	N14	GNDPLL	V5	EBI1_A1_NWR2
D15	PC10	J6	PD23	N15	PA1	V6	EBI1_A3
D16	PC2	J7	PD21	N16	PA0	V7	EBI1_A9
D17	PC1	J8	PD20	N17	TMS	V8	EBI1_A15
D18	HDMB	J9	GND	N18	TDO	V9	EBI1_A20
E1	EBI0_D15	J10	GND	P1	XIN32	V10	EBI1_NBS1_NWR1
E2	EBI0_D7	J11	GND	P2	SHDN	V11	EBI1_D5
E3	EBI0_D5	J12	PB11	P3	PA16	V12	EBI1_D11
E4	EBI0_D8	J13	PB9	P4	WKUP	V13	PE21
E5	EBI0_NBS1_NWR1	J14	PB10	P5	JTAGSEL	V14	PE24
E6	EBI0_NRD	J15	PB5	P6	PE20	V15	NRST
E7	EBI0_A14	J16	PB6	P7	EBI1_A8	V16	GND
E8	EBI0_SDA10	J17	PB7	P8	EBI1_A4	V17	GND
E9	EBI0_A0_NBS0	J18	PB8	P9	EBI1_A19	V18	VDDPLLB

Note: 1. NC pins must be left unconnected.

6. I/O Line Considerations

6.1 JTAG Port Pins

TMS, TDI and TCK are Schmitt trigger inputs and have no pull-up resistors.

TDO and RTCK are outputs, driven at up to VDDIOP0, and have no pull-up resistors.

The JTAGSEL pin is used to select the JTAG boundary scan when asserted at a high level (VDDBU). It integrates a permanent pull-down resistor of about 15 kΩ to GNDBU, so that it can be left unconnected for normal operations.

The NTRST signal is described in Section 6.3.

All JTAG signals except JTAGSEL (VDDBU) are supplied with VDDIOP0.

6.2 Test Pin

The TST pin is used for manufacturing test purposes when asserted high. It integrates a permanent pull-down resistor of about 15 kΩ to GNDBU, so that it can be left unconnected for normal operations. Driving this line at a high level leads to unpredictable results.

This pin is supplied with VDDBU.

6.3 Reset Pins

NRST is an open-drain output integrating a non-programmable pull-up resistor. It can be driven with voltage at up to VDDIOP0.

NTRST is an input which allows reset of the JTAG Test Access port. It has no action on the processor.

As the product integrates power-on reset cells, which manage the processor and the JTAG reset, the NRST and NTRST pins can be left unconnected.

The NRST and NTRST pins both integrate a permanent pull-up resistor of 100 kΩ minimum to VDDIOP0.

The NRST signal is inserted in the Boundary Scan.

6.4 PIO Controllers

All the I/O lines managed by the PIO Controllers integrate a programmable pull-up resistor of 100 kΩ typical. Programming of this pull-up resistor is performed independently for each I/O line through the PIO Controllers.

After reset, all the I/O lines default as inputs with pull-up resistors enabled, except those which are multiplexed with the External Bus Interface signals that require to be enabled as Peripheral at reset. This is explicitly indicated in the column “Reset State” of the PIO Controller multiplexing tables on page 33 and following.

6.5 Shutdown Logic Pins

The SHDN pin is a tri-state output only pin, which is driven by the Shutdown Controller. There is no internal pull-up. An external pull-up to VDDBU is needed and its value must be higher than 1 MΩ. The resistor value is calculated according to the regulator enable implementation and the SHDN level.

The pin WKUP is an input-only. It can accept voltages only between 0V and VDDBU.

7. Processor and Architecture

7.1 ARM926EJ-S Processor

- RISC Processor based on ARM v5TEJ Harvard Architecture with Jazelle technology for Java acceleration
- Two Instruction Sets
  - ARM High-performance 32-bit Instruction Set
  - Thumb High Code Density 16-bit Instruction Set
- DSP Instruction Extensions
- 5-stage Pipeline Architecture
  - Instruction Fetch (F)
  - Instruction Decode (D)
  - Execute (E)
  - Data Memory (M)
  - Register Write (W)
- 16 Kbyte Data Cache, 16 Kbyte Instruction Cache
  - Virtually-addressed 4-way Associative Cache
  - Eight words per line
  - Write-through and Write-back Operation
  - Pseudo-random or Round-robin Replacement
- Write Buffer
  - Main Write Buffer with 16-word Data Buffer and 4-address Buffer
  - DCache Write-back Buffer with 8-word Entries and a Single Address Entry
  - Software Control Drain
- Standard ARM v4 and v5 Memory Management Unit (MMU)
  - Access Permission for Sections
  - Access Permission for large pages and small pages can be specified separately for each quarter of the page
  - 16 embedded domains
- Bus Interface Unit (BIU)
  - Arbitrates and Schedules AHB Requests
  - Separate Masters for both instruction and data access providing complete Matrix system flexibility
  - Separate Address and Data Buses for both the 32-bit instruction interface and the 32-bit data interface
  - On Address and Data Buses, data can be 8-bit (Bytes), 16-bit (Half-words) or 32-bit (Words)

7.2 Bus Matrix

- 9-layer Matrix, handling requests from 9 masters
- Programmable Arbitration strategy
  - Fixed-priority Arbitration
  - Round-Robin Arbitration, either with no default master, last accessed default master or fixed default master
- Burst Management
  - Breaking with Slot Cycle Limit Support
  - Undefined Burst Length Support
- One Address Decoder provided per Master
  - Three different slaves may be assigned to each decoded memory area: one for internal boot, one for external boot, one after remap

- Boot Mode Select
  - Non-volatile Boot Memory can be internal or external
  - Selection is made by BMS pin sampled at reset
- Remap Command
  - Allows Remapping of an Internal SRAM in Place of the Boot Non-Volatile Memory
  - Allows Handling of Dynamic Exception Vectors

7.3 Matrix Masters

The Bus Matrix of the AT91SAM9263 manages nine masters, thus each master can perform an access concurrently with others to an available slave peripheral or memory.

Each master has its own decoder, which is defined specifically for each master.

Table 7-1. List of Bus Matrix Masters

Master 0	OHCI USB Host Controller
Master 1	Image Sensor Interface
Master 2	Two D Graphic Controller
Master 3	DMA Controller
Master 4	Ethernet MAC
Master 5	LCD Controller
Master 6	Peripheral DMA Controller
Master 7	ARM926 Data
Master 8	ARM926™ Instruction

7.4 Matrix Slaves

The Bus Matrix of the AT91SAM9263 manages eight slaves. Each slave has its own arbiter, thus allowing to program a different arbitration per slave.

The LCD Controller, the DMA Controller, the USB OTG and the USB Host have a user interface mapped as a slave on the Matrix. They share the same layer, as programming them does not require a high bandwidth.

Table 7-2. List of Bus Matrix Slaves

Slave 0	Internal ROM
Slave 1	Internal 80 Kbyte SRAM
Slave 2	Internal 16 Kbyte SRAM
Slave 3	LCD Controller User Interface
	DMA Controller User Interface
	USB Host User Interface
Slave 4	External Bus Interface 0
Slave 5	External Bus Interface 1
Slave 6	Peripheral Bridge

7.5 Master to Slave Access

In most cases, all the masters can access all the slaves. However, some paths do not make sense, for example, allowing access from the Ethernet MAC to the Internal Peripherals. Thus, these paths are forbidden or simply not wired, and are shown as “-” in Table 7-3.

Table 7-3. Masters to Slaves Access

Master		0	1	2	3	4	5	6	7&8
Slave		OHCI USB Host Controller	Image Sensor Interface	Two D Graphics Controller	DMA Controller	Ethernet MAC	LCD Controller	Peripheral DMA Controller	ARM926 Data & Instruction
0	Internal ROM	X	X	X	X	X	X	X	X
1	Internal 80 Kbyte SRAM	X	X	X	X	X	X	X	X
2	Internal 16 Kbyte SRAM Bank	X	X	X	X	X	X	X	X
3	LCD Controller User Interface	-	-	-	-	-	-	-	X
	DMA Controller User Interface	-	-	-	-	-	-	-	X
	USB Host User Interface	-	-	-	-	-	-	-	X
4	External Bus Interface 0	X	X	X	X	X	X	X	X
5	External Bus Interface 1	X	X	X	X	X	X	X	X
6	Peripheral Bridge	-	-	-	X	-	-	X	X

7.6 Peripheral DMA Controller

- Acts as one Matrix Master
- Allows data transfers between a peripheral and memory without any intervention of the processor
- Next Pointer support, removes heavy real-time constraints on buffer management.
- Twenty channels
  - Two for each USART
  - Two for the Debug Unit
  - Two for each Serial Synchronous Controller
  - Two for each Serial Peripheral Interface
  - Two for the AC97 Controller
  - One for each Multimedia Card Interface

The Peripheral DMA Controller handles transfer requests from the channel according to the following priorities (low to high priorities):

- DBGU Transmit Channel
- USART2 Transmit Channel
- USART1 Transmit Channel
- USART0 Transmit Channel
- AC97 Transmit Channel

Within the 80 Kbytes of SRAM available, the amount of memory assigned to each block is software programmable as a multiple of 16 Kbytes as shown in Table 8-2. This table provides the size of the Internal SRAM C according to the size of the internal SRAM A and the internal SRAM B.

Table 8-2. Internal SRAM Block Size

Internal SRAM C		Internal SRAM A (ITCM) Size		
		0	16 Kbytes	32 Kbytes
Internal SRAM B (DTCM) size	0	80 Kbytes	64 Kbytes	48 Kbytes
	16 Kbytes	64 Kbytes	48 Kbytes	32 Kbytes
	32 Kbytes	48 Kbytes	32 Kbytes	16 Kbytes

Note that among the five 16 Kbyte blocks making up the Internal SRAM, one is permanently assigned to Internal SRAM C.

At reset, the whole memory (80 Kbytes) is assigned to Internal SRAM C.

The memory blocks assigned to SRAM A, SRAM B and SRAM C areas are not contiguous and when the user dynamically changes the Internal SRAM configuration, the new 16 Kbyte block organization may affect the previous configuration from a software point of view.

Table 8-3 illustrates different configurations and the related 16 Kbyte blocks assignments (RB0 to RB4).

Table 8-3. 16 Kbyte Block Allocation

Decoded Area	Address	Configuration examples and related 16 Kbyte block assignments				
		ITCM = 0 Kbyte DTCM = 0 Kbyte AHB = 80 Kbytes (1)	ITCM = 32 Kbytes DTCM = 32 Kbytes AHB = 16 Kbytes	ITCM = 16 Kbytes DTCM = 32 Kbytes AHB = 32 Kbytes	ITCM = 32 Kbytes DTCM = 16 Kbytes AHB = 32 Kbytes	ITCM = 16 Kbytes DTCM = 16 Kbytes AHB = 48 Kbytes
Internal SRAM A (ITCM)	0x0010 0000		RB1	RB1	RB1	RB1
	0x0010 4000		RB0		RB0	
Internal SRAM B (DTCM)	0x0020 0000		RB3	RB3	RB3	RB3
	0x0020 4000		RB2	RB2		
Internal SRAM C (AHB)	0x0030 0000	RB4	RB4	RB4	RB4	RB4
	0x0030 4000	RB3		RB0	RB2	RB2
	0x0030 8000	RB2				RB0
	0x0030 C000	RB1				
	0x0031 0000	RB0				

Note: 1. Configuration after reset.

When accessed from the Bus Matrix, the internal 80 Kbytes of Fast SRAM is single cycle accessible at full matrix speed (MCK). When accessed from the processor's TCM Interface, they are also single cycle accessible at full processor speed.

8.1.1.2 Internal 16 Kbyte Fast SRAM

The AT91SAM9263 integrates a 16 Kbyte SRAM, mapped at address 0x0050 0000. This SRAM is single cycle accessible at full Bus Matrix speed.

8.1.2 Boot Strategies

The system always boots at address 0x0. To ensure maximum boot possibilities, the memory layout can be changed with two parameters.

REMAP allows the user to layout the internal SRAM bank to 0x0. This is done by software once the system has booted. Refer to the section “AT91SAM9263 Bus Matrix” in the product datasheet for more details.

When REMAP = 0, BMS allows the user to layout at address 0x0 either the ROM or an external memory. This is done via hardware at reset.

Note: Memory blocks not affected by these parameters can always be seen at their specified base addresses. See the complete memory map presented in Figure 8-1 on page 20.

The AT91SAM9263 Bus Matrix manages a boot memory that depends on the level on the pin BMS at reset. The internal memory area mapped between address 0x0 and 0x000F FFFF is reserved to this effect.

If BMS is detected at 1, the boot memory is the embedded ROM.

If BMS is detected at 0, the boot memory is the memory connected on the Chip Select 0 of the External Bus Interface.

8.1.2.1 BMS = 1, Boot on Embedded ROM

The system boots on Boot Program.

- Boot at slow clock
- Auto baudrate detection
- Downloads and runs an application from external storage media into internal SRAM
- Downloaded code size depends on embedded SRAM size
- Automatic detection of valid application
- Bootloader on a non-volatile memory
  - SD Card
  - NAND Flash
  - SPI DataFlash® and Serial Flash connected on NPCS0 of the SPI0
- Interface with SAM-BA® Graphic User Interface to enable code loading via:
  - Serial communication on a DBGU
  - USB Bulk Device Port

8.1.2.2 BMS = 0, Boot on External Memory

- Boot at slow clock
- Boot with the default configuration for the Static Memory Controller, byte select mode, 16-bit data bus, Read/Write controlled by Chip Select, allows boot on 16-bit non-volatile memory.

The customer-programmed software must perform a complete configuration.

To speed up the boot sequence when booting at 32 kHz EBI0 CS0 (BMS=0) the user must:

1. Program the PMC (main oscillator enable or bypass mode).
2. Program and Start the PLL.
3. Reprogram the SMC setup, cycle, hold, mode timings registers for CS0 to adapt them to the new clock.
4. Switch the main clock to the new value.

8.2 External Memories

The external memories are accessed through the External Bus Interfaces 0 and 1. Each Chip Select line has a 256 Mbyte memory area assigned.

Refer to Figure 8-1 on page 20.

8.2.1 External Bus Interfaces

The AT91SAM9263 features two External Bus Interfaces to offer more bandwidth to the system and to prevent bottlenecks while accessing external memories.

    - Standard and Low-power SDRAM (Mobile SDRAM)
- Numerous configurations supported
    - **2K, 4K, 8K Row Address Memory Parts**
    - **SDRAM with two or four Internal Banks**
    - **SDRAM with 16- or 32-bit Data Path**
- Programming facilities
    - **Word, half-word, byte access**
    - **Automatic page break when Memory Boundary has been reached**
    - **Multibank Ping-pong Access**
    - **Timing parameters specified by software**
    - **Automatic refresh operation, refresh rate is programmable**
- **Energy-saving capabilities**
    - **Self-refresh, power down and deep power down modes supported**
- Error detection
    - **Refresh Error Interrupt**
- **SDRAM Power-up Initialization by software**
- **CAS Latency of 1, 2 and 3 supported**
- **Auto Precharge Command not used**

8.2.4 Error Corrected Code Controller

- Tracking the accesses to a NAND Flash device by triggering on the corresponding chip select
- Single-bit error correction and two-bit random detection
- Automatic Hamming Code Calculation while writing
    - ECC value available in a register
- Automatic Hamming Code Calculation while reading
    - Error Report, including error flag, correctable error flag and word address being detected erroneous
    - Support 8- or 16-bit NAND Flash devices with 512-, 1024-, 2048- or 4096-byte pages

9. System Controller

The System Controller is a set of peripherals that allow handling of key elements of the system, such as power, resets, clocks, time, interrupts, watchdog, etc.

The System Controller User Interface also embeds registers that are used to configure the Bus Matrix and a set of registers for the chip configuration. The chip configuration registers can be used to configure:

- EBI0 and EBI1 chip select assignment and voltage range for external memories
- ARM Processor Tightly Coupled Memories

The System Controller peripherals are all mapped within the highest 16 Kbytes of address space, between addresses 0xFFFF C000 and 0xFFFF FFFF.

However, all the registers of the System Controller are mapped on the top of the address space. This allows all the registers of the System Controller to be addressed from a single pointer by using the standard ARM instruction set, as the Load/Store instructions have an indexing mode of ± 4 Kbytes.

Figure 9-1 on page 26 shows the System Controller block diagram.

Figure 8-1 on page 20 shows the mapping of the User Interfaces of the System Controller peripherals.

9.13 Chip Identification

- Chip ID: 0x019607A0
- JTAG ID: 0x05B0C03F
- ARM926 TAP ID: 0x0792603F

9.14 PIO Controllers

- Five PIO Controllers, PIOA to PIOE, controlling a total of 160 I/O Lines
- Each PIO Controller controls up to 32 programmable I/O Lines
  - PIOA has 32 I/O Lines
  - PIOB has 32 I/O Lines
  - PIOC has 32 I/O Lines
  - PIOD has 32 I/O Lines
  - PIOE has 32 I/O Lines
- Fully programmable through Set/Clear Registers
- Multiplexing of two peripheral functions per I/O Line
- For each I/O Line (whether assigned to a peripheral or used as general-purpose I/O)
  - Input change interrupt
  - Glitch filter
  - Multi-drive option enables driving in open drain
  - Programmable pull-up on each I/O line
  - Pin data status register, supplies visibility of the level on the pin at any time
- Synchronous output, provides Set and Clear of several I/O lines in a single write

10.3.2 PIO Controller B Multiplexing

Table 10-3. Multiplexing on PIO Controller B

PIO Controller B					Application Usage	
I/O Line	Peripheral A	Peripheral B	Reset State	Power Supply	Function	Comments
PB0	AC97FS	TF0	I/O	VDDIOP0		
PB1	AC97CK	TK0	I/O	VDDIOP0		
PB2	AC97TX	TD0	I/O	VDDIOP0		
PB3	AC97RX	RD0	I/O	VDDIOP0		
PB4	TWD	RK0	I/O	VDDIOP0		
PB5	TWCK	RF0	I/O	VDDIOP0		
PB6	TF1	DMARQ1	I/O	VDDIOP0		
PB7	TK1	PWM0	I/O	VDDIOP0		
PB8	TD1	PWM1	I/O	VDDIOP0		
PB9	RD1	LCDCC	I/O	VDDIOP0		
PB10	RK1	PCK1	I/O	VDDIOP0		
PB11	RF1	SPI0_NPCS3	I/O	VDDIOP0		
PB12	SPI1_MISO		I/O	VDDIOP0		
PB13	SPI1_MOSI		I/O	VDDIOP0		
PB14	SPI1_SPCK		I/O	VDDIOP0		
PB15	SPI1_NPCS0		I/O	VDDIOP0		
PB16	SPI1_NPCS1	PCK1	I/O	VDDIOP0		
PB17	SPI1_NPCS2	TIOA2	I/O	VDDIOP0		
PB18	SPI1_NPCS3	TIOB2	I/O	VDDIOP0		
PB19			I/O	VDDIOP0		
PB20			I/O	VDDIOP0		
PB21			I/O	VDDIOP0		
PB22			I/O	VDDIOP0		
PB23			I/O	VDDIOP0		
PB24		DMARQ3	I/O	VDDIOP0		
PB25			I/O	VDDIOP0		
PB26			I/O	VDDIOP0		
PB27		PWM2	I/O	VDDIOP0		
PB28		TCLK0	I/O	VDDIOP0		
PB29		PWM3	I/O	VDDIOP0		
PB30			I/O	VDDIOP0		
PB31			I/O	VDDIOP0		

10.3.3 PIO Controller C Multiplexing

Table 10-4. Multiplexing on PIO Controller C

PIO Controller C					Application Usage	
I/O Line	Peripheral A	Peripheral B	Reset State	Power Supply	Function	Comments
PC0	LCDVSYNC		I/O	VDDIOP0		
PC1	LCDHSYNC		I/O	VDDIOP0		
PC2	LCDDOTCK		I/O	VDDIOP0		
PC3	LCDDEN	PWM1	I/O	VDDIOP0		
PC4	LCDD0	LCDD3	I/O	VDDIOP0		
PC5	LCDD1	LCDD4	I/O	VDDIOP0		
PC6	LCDD2	LCDD5	I/O	VDDIOP0		
PC7	LCDD3	LCDD6	I/O	VDDIOP0		
PC8	LCDD4	LCDD7	I/O	VDDIOP0		
PC9	LCDD5	LCDD10	I/O	VDDIOP0		
PC10	LCDD6	LCDD11	I/O	VDDIOP0		
PC11	LCDD7	LCDD12	I/O	VDDIOP0		
PC12	LCDD8	LCDD13	I/O	VDDIOP0		
PC13	LCDD9	LCDD14	I/O	VDDIOP0		
PC14	LCDD10	LCDD15	I/O	VDDIOP0		
PC15	LCDD11	LCDD19	I/O	VDDIOP0		
PC16	LCDD12	LCDD20	I/O	VDDIOP0		
PC17	LCDD13	LCDD21	I/O	VDDIOP0		
PC18	LCDD14	LCDD22	I/O	VDDIOP0		
PC19	LCDD15	LCDD23	I/O	VDDIOP0		
PC20	LCDD16	ETX2	I/O	VDDIOP0		
PC21	LCDD17	ETX3	I/O	VDDIOP0		
PC22	LCDD18	ERX2	I/O	VDDIOP0		
PC23	LCDD19	ERX3	I/O	VDDIOP0		
PC24	LCDD20	ETXER	I/O	VDDIOP0		
PC25	LCDD21	ERXDV	I/O	VDDIOP0		
PC26	LCDD22	ECOL	I/O	VDDIOP0		
PC27	LCDD23	ERXCK	I/O	VDDIOP0		
PC28	PWM0	TCLK1	I/O	VDDIOP0		
PC29	PCK0	PWM2	I/O	VDDIOP0		
PC30	DRXD		I/O	VDDIOP0		
PC31	DTXD		I/O	VDDIOP0		

10.3.5 PIO Controller E Multiplexing

Table 10-6. Multiplexing on PIO Controller E

PIO Controller E					Application Usage	
I/O Line	Peripheral A	Peripheral B	Reset State	Power Supply	Function	Comments
PE0	ISI_D0		I/O	VDDIOP1		
PE1	ISI_D1		I/O	VDDIOP1		
PE2	ISI_D2		I/O	VDDIOP1		
PE3	ISI_D3		I/O	VDDIOP1		
PE4	ISI_D4		I/O	VDDIOP1		
PE5	ISI_D5		I/O	VDDIOP1		
PE6	ISI_D6		I/O	VDDIOP1		
PE7	ISI_D7		I/O	VDDIOP1		
PE8	ISI_PCK	TIOA1	I/O	VDDIOP1		
PE9	ISI_HSYNC	TIOB1	I/O	VDDIOP1		
PE10	ISI_VSYNC	PWM3	I/O	VDDIOP1		
PE11		PCK3	I/O	VDDIOP1		
PE12		ISI_D8	I/O	VDDIOP1		
PE13		ISI_D9	I/O	VDDIOP1		
PE14		ISI_D10	I/O	VDDIOP1		
PE15		ISI_D11	I/O	VDDIOP1		
PE16			I/O	VDDIOP1		
PE17			I/O	VDDIOP1		
PE18		TIOA0	I/O	VDDIOP1		
PE19		TIOB0	I/O	VDDIOP1		
PE20		EBI1_NWAIT	I/O	VDDIOM1		
PE21	ETXCK	EBI1_NANDWE	I/O	VDDIOM1		
PE22	ECRS	EBI1_NCS2/NANDCS	I/O	VDDIOM1		
PE23	ETX0	EB1_NANDOE	I/O	VDDIOM1		
PE24	ETX1	EBI1_NWR3/NBS3	I/O	VDDIOM1		
PE25	ERX0	EBI1_NCS1/SDCS	I/O	VDDIOM1		
PE26	ERX1		I/O	VDDIOM1		
PE27	ERXER	EBI1_SDCKE	I/O	VDDIOM1		
PE28	ETXEN	EBI1_RAS	I/O	VDDIOM1		
PE29	EMDC	EBI1_CAS	I/O	VDDIOM1		
PE30	EMDIO	EBI1_SDWE	I/O	VDDIOM1		
PE31	EF100	EBI1_SDA10	I/O	VDDIOM1		

- Supports both low-speed 1.5 Mbps and full-speed 12 Mbps devices
- Root hub integrated with two downstream USB ports
- Two embedded USB transceivers
- Supports power management
- Operates as a master on the matrix

10.5.11 USB Device Port

- USB V2.0 full-speed compliant, 12 Mbits per second
- Embedded USB V2.0 full-speed transceiver
- Embedded 2,432-byte dual-port RAM for endpoints
- Suspend/Resume logic
- Ping-pong mode (two memory banks) for isochronous and bulk endpoints
- Six general-purpose endpoints
    - Endpoint 0 and 3: 64 bytes, no ping-pong mode
    - Endpoint 1 and 2: 64 bytes, ping-pong mode
    - Endpoint 4 and 5: 512 bytes, ping-pong mode

10.5.12 LCD Controller

- Single and Dual scan color and monochrome passive STN LCD panels supported
- Single scan active TFT LCD panels supported
- 4-bit single scan, 8-bit single or dual scan, 16-bit dual scan STN interfaces supported
- Up to 24-bit single scan TFT interfaces supported
- Up to 16 gray levels for mono STN and up to 4096 colors for color STN displays
- 1, 2 bits per pixel (palletized), 4 bits per pixel (non-palletized) for mono STN
- 1, 2, 4, 8 bits per pixel (palletized), 16 bits per pixel (non-palletized) for color STN
- 1, 2, 4, 8 bits per pixel (palletized), 16, 24 bits per pixel (non-palletized) for TFT
- Single clock domain architecture
- Resolution supported up to 2048x2048
- 2D DMA Controller for management of virtual Frame Buffer
    - Allows management of frame buffer larger than the screen size and moving the view over this virtual frame buffer
- Automatic resynchronization of the frame buffer pointer to prevent flickering

10.5.13 Two D Graphics Controller

- Acts as one Matrix Master
- Commands are passed through the APB User Interface
- Operates directly in the frame buffer of the LCD Controller
    - Line draw
    - Block transfer
    - Clipping
- Commands queuing through a FIFO

10.5.14 Ethernet 10/100 MAC

- Compatibility with IEEE Standard 802.3
- 10 and 100 Mbits per second data throughput capability
- Full- and half-duplex operations
- MII or RMII interface to the physical layer

- Register Interface to address, data, status and control registers
- DMA Interface, operating as a master on the Memory Controller
- Interrupt generation to signal receive and transmit completion
- 28-byte transmit and 28-byte receive FIFOs
- Automatic pad and CRC generation on transmitted frames
- Address checking logic to recognize four 48-bit addresses
- Support promiscuous mode where all valid frames are copied to memory
- Support physical layer management through MDIO interface control of alarm and update time/calendar data in

10.5.15 Image Sensor Interface

- ITU-R BT. 601/656 8-bit mode external interface support
- Support for ITU-R BT.656-4 SAV and EAV synchronization
- Vertical and horizontal resolutions up to 2048 x 2048
- Preview Path up to 640*480
- Support for packed data formatting for YCbCr 4:2:2 formats
- Preview scaler to generate smaller size image
- Programmable frame capture rate

13. Revision History

Table 13-1. Revision History

Document Ref.	Comments	Change Request Ref.
6459IS	**Ordering Code:** Table 12-1, ”AT91SAM9263 Ordering Information”, Removed all reference to Marketing Revision Level A, AT91SAM9263-CU Added AT91SAM9263B-CU-100 to Marketing Revision Level B Ordering Code.	8456 (msg3)
	Package Drawings: Section 11. ”Package Drawings” Old Package Drawing removed. Existing package described in: Section 11.1 ”Package Drawing AT91SAM9263B-CU” Package drawings and related information added for SAM9263B-CU-100. Section 11.2 ”Package Drawing (AT91SAM9263B-CU-100)” Document format updated with subsequent change to pagination.	8456 (msg3)
6249HS	EBI0_NCS3 restriction added to Section 10.4.2 “ETM™” on page 38	6053
	Second paragraph in Section 5.3 “Programmable I/O Lines Power Supplies” on page 13 edited.	6395
6249GS	Overview: ”Features” Debug Unit (DBGU) updated. Section 10.4.3 ”EBI1”, updated Section 10.4.4 ”Ethernet 10/100MAC”, added to datasheet Section 6.5 ”Shutdown Logic Pins”, updated, “SHDN pin is tri state output.....”	5846 5903 rfo
6249FS	Section 5.1 ”Power Supplies”, VDDCORE and VDDBU updated. Section 5.2, “Power Sequence Requirements removed from datasheet.	5791/5793
6249ES	New Ordering Code: **AT91SAM9263B-CU** added to Table 12-1, ”AT91SAM9263 Ordering Information”.	5560
	Section 8.1.2.1 ”BMS = 1, Boot on Embedded ROM”, changes to list under “Bootloader on a non-volatile memory”	5425
	Section 5.2 ”Power Sequence Requirements”, section added to datasheet.	5643
	Section 10.4.3 ”EBI1”, System Resource Multiplexing, Ethernet 10/100 MAC limitation on EBI1 updated.	5713
	Section 10.5.8 ”Multimedia Card Interface”, protocol specification compatibilities updated.	5282
	Section 10.5.13 ”Two D Graphics Controller”, removed reference to Polygon Fill, removed from Features also.	5206
	Table 3-1, ”Signal Description List”, Image Sensor Interface, ISI_MCK is provided by PCK3. Table 10-6, ”Multiplexing on PIO Controller E”, ISI_MCK removed from PE11 line of the table.	5329

Table 13-1. Revision History

Document Ref.	Comments	Change Request Ref.
6249DS	”Features”, SPI: Synchronous Communications feature removed.	4910
	Section 5.1 ”Power Supplies”, VDDIO and VDDBU slope alignment described.	4967
	Section 5.2 ”Power Consumption”, paragraph beginning with “On VDDBU...” updated.	4505
	Section 10.5.8 ”Multimedia Card Interface”, “When REMAP = 1.....” removed from 2nd paragraph.	5029
	Section 10.5.8 ”Multimedia Card Interface”, MMC and SDMC compatibility updated.	4945
	Section 8.2.1.1 ”External Bus Interface 0”, feature added.	4146
	Section 8.2.1.1 ”External Bus Interface 0”, feature added.	
	“Package and Pinout” , references to package are “324-TFBGA.	4664
	Figure 9-3 ”AT91SAM9263 Power Management Controller Block Diagram” on page 28, /3 divider removed.	4834
	Figure 11-1 ”324-ball TFBGA Package Drawing” on page 44, updated.	4668