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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	80C51
Core Size	8-Bit
Speed	48MHz
Connectivity	I²C, SPI, UART/USART, USB
Peripherals	LED, POR, PWM, WDT
Number of I/O	34
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	1.25K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at89c5130a-rdrum

Table 3-10. USB Signal Description

Signal Name	Type	Description	Alternate Function
D+	I/O	USB Data + signal Set to high level under reset.	-
D-	I/O	USB Data - signal Set to low level under reset.	-
VREF	O	**USB Reference Voltage** Connect this pin to D+ using a 1.5 kΩ resistor to use the Detach function.	-

Table 3-11. System Signal Description

Signal Name	Type	Description	Alternate Function
AD[7:0]	I/O	Multiplexed Address/Data LSB for external access Data LSB for Slave port access (used for 8-bit and 16-bit modes)	P0[7:0]
A[15:8]	I/O	Address Bus MSB for external access	P2[7:0]
$\overline{RD}$	I/O	**Read Signal** Read signal asserted during external data memory read operation. Control input for slave port read access cycles.	P3.7
$\overline{WR}$	I/O	**Write Signal** Write signal asserted during external data memory write operation. Control input for slave write access cycles.	P3.6
RST	O	**Reset Input** Holding this pin low for 64 oscillator periods while the oscillator is running resets the device. The Port pins are driven to their reset conditions when a voltage lower than V_{IL} is applied, whether or not the oscillator is running. This pin has an internal pull-up resistor which allows the device to be reset by connecting a capacitor between this pin and VSS. Asserting $\overline{RST}$ when the chip is in Idle mode or Power-down mode returns the chip to normal operation. This pin is tied to 0 for at least 12 oscillator periods when an internal reset occurs (hardware watchdog or power monitor).	-
ALE	O	**Address Latch Enable Output** The falling edge of ALE strobes the address into external latch. This signal is active only when reading or writing external memory using MOVX instructions.	-
PSEN	I/O	**Program Strobe Enable / Hardware conditions Input for ISP** Used as input under reset to detect external hardware conditions of ISP mode.	-
$\overline{EA}$	I	External Access Enable This pin must be held low to force the device to fetch code from external program memory starting at address 0000h.	-

Table 3-12. Power Signal Description

Signal Name	Type	Description	Alternate Function
AVSS	GND	**Analog Ground** AVSS is used to supply the on-chip PLL and the USB PAD.	-

4. Typical Application

4.1 Recommended External components

All the external components described in the figure below must be implemented as close as possible from the microcontroller package.

The following figure represents the typical wiring schematic.

Figure 4-1. Typical Application

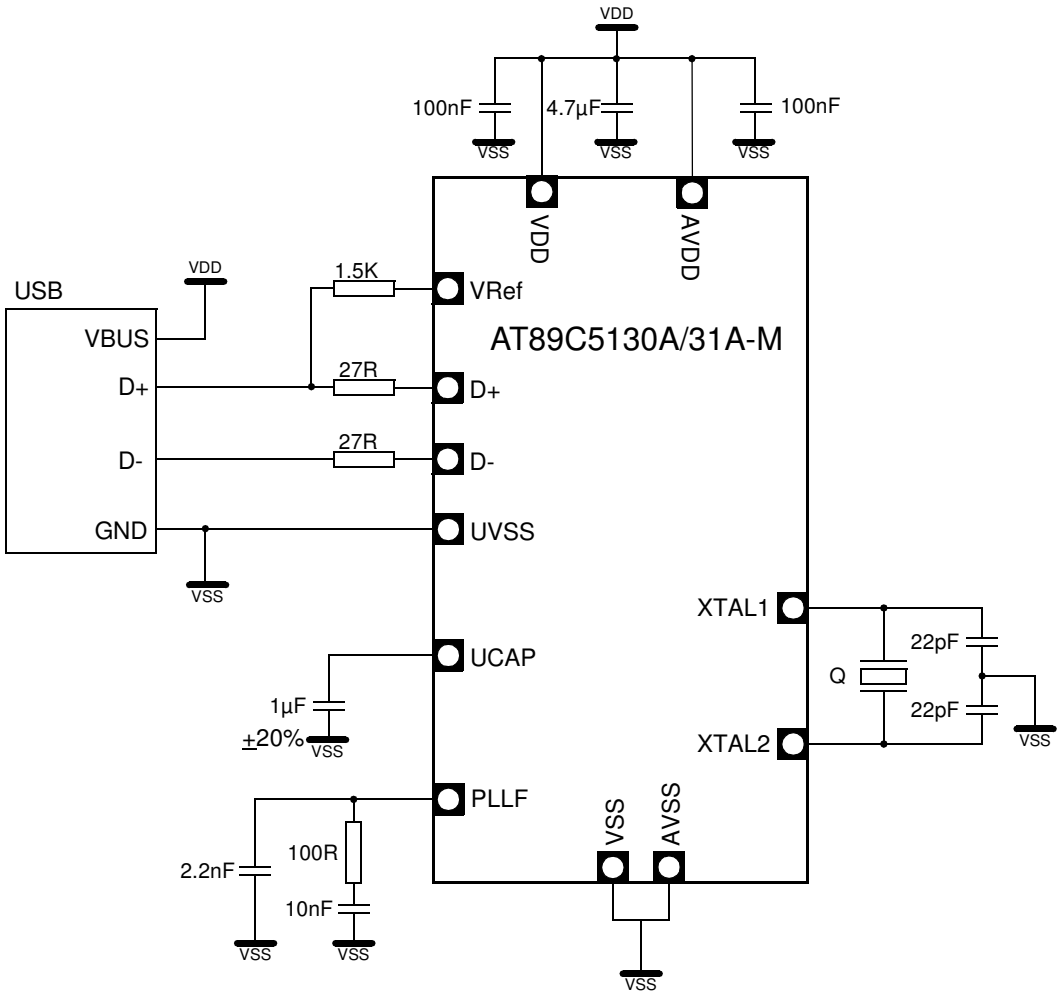
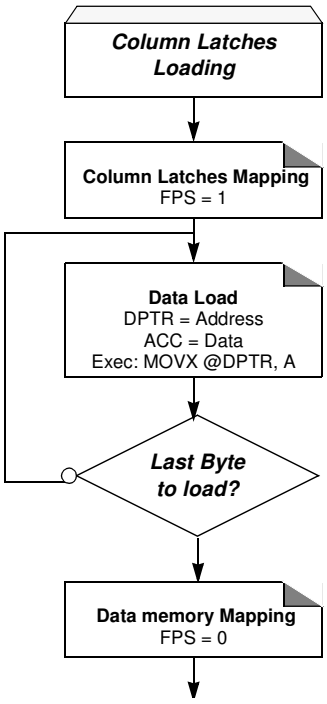


Figure 8-5. Column Latches Loading Procedure



8.3.6 Programming the Flash Spaces

8.3.6.1 User

The following procedure is used to program the User space and is summarized in Figure 8-6:

- Load data in the column latches from address 0000h to 7FFFh(1).
- Disable the interrupts.
- Launch the programming by writing the data sequence 50h followed by A0h in FCON register.
  The end of the programming indicated by the FBUSY flag cleared.
- Enable the interrupts.

Note: 1. The last page address used when loading the column latch is the one used to select the page programming address.

8.3.6.2 Extra Row

The following procedure is used to program the Extra Row space and is summarized in Figure 8-6:

- Load data in the column latches from address FF80h to FFFFh.
- Disable the interrupts.
- Launch the programming by writing the data sequence 52h followed by A2h in FCON register.
  The end of the programming indicated by the FBUSY flag cleared.
- Enable the interrupts.

Table 9-5. Program Lock Bits of the SSB

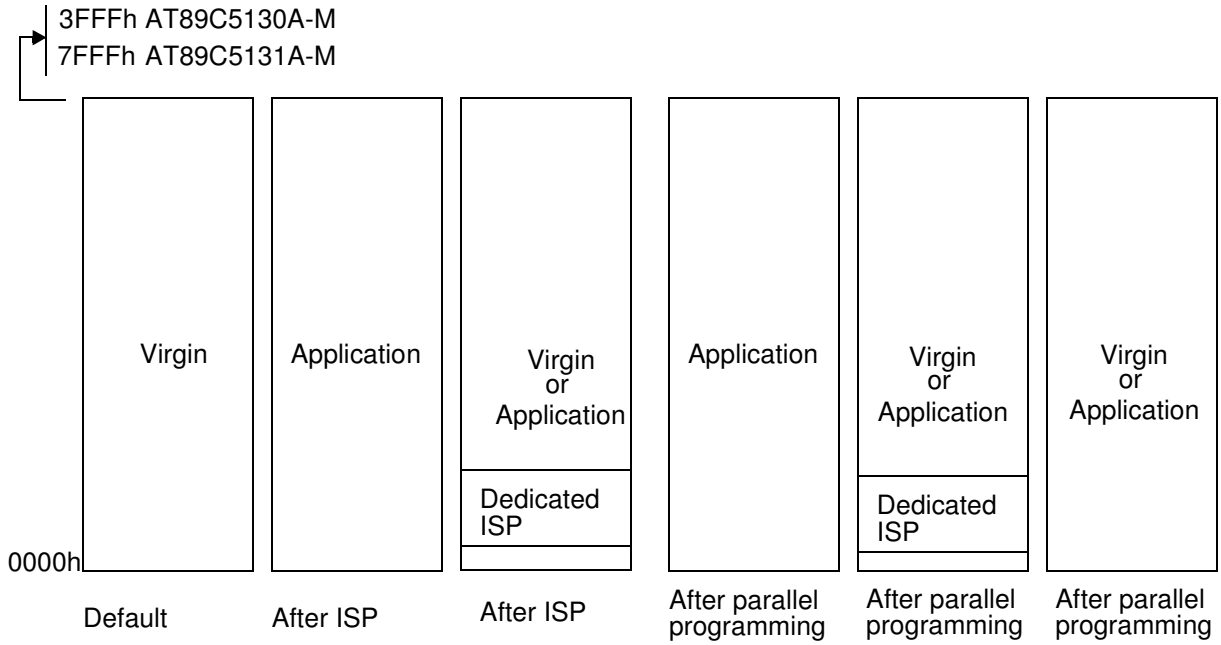
Program Lock Bits			
Security Level	**LB0**	**LB1**	**Protection Description**
1	U	U	No program lock features enabled.
2	P	U	ISP programming of the Flash is disabled.
3	P	P	Same as 2, also verify through ISP programming interface is disabled.

Notes:
1. U: unprogrammed or "one" level.
2. P: programmed or “zero” level.
3. WARNING: Security level 2 and 3 should only be programmed after Flash and code verification.

9.5 Flash Memory Status

AT89C5130A/31A-M parts are delivered with the ISP boot in the Flash memory. After ISP or parallel programming, the possible contents of the Flash memory are summarized in Figure 9-1:

Figure 9-1. Flash Memory Possible Contents



9.6 Memory Organization

In the AT89C5130A/31A-M, the lowest 16/32K of the 64 Kbyte program memory address space is filled by internal Flash.

When the $\overline{EA}$ is pin high, the processor fetches instructions from internal program Flash. Bus expansion for accessing program memory from 16/32K upward is automatic since external instruction fetches occur automatically when the program counter exceeds 3FFFh (16K) or 7FFFh (32K). If the $\overline{EA}$ pin is tied low, all program memory fetches are from external memory. If all storage is on chip, then byte location 3FFFh (16K) or 7FFFh (32K) should be left vacant to prevent and undesired pre-fetch from external program memory address 4000h (16K) or 8000h (32K).

12. On-chip Expanded RAM (ERAM)

The AT89C5130A/31A-M provides additional Bytes of random access memory (RAM) space for increased data parameters handling and high level language usage.

AT89C5130A/31A-M devices have expanded RAM in external data space; maximum size and location are described in Table 12-1.

Table 12-1. Description of Expanded RAM

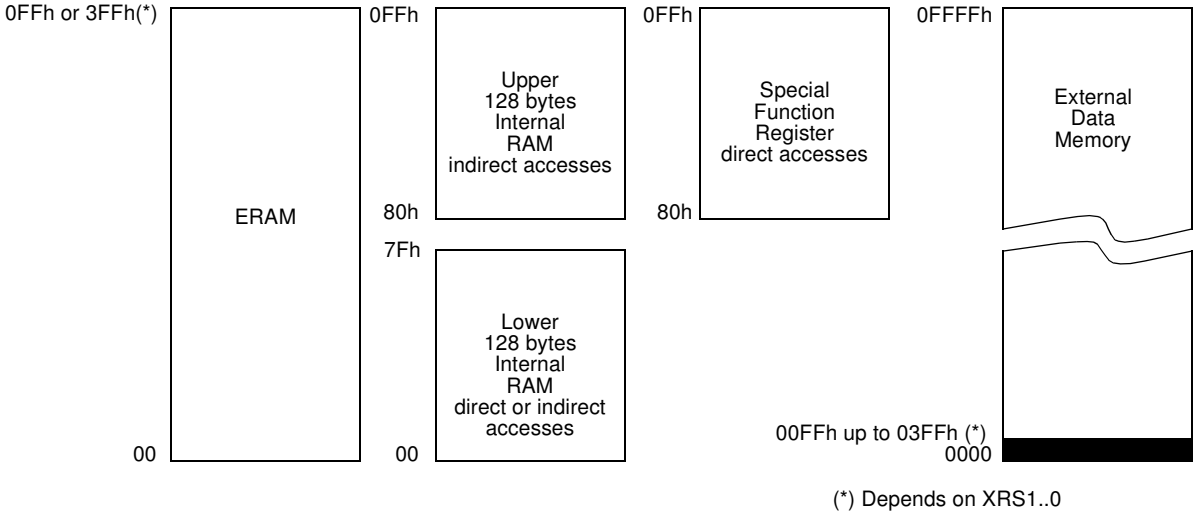
Part Number	ERAM Size	Address	
		Start	End
AT89C5130A/31A-M	1024	00h	3FFh

The AT89C5130A/31A-M has on-chip data memory which is mapped into the following four separate segments.

1. The Lower 128 bytes of RAM (addresses 00h to 7Fh) are directly and indirectly addressable.
2. The Upper 128 bytes of RAM (addresses 80h to FFh) are indirectly addressable only.
3. The Special Function Registers, SFRs, (addresses 80h to FFh) are directly addressable only.
4. The expanded RAM bytes are indirectly accessed by MOVX instructions, and with the EXTRAM bit cleared in the AUXR register (see Table 12-1)

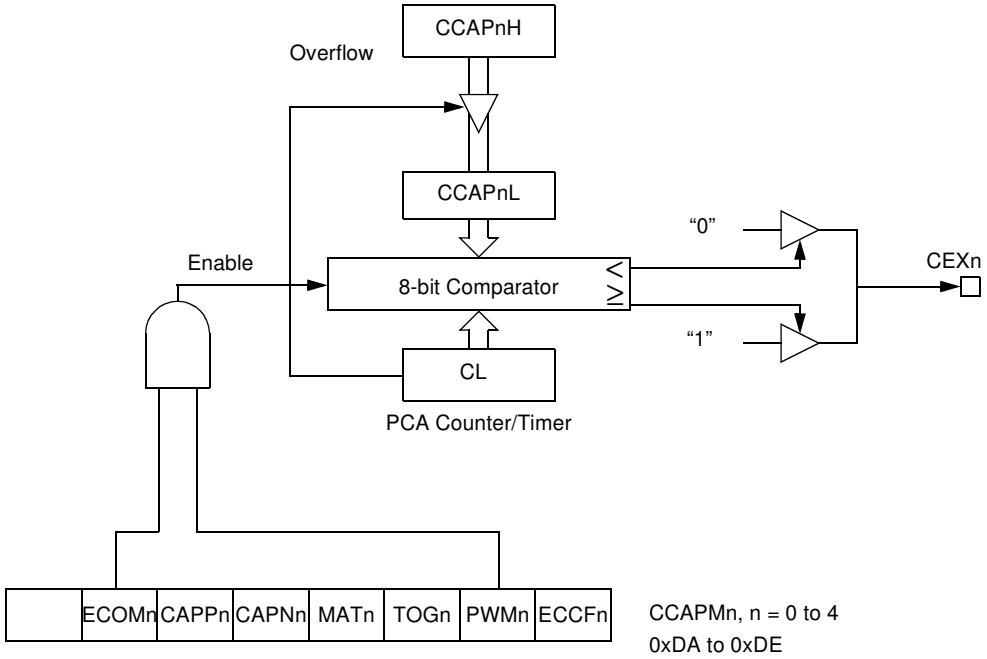
The lower 128 bytes can be accessed by either direct or indirect addressing. The Upper 128 bytes can be accessed by indirect addressing only. The Upper 128 bytes occupy the same address space as the SFR. That means they have the same address, but are physically separate from SFR space.

Figure 12-1. Internal and External Data Memory Address



When an instruction accesses an internal location above address 7Fh, the CPU knows whether the access is to the upper 128 bytes of data RAM or to SFR space by the addressing mode used in the instruction.

Figure 14-6. PCA PWM Mode



14.5 PCA Watchdog Timer

An on-board watchdog timer is available with the PCA to improve the reliability of the system without increasing chip count. Watchdog timers are useful for systems that are susceptible to noise, power glitches, or electrostatic discharge. Module 4 is the only PCA module that can be programmed as a watchdog. However, this module can still be used for other modes if the watchdog is not needed. Figure 14-4 shows a diagram of how the watchdog works. The user pre-loads a 16-bit value in the compare registers. Just like the other compare modes, this 16-bit value is compared to the PCA timer value. If a match is allowed to occur, an internal reset will be generated. This will not cause the $\overline{\text{RST}}$ pin to be driven low.

In order to hold off the reset, the user has three options:

1. Periodically change the compare value so it will never match the PCA timer
2. Periodically change the PCA timer value so it will never match the compare values, or
3. Disable the watchdog by clearing the WDTE bit before a match occurs and then re-enable it

The first two options are more reliable because the watchdog timer is never disabled as in option #3. If the program counter ever goes astray, a match will eventually occur and cause an internal reset. The second option is also not recommended if other PCA modules are being used. Remember, the PCA timer is the time base for all modules; changing the time base for other modules would not be a good idea. Thus, in most applications the first solution is the best option.

This watchdog timer won't generate a reset out on the reset pin.

Bit Number	Bit Mnemonic	Description
7	FE	**Framing Error bit (SMOD0 = 1**) Clear to reset the error state, not cleared by a valid stop bit. Set by hardware when an invalid stop bit is detected. SMOD0 must be set to enable access to the FE bit
	SM0	**Serial port Mode bit 0** Refer to SM1 for serial port mode selection. SMOD0 must be cleared to enable access to the SM0 bit
6	SM1	**Serial port Mode bit 1** SM0 SM1 Mode Description Baud Rate 0 0 0 Shift Register $F_{CPU\ PERIPH}/6$ 0 1 1 8-bit UART Variable 1 0 2 9-bit UART $F_{CPU\ PERIPH}/32$ or /16 1 1 3 9-bit UART Variable
5	SM2	**Serial port Mode 2 bit/Multiprocessor Communication Enable bit** Clear to disable multiprocessor communication feature. Set to enable multiprocessor communication feature in mode 2 and 3, and eventually mode 1. This bit should be cleared in mode 0.
4	REN	**Reception Enable bit** Clear to disable serial reception. Set to enable serial reception.
3	TB8	Transmitter Bit 8/Ninth bit to Transmit in Modes 2 and 3 Clear to transmit a logic 0 in the 9th bit. Set to transmit a logic 1 in the 9th bit.
2	RB8	**Receiver Bit 8/Ninth bit received in modes 2 and 3** Cleared by hardware if 9th bit received is a logic 0. Set by hardware if 9th bit received is a logic 1. In mode 1, if SM2 = 0, RB8 is the received stop bit. In mode 0 RB8 is not used.
1	TI	**Transmit Interrupt flag** Clear to acknowledge interrupt. Set by hardware at the end of the 8th bit time in mode 0 or at the beginning of the stop bit in the other modes.
0	RI	**Receive Interrupt flag** Clear to acknowledge interrupt. Set by hardware at the end of the 8th bit time in mode 0, see Figure 15-2. and Figure 15-3. in the other modes.

Reset Value = 0000 0000b

Bit addressable

Each interrupt source can also be individually programmed to one out of four priority levels by setting or clearing a bit in the Interrupt Priority register (Table 16-3.) and in the Interrupt Priority High register (Table 16-4). Table 16-1. shows the bit values and priority levels associated with each combination.

16.2 Registers

The PCA interrupt vector is located at address 0033H, the SPI interrupt vector is located at address 004BH and Keyboard interrupt vector is located at address 003BH. All other vectors addresses are the same as standard C52 devices.

Table 16-1. Priority Level Bit Values

IPH.x	IPL.x	Interrupt Level Priority
0	0	0 (Lowest)
0	1	1
1	0	2
1	1	3 (Highest)

A low-priority interrupt can be interrupted by a high priority interrupt, but not by another low-priority interrupt. A high-priority interrupt can't be interrupted by any other interrupt source.

If two interrupt requests of different priority levels are received simultaneously, the request of higher priority level is serviced. If interrupt requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence.

Table 16-2. IEN0 Register

IEN0 - Interrupt Enable Register (A8h)

7	6	5	4	3	2	1	0
EA	EC	ET2	ES	ET1	EX1	ET0	EX0

16.3 Interrupt Sources and Vector Addresses

Table 16-8. Vector Table

Number	Polling Priority	Interrupt Source	Interrupt Request	Vector Address
0	0	Reset		0000h
1	1	INT0	IE0	0003h
2	2	Timer 0	TF0	000Bh
3	3	INT1	IE1	0013h
4	4	Timer 1	IF1	001Bh
5	6	UART	RI+TI	0023h
6	7	Timer 2	TF2+EXF2	002Bh
7	5	PCA	CF + CCFn (n = 0-4)	0033h
8	8	Keyboard	KBDIT	003Bh
9	9	TWI	TWIIT	0043h
10	10	SPI	SPIIT	004Bh
11	11			0053h
12	12			005Bh
13	13			0063h
14	14	USB	UEPINT + USBINT	006Bh
15	15			0073h

address and the data direction bit (SLA+R). The serial interrupt flag SI must then be cleared before the serial transfer can continue.

When the slave address and the direction bit have been transmitted and an acknowledgement bit has been received, the serial interrupt flag is set again and a number of status code in SSCS are possible. There are 40h, 48h or 38h for the master mode and also 68h, 78h or B0h if the slave mode was enabled (AA=logic 1). The appropriate action to be taken for each of these status code is detailed in Table . This scheme is repeated until a STOP condition is transmitted.

SSIE, CR2, CR1 and CR0 are not affected by the serial transfer and are referred to Table 7 to Table 11. After a repeated START condition (state 10h) the TWI module may switch to the master transmitter mode by loading SSDAT with SLA+W.

20.1.3 Slave Receiver Mode

In the slave receiver mode, a number of data bytes are received from a master transmitter (Figure 20-6). To initiate the slave receiver mode, SSADR and SSCON must be loaded as follows:

Table 20-2. SSADR: Slave Receiver Mode Initialization

A6	A5	A4	A3	A2	A1	A0	GC
own slave address							

The upper 7 bits are the address to which the TWI module will respond when addressed by a master. If the LSB (GC) is set the TWI module will respond to the general call address (00h); otherwise it ignores the general call address.

Table 20-3. SSCON: Slave Receiver Mode Initialization

CR2	SSIE	STA	STO	SI	AA	CR1	CR0
bit rate	1	0	0	0	1	bit rate	bit rate

CR0, CR1 and CR2 have no effect in the slave mode. SSIE must be set to enable the TWI. The AA bit must be set to enable the own slave address or the general call address acknowledgement. STA, STO and SI must be cleared.

When SSADR and SSCON have been initialised, the TWI module waits until it is addressed by its own slave address followed by the data direction bit which must be at logic 0 (W) for the TWI to operate in the slave receiver mode. After its own slave address and the W bit have been received, the serial interrupt flag is set and a valid status code can be read from SSCS. This status code is used to vector to an interrupt service routine.The appropriate action to be taken for each of these status code is detailed in Table . The slave receiver mode may also be entered if arbitration is lost while TWI is in the master mode (states 68h and 78h).

If the AA bit is reset during a transfer, TWI module will return a not acknowledge (logic 1) to SDA after the next received data byte. While AA is reset, the TWI module does not respond to its own slave address. However, the 2-wire bus is still monitored and address recognition may be resume at any time by setting AA. This means that the AA bit may be used to temporarily isolate the module from the 2-wire bus.

Figure 20-7. Format and State in the Slave Transmitter Mode

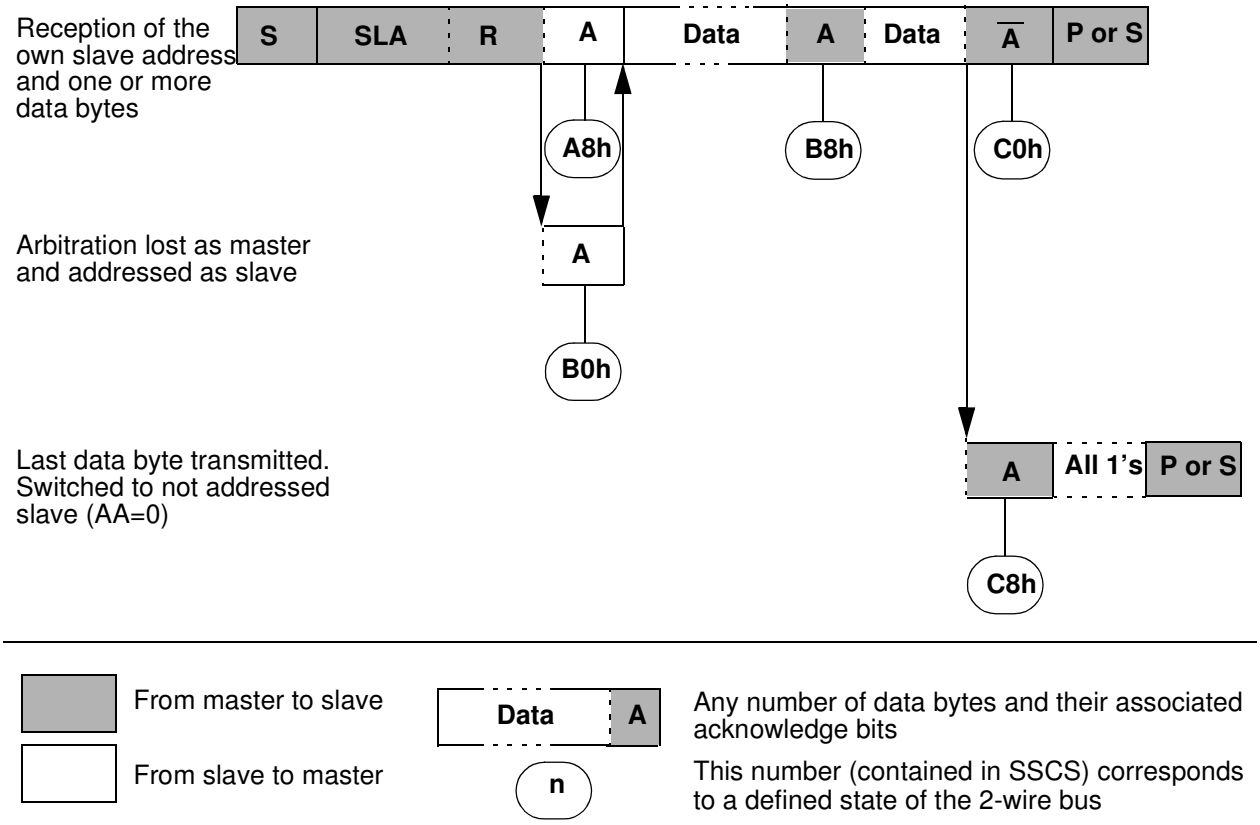
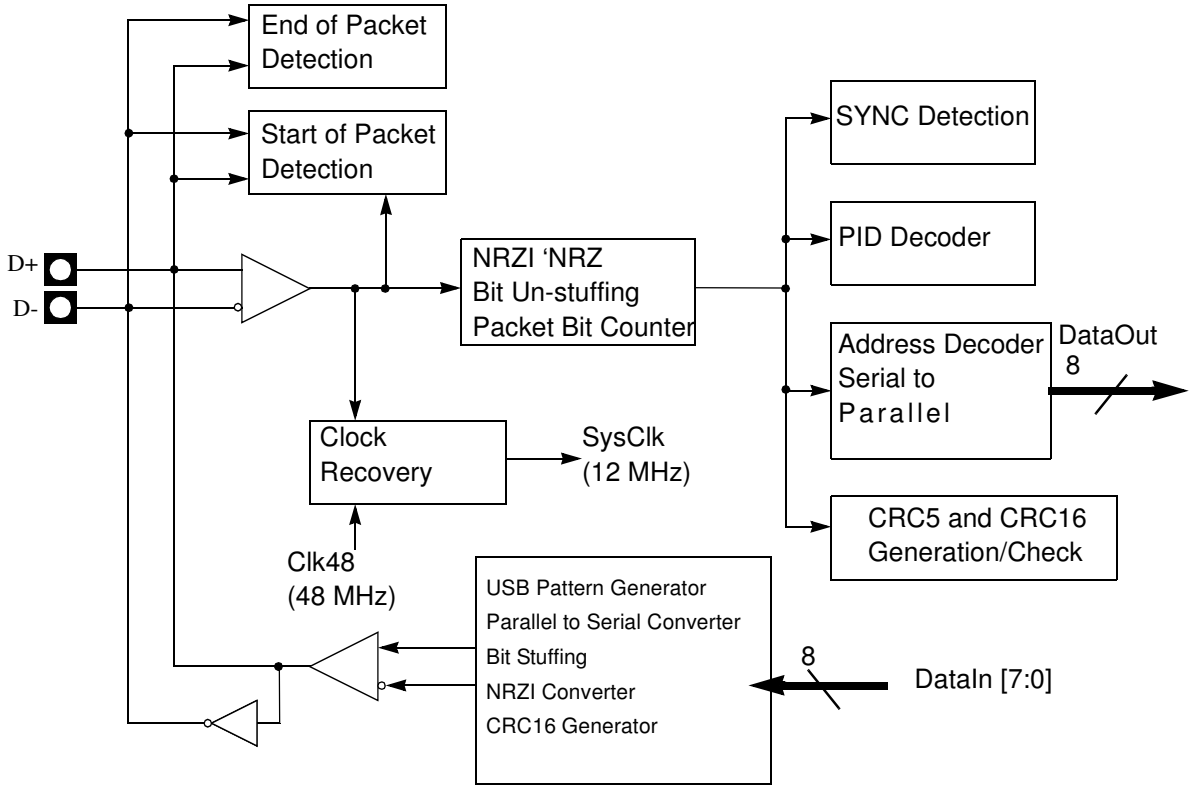


Table 20-8. Status in Slave Transmitter Mode

Status Code (SSCS)	Status of the 2-wire bus and 2-wire hardware	Application Software Response					Next Action Taken By 2-wire Software
		To/from SSDAT	To SSCON				
			STA	STO	SI	AA	
A8h	Own SLA+R has been received; ACK has been returned	Load data byte or	X	0	0	0	Last data byte will be transmitted and NOT ACK will be received
		Load data byte	X	0	0	1	Data byte will be transmitted and ACK will be received
B0h	Arbitration lost in SLA+R/W as master; own SLA+R has been received; ACK has been returned	Load data byte or	X	0	0	0	Last data byte will be transmitted and NOT ACK will be received
		Load data byte	X	0	0	1	Data byte will be transmitted and ACK will be received
B8h	Data byte in SSDAT has been transmitted; NOT ACK has been received	Load data byte or	X	0	0	0	Last data byte will be transmitted and NOT ACK will be received
		Load data byte	X	0	0	1	Data byte will be transmitted and ACK will be received

- Address checking.
- Clock generation (via DPLL).

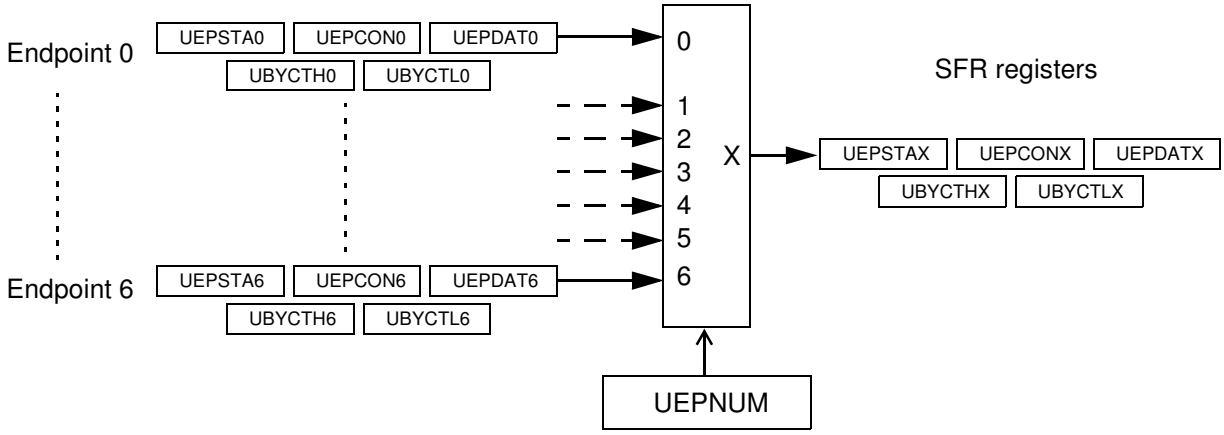
Figure 21-2. SIE Block Diagram



21.1.2 Function Interface Unit (FIU)

The Function Interface Unit provides the interface between the AT89C5131 and the SIE. It manages transactions at the packet level with minimal intervention from the device firmware, which reads and writes the endpoint FIFOs.

Figure 21-6. Endpoint FIFO Configuration



21.3.2 Read Data FIFO

The read access for each OUT endpoint is performed using the UEPDATX register.

After a new valid packet has been received on an Endpoint, the data are stored into the FIFO and the byte counter of the endpoint is updated (UBYCTLX and UBYCTHX registers). The firmware has to store the endpoint byte counter before any access to the endpoint FIFO. The byte counter is not updated when reading the FIFO.

To read data from an endpoint, select the correct endpoint number in UEPNUM and read the UEPDATX register. This action automatically decreases the corresponding address vector, and the next data is then available in the UEPDATX register.

21.3.3 Write Data FIFO

The write access for each IN endpoint is performed using the UEPDATX register.

To write a byte into an IN endpoint FIFO, select the correct endpoint number in UEPNUM and write into the UEPDATX register. The corresponding address vector is automatically increased, and another write can be carried out.

Warning 1: The byte counter is not updated.
Warning 2: Do not write more bytes than supported by the corresponding endpoint.

21.4 Bulk/Interrupt Transactions

Bulk and Interrupt transactions are managed in the same way.

Table 21-5. USBIEN Register
USBIEN (S:BEh)
USB Global Interrupt Enable Register

7	6	5	4	3	2	1	0
-	-	EWUPCPU	EEORINT	ESOFINT	-	-	ESPINT

Bit Number	Bit Mnemonic	Description
7-6	-	**Reserved** The value read from these bits is always 0. Do not set these bits.
5	EWUPCPU	**Enable Wake Up CPU Interrupt** Set this bit to enable Wake Up CPU Interrupt. (See "USBIEN Register USBIEN (S:BEh) USB Global Interrupt Enable Register" on page 141.) Clear this bit to disable Wake Up CPU Interrupt.
4	EEORINT	**Enable End Of Reset Interrupt** Set this bit to enable End Of Reset Interrupt. (See "USBIEN Register USBIEN (S:BEh) USB Global Interrupt Enable Register" on page 141.). This bit is set after reset. Clear this bit to disable End Of Reset Interrupt.
3	ESOFINT	**Enable SOF Interrupt** Set this bit to enable SOF Interrupt. (See "USBIEN Register USBIEN (S:BEh) USB Global Interrupt Enable Register" on page 141.). Clear this bit to disable SOF Interrupt.
2	-	**Reserved** The value read from these bits is always 0. Do not set these bits.
1	-	
0	ESPINT	**Enable Suspend Interrupt** Set this bit to enable Suspend Interrupts (see the "USBIEN Register USBIEN (S:BEh) USB Global Interrupt Enable Register" on page 141). Clear this bit to disable Suspend Interrupts.

Reset Value = 10h

Table 21-14. UEPINT Register
UEPINT (S:F8h read-only)
USB Endpoint Interrupt Register

7	6	5	4	3	2	1	0
-	EP6INT	EP5INT	EP4INT	EP3INT	EP2INT	EP1INT	EP0INT

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is always 0. Do not set this bit.
6	EP6INT	Endpoint 6 Interrupt This bit is set by hardware when an endpoint interrupt source has been detected on the endpoint 6. The endpoint interrupt sources are in the UEPSTAX register and can be: TXCMP, RXOUTB0, RXOUTB1, RXSETUP or STLCRC. A USB interrupt is triggered when the EP6IE bit in the UEPIEN register is set. This bit is cleared by hardware when all the endpoint interrupt sources are cleared
5	EP5INT	Endpoint 5 Interrupt This bit is set by hardware when an endpoint interrupt source has been detected on the endpoint 5. The endpoint interrupt sources are in the UEPSTAX register and can be: TXCMP, RXOUTB0, RXOUTB1, RXSETUP or STLCRC. A USB interrupt is triggered when the EP5IE bit in the UEPIEN register is set. This bit is cleared by hardware when all the endpoint interrupt sources are cleared
4	EP4INT	Endpoint 4 Interrupt This bit is set by hardware when an endpoint interrupt source has been detected on the endpoint 4. The endpoint interrupt sources are in the UEPSTAX register and can be: TXCMP, RXOUTB0, RXOUTB1, RXSETUP or STLCRC. A USB interrupt is triggered when the EP4IE bit in the UEPIEN register is set. This bit is cleared by hardware when all the endpoint interrupt sources are cleared
3	EP3INT	Endpoint 3 Interrupt This bit is set by hardware when an endpoint interrupt source has been detected on the endpoint 3. The endpoint interrupt sources are in the UEPSTAX register and can be: TXCMP, RXOUTB0, RXOUTB1, RXSETUP or STLCRC. A USB interrupt is triggered when the EP3IE bit in the UEPIEN register is set. This bit is cleared by hardware when all the endpoint interrupt sources are cleared
2	EP2INT	Endpoint 2 Interrupt This bit is set by hardware when an endpoint interrupt source has been detected on the endpoint 2. The endpoint interrupt sources are in the UEPSTAX register and can be: TXCMP, RXOUTB0, RXOUTB1, RXSETUP or STLCRC. A USB interrupt is triggered when the EP2IE bit in the UEPIEN register is set. This bit is cleared by hardware when all the endpoint interrupt sources are cleared
1	EP1INT	Endpoint 1 Interrupt This bit is set by hardware when an endpoint interrupt source has been detected on the endpoint 1. The endpoint interrupt sources are in the UEPSTAX register and can be: TXCMP, RXOUTB0, RXOUTB1, RXSETUP or STLCRC. A USB interrupt is triggered when the EP1IE bit in the UEPIEN register is set. This bit is cleared by hardware when all the endpoint interrupt sources are cleared
0	EP0INT	Endpoint 0 Interrupt This bit is set by hardware when an endpoint interrupt source has been detected on the endpoint 0. The endpoint interrupt sources are in the UEPSTAX register and can be: TXCMP, RXOUTB0, RXOUTB1, RXSETUP or STLCRC. A USB interrupt is triggered when the EP0IE bit in the UEPIEN register is set. This bit is cleared by hardware when all the endpoint interrupt sources are cleared

Reset Value = 00h

Table 21-16. UFNUMH Register
UFNUMH (S:BBh, read-only)
USB Frame Number High Register

7	6	5	4	3	2	1	0
-	-	CRCOK	CRCERR	-	FNUM10	FNUM9	FNUM8

Bit Number	Bit Mnemonic	Description
5	CRCOK	**Frame Number CRC OK** This bit is set by hardware when a new Frame Number in Start of Frame Packet is received without CRC error. This bit is updated after every Start of Frame packet receipt. Important note: the Start of Frame interrupt is generated just after the PID receipt.
4	CRCERR	**Frame Number CRC Error** This bit is set by hardware when a corrupted Frame Number in Start of Frame packet is received. This bit is updated after every Start of Frame packet receipt. Important note: the Start of Frame interrupt is generated just after the PID receipt.
3	-	**Reserved** The value read from this bit is always 0. Do not set this bit.
2-0	FNUM[10:8]	**Frame Number** FNUM[10:8] are the upper 3 bits of the 11-bit Frame Number (see the "UFNUML Register UFNUML (S:BAh, read-only) USB Frame Number Low Register" on page 150). It is provided in the last received SOF packet (see SOFINT in the "USBIEN Register USBIEN (S:BEh) USB Global Interrupt Enable Register" on page 141). FNUM is updated if a corrupted SOF is received.

Reset Value = 00h

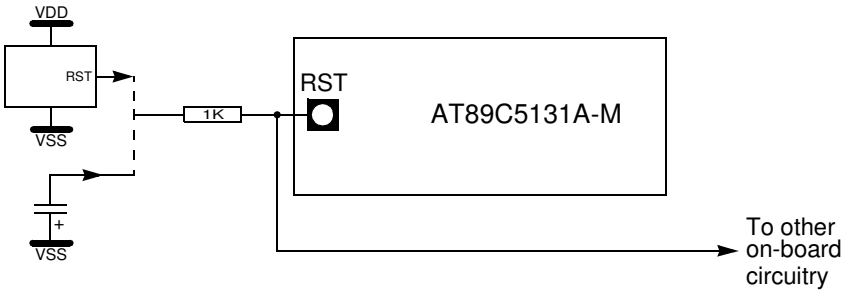
Table 21-17. UFNUML Register
UFNUML (S:BAh, read-only)
USB Frame Number Low Register

7	6	5	4	3	2	1	0
FNUM7	FNUM6	FNUM5	FNUM4	FNUM3	FNUM2	FNUM1	FNUM0

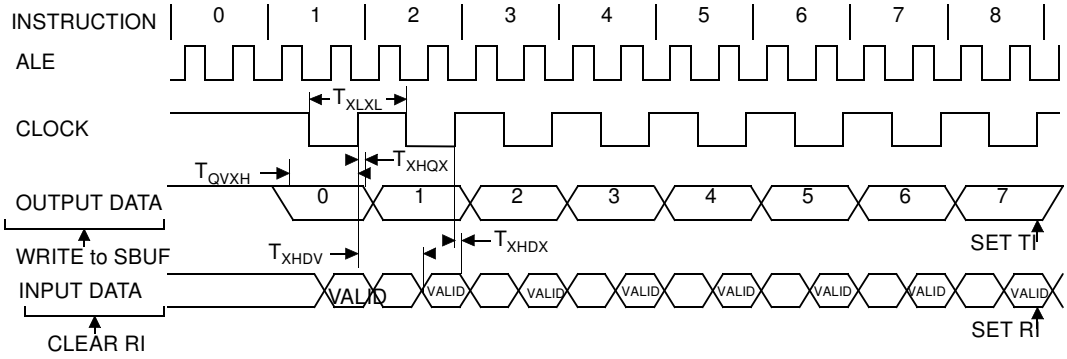
Bit Number	Bit Mnemonic	Description
7 - 0	FNUM[7:0]	**Frame Number** FNUM[7:0] are the lower 8 bits of the 11-bit Frame Number (See "UFNUMH Register UFNUMH (S:BBh, read-only) USB Frame Number High Register" on page 150.).

Reset Value = 00h

Figure 22-3. Recommended Reset Output Schematic



27.4.8 Shift Register Timing Waveform

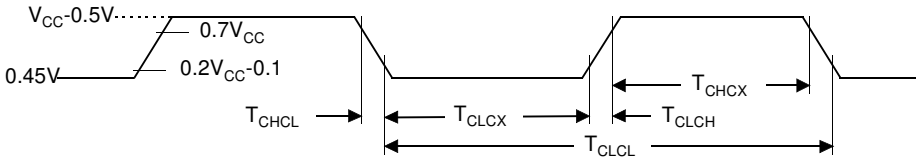


27.4.9 External Clock Drive Characteristics (XTAL1)

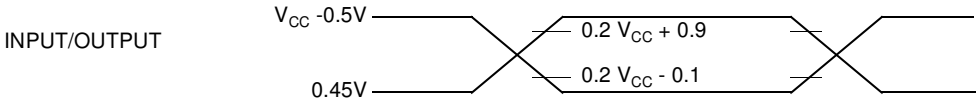
Table 27-11. AC Parameters

Symbol	Parameter	Min	Max	Units
T_{CLCL}	Oscillator Period	21		ns
T_{CHCX}	High Time	5		ns
T_{CLCX}	Low Time	5		ns
T_{CLCH}	Rise Time		5	ns
T_{CHCL}	Fall Time		5	ns
T_{CHCX}/T_{CLCX}	Cyclic ratio in X2 mode	40	60	%

27.4.10 External Clock Drive Waveforms

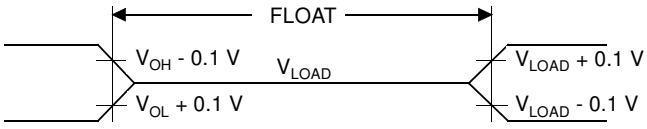


27.4.11 AC Testing Input/Output Waveforms



AC inputs during testing are driven at V_{CC} - 0.5 for a logic “1” and 0.45V for a logic “0”. Timing measurement are made at V_{IH} min for a logic “1” and V_{IL} max for a logic “0”.

27.4.12 Float Waveforms



For timing purposes as port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} \geq \pm 20$ mA.

V_{DD} = 2.7 to 5.5 V, T_A = -40 to +85°C

Symbol	Parameter	Min	Max	Unit
Slave Mode				
T_{CHCH}	Clock Period	2		T_{PER}
T_{CHCX}	Clock High Time	0.8		T_{PER}
T_{CLCX}	Clock Low Time	0.8		T_{PER}
T_{SLCH}, T_{SLCL}	$\overline{SS}$ Low to Clock edge	100		ns
T_{IVCL}, T_{IVCH}	Input Data Valid to Clock Edge	50		ns
T_{CLIX}, T_{CHIX}	Input Data Hold after Clock Edge	50		ns
$T_{CLOV,}$ T_{CHOV}	Output Data Valid after Clock Edge		50	ns
T_{CLOX}, T_{CHOX}	Output Data Hold Time after Clock Edge	0		ns
T_{CLSH}, T_{CHSH}	$\overline{SS}$ High after Clock Edge	0		ns
T_{SLOV}	$\overline{SS}$ Low to Output Data Valid		$4T_{PER}$+20	ns
T_{SHOX}	Output Data Hold after $\overline{SS}$ High		$2T_{PER}$+100	ns
T_{SHSL}	$\overline{SS}$ High to $\overline{SS}$ Low	$2T_{PER}$+120		
T_{ILIH}	Input Rise Time		2	µs
T_{IHIL}	Input Fall Time		2	µs
T_{OLOH}	Output Rise time		100	ns
T_{OHOL}	Output Fall Time		100	ns
Master Mode				
T_{CHCH}	Clock Period	4		T_{PER}
T_{CHCX}	Clock High Time	$2T_{PER}$-20		ns
T_{CLCX}	Clock Low Time	$2T_{PER}$-20		ns
T_{IVCL}, T_{IVCH}	Input Data Valid to Clock Edge	50		ns
T_{CLIX}, T_{CHIX}	Input Data Hold after Clock Edge	50		ns
$T_{CLOV,}$ T_{CHOV}	Output Data Valid after Clock Edge		20	ns
T_{CLOX}, T_{CHOX}	Output Data Hold Time after Clock Edge	0		ns

Note: T_{PER} is XTAL period when SPI interface operates in X2 mode or twice XTAL period when SPI interface operates in X1 mode.

28. Ordering Information

Table 28-1. Possible Order Entries

Part Number	Memory Size (Kbytes)	Supply Voltage	Temperature Range	Package	Packing
AT89C5130A-RDTUM	16	2.7 to 5.5V	Industrial & Green	VQFP64	Tray & Dry Pack
AT89C5130A-PUTUM	16	2.7 to 5.5V	Industrial & Green	QFN32	Tray & Dry Pack
AT89C5130A-S3SUM	16	2.7 to 5.5V	Industrial & Green	PLCC52	Stick
AT89C5131A-RDTUM	32	2.7 to 5.5V	Industrial & Green	VQFP64	Tray & Dry Pack
AT89C5131A-PUTUM	32	2.7 to 5.5V	Industrial & Green	QFN32	Tray & Dry Pack
AT89C5131A-S3SUM	32	2.7 to 5.5V	Industrial & Green	PLCC52	Stick

Notes: 1. Optional Packing and Package options (please consult Atmel sales representative)
-Tape and Reel
-Die form