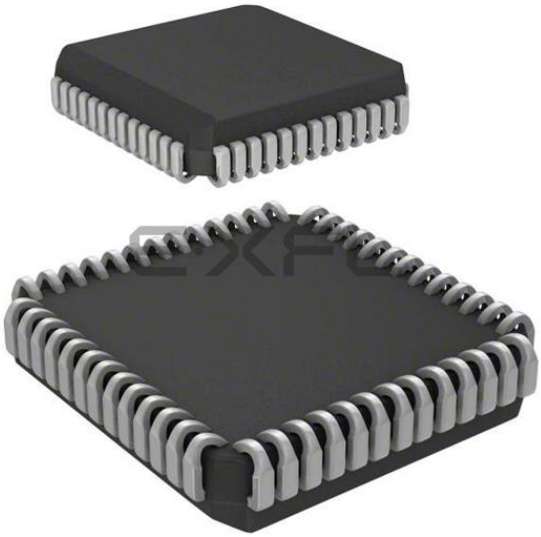


Welcome to E-XFL.COM

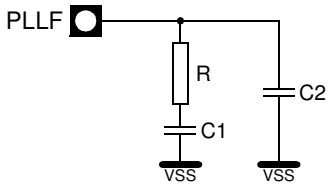
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	80C51
Core Size	8-Bit
Speed	48MHz
Connectivity	I²C, SPI, UART/USART, USB
Peripherals	LED, POR, PWM, WDT
Number of I/O	34
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	1.25K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	52-LCC (J-Lead)
Supplier Device Package	52-PLCC (19.15x19.15)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at89c5130a-s3sum

Figure 5-4. PLL Filter Connection

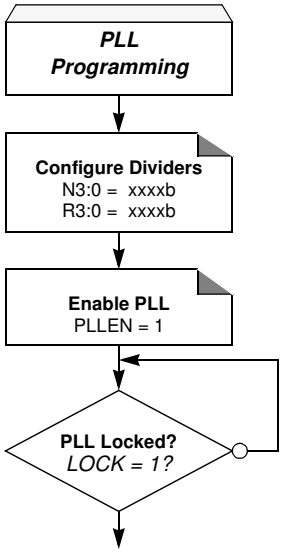


The typical values are: R = 100 Ω, C1 = 10 nf, C2 = 2.2 nF.

5.3.2 PLL Programming

The PLL is programmed using the flow shown in Figure 5-5. As soon as clock generation is enabled user must wait until the lock indicator is set to ensure the clock output is stable.

Figure 5-5. PLL Programming Flow



5.3.3 Divider Values

To generate a 48 MHz clock using the PLL, the divider values have to be configured following the oscillator frequency. The typical divider values are shown in Table 5-1.

Table 5-1. Typical Divider Values

Oscillator Frequency	R+1	N+1	PLLDIV
3 MHz	16	1	F0h
6 MHz	8	1	70h
8 MHz	6	1	50h
12 MHz	4	1	30h
16 MHz	3	1	20h
18 MHz	8	3	72h
20 MHz	12	5	B4h
24 MHz	2	1	10h

Reset Value = 0000 0000b

Table 5-3. CKCON1 (S:AFh)
Clock Control Register 1

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	SPIX2

Bit Number	Bit Mnemonic	Description
7-1	-	**Reserved** The value read from this bit is always 0. Do not set this bit.
0	SPIX2	**SPI Clock** **This control bit is validated when the CPU clock X2 is set. When X2 is low, this bit has no effect.** Clear to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.

Reset Value = 0000 0000b

Table 5-4. PLLCON (S:A3h)
PLL Control Register

7	6	5	4	3	2	1	0
-	-	-	-	-	EXT48	PLLEN	PLOCK

Bit Number	Bit Mnemonic	Description
7-3	-	**Reserved** The value read from this bit is always 0. Do not set this bit.
2	EXT48	**External 48 MHz Enable Bit** Set this bit to bypass the PLL and disable the crystal oscillator. Clear this bit to select the PLL output as USB clock and to enable the crystal oscillator.
1	PLLEN	**PLL Enable Bit** Set to enable the PLL. Clear to disable the PLL.
0	PLOCK	**PLL Lock Indicator** Set by hardware when PLL is locked. Clear by hardware when PLL is unlocked.

Reset Value = 0000 0000b

Table 5-5. PLLDIV (S:A4h)
PLL Divider Register

7	6	5	4	3	2	1	0
R3	R2	R1	R0	N3	N2	N1	N0

The table below shows all SFRs with their address and their reset value.

Table 6-1. SFR Descriptions

	Bit Addressable	**Non-Bit Addressable**							
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	
F8h	UEPINT 0000 0000	CH 0000 0000	CCAP0H XXXX XXXX	CCAP1H XXXX XXXX	CCAP2H XXXX XXXX	CCAP3H XXXX XXXX	CCAP4H XXXX XXXX		FFh
F0h	B 0000 0000	LEDCON 0000 0000							F7h
E8h		CL 0000 0000	CCAP0L XXXX XXXX	CCAP1L XXXX XXXX	CCAP2L XXXX XXXX	CCAP3L XXXX XXXX	CCAP4L XXXX XXXX		EFh
E0h	ACC 0000 0000		UBYCTLX 0000 0000	UBYCTHX 0000 0000					E7h
D8h	CCON 00X0 0000	CMOD 00XX X000	CCAPM0 X000 0000	CCAPM1 X000 0000	CCAPM2 X000 0000	CCAPM3 X000 0000	CCAPM4 X000 0000		DFh
D0h	PSW 0000 0000	FCON (1) XXXX 0000	EECON XXXX XX00		UEPCONX 1000 0000	UEPRST 0000 0000			D7h
C8h	T2CON 0000 0000	T2MOD XXXX XX00	RCAP2L 0000 0000	RCAP2H 0000 0000	TL2 0000 0000	TH2 0000 0000	UEPSTAX 0000 0000	UEPDATX 0000 0000	CFh
C0h	P4 XXXX 1111		UEPIEN 0000 0000	SPCON 0001 0100	SPSTA 0000 0000	SPDAT XXXX XXXX	USBADDR 1000 0000	UEPNUM 0000 0000	C7h
B8h	IPL0 X000 000	SADEN 0000 0000	UFNUML 0000 0000	UFNUMH 0000 0000	USBCON 0000 0000	USBINT 0000 0000	USBIEN 0000 0000		BFh
B0h	P3 1111 1111	IEN1 X0XX X000	IPL1 X0XX X000	IPH1 X0XX X000				IPH0 X000 0000	B7h
A8h	IEN0 0000 0000	SADDR 0000 0000						CKCON1 0000 0000	AFh
A0h	P2 1111 1111		AUXR1 XXXX X0X0	PLLCON XXXX XX00	PLLDIV 0000 0000		WDTRST XXXX XXXX	WDTPRG XXXX X000	A7h
98h	SCON 0000 0000	SBUF XXXX XXXX	BRL 0000 0000	BDRCON XXX0 0000	KBLS 0000 0000	KBE 0000 0000	KBF 0000 0000		9Fh
90h	P1 1111 1111			SSCON 0000 0000	SSCS 1111 1000	SSDAT 1111 1111	SSADR 1111 1110		97h
88h	TCON 0000 0000	TMOD 0000 0000	TL0 0000 0000	TL1 0000 0000	TH0 0000 0000	TH1 0000 0000	AUXR XX0X 0000	CKCON0 0000 0000	8Fh
80h	P0 1111 1111	SP 0000 0111	DPL 0000 0000	DPH 0000 0000				PCON 00X1 0000	87h
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	

Note: 1. FCON access is reserved for the Flash API and ISP software.

Reserved

8.2.1.4 *Column Latches*

The column latches, also part of FM0, have a size of full page (128 bytes).
The column latches are the entrance buffers of the three previous memory locations (user array, XRow and Hardware security byte).

8.3 Overview of FM0 Operations

The CPU interfaces to the Flash memory through the FCON register and AUXR1 register.

These registers are used to:

- Map the memory spaces in the adressable space
- Launch the programming of the memory spaces
- Get the status of the Flash memory (busy/not busy)
- Select the Flash memory FM0/FM1.

8.3.1 Mapping of the Memory Space

By default, the user space is accessed by MOVC instruction for read only. The column latches space is made accessible by setting the FPS bit in FCON register. Writing is possible from 0000h to 3FFFH/7FFFh, address bits 6 to 0 are used to select an address within a page while bits 14 to 7 are used to select the programming address of the page.

Setting this bit takes precedence on the EXTRAM bit in AUXR register.

The other memory spaces (user, extra row, hardware security) are made accessible in the code segment by programming bits FMOD0 and FMOD1 in FCON register in accordance with Table 8-2. A MOVC instruction is then used for reading these spaces.

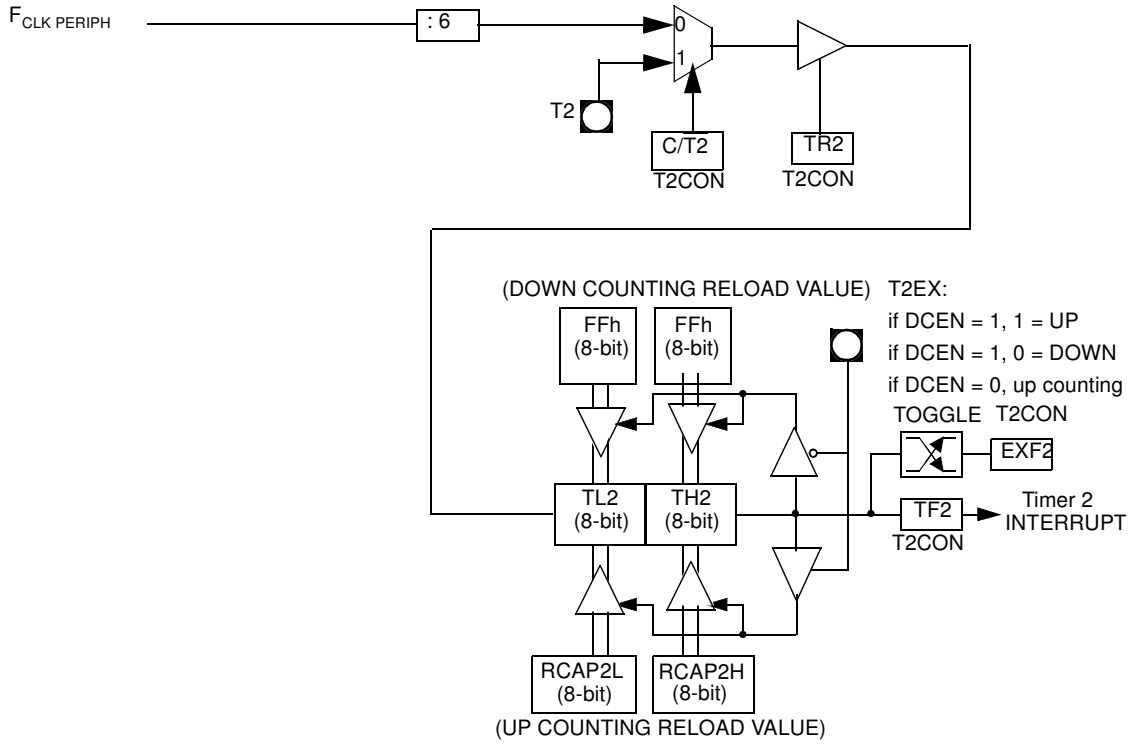
Table 8-2. FM0 Blocks Select Bits

FMOD1	FMOD0	FM0 Adressable Space
0	0	User (0000h-FFFFh)
0	1	Extra Row(FF80h-FFFFh)
1	0	Hardware Security (0000h)
1	1	reserved

8.3.2 Launching Programming

FPL3:0 bits in FCON register are used to secure the launch of programming. A specific sequence must be written in these bits to unlock the write protection and to launch the programming. This sequence is 5 followed by A. Table 8-3 summarizes the memory spaces to program according to FMOD1:0 bits.

Figure 13-1. Auto-reload Mode Up/Down Counter (DCEN = 1)



13.2 Programmable Clock Output

In the Clock-out mode, Timer 2 operates as a 50%-duty-cycle, programmable clock generator (See Figure 13-2). The input clock increments TL2 at frequency $F_{CLK\ PERIPH}/2$. The timer repeatedly counts to overflow from a loaded value. At overflow, the contents of RCAP2H and RCAP2L registers are loaded into TH2 and TL2. In this mode, Timer 2 overflows do not generate interrupts. The following formula gives the Clock-out frequency as a function of the system oscillator frequency and the value in the RCAP2H and RCAP2L registers

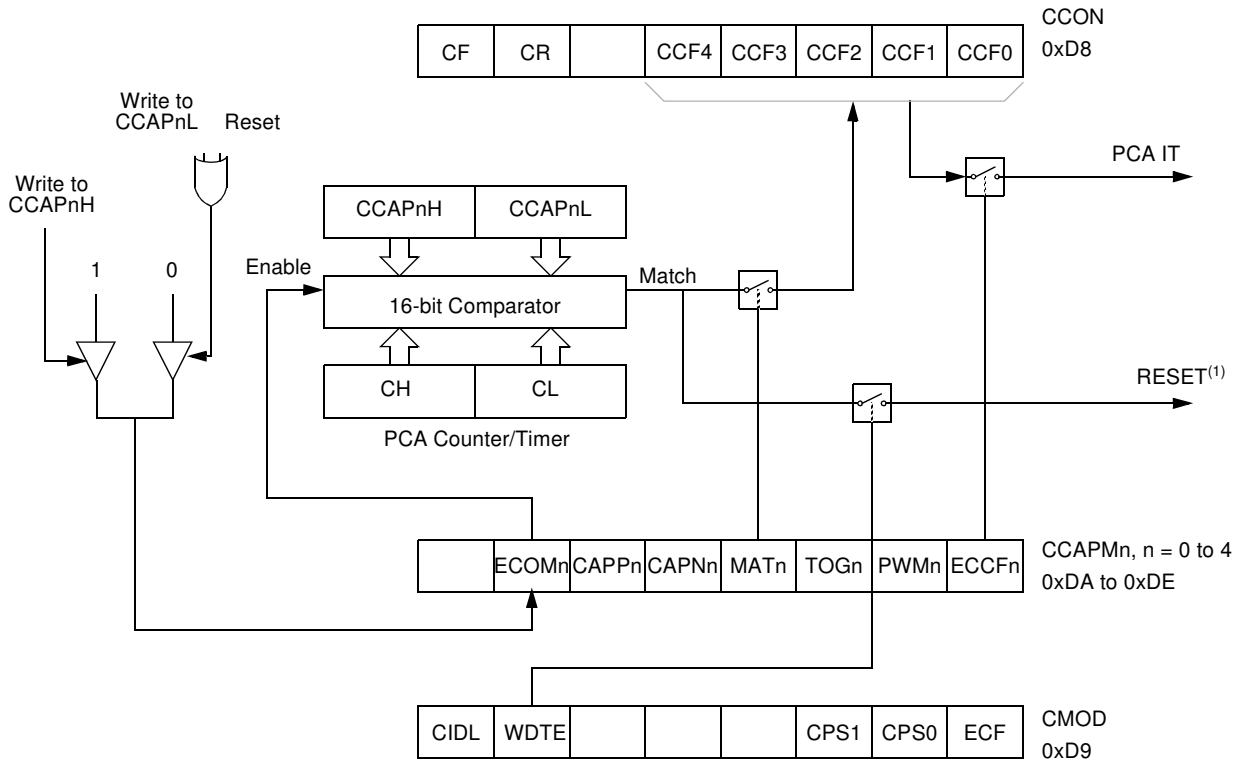
$$Clock-OutFrequency = \frac{F_{CLKPERIPH}}{4 \times (65536 - RCAP2H/RCAP2L)}$$

For a 16 MHz system clock, Timer 2 has a programmable frequency range of 61 Hz ($F_{CLK\ PERIPH}/2^{16)}$ to 4 MHz ($F_{CLK\ PERIPH}/4$). The generated clock signal is brought out to T2 pin (P1.0).

Timer 2 is programmed for the Clock-out mode as follows:

- Set T2OE bit in T2MOD register.
- Clear C/$\overline{T2}$ bit in T2CON register.
- Determine the 16-bit reload value from the formula and enter it in RCAP2H/RCAP2L registers.
- Enter a 16-bit initial value in timer registers TH2/TL2. It can be the same as the reload value or a different one depending on the application.
- To start the timer, set TR2 run control bit in T2CON register.

Figure 14-4. PCA Compare Mode and PCA Watchdog Timer



Note: 1. Only for Module 4

Before enabling ECOM bit, CCAPnL and CCAPnH should be set with a non zero value, otherwise an unwanted match could happen. Writing to CCAPnH will set the ECOM bit.

Once ECOM set, writing CCAPnL will clear ECOM so that an unwanted match doesn't occur while modifying the compare value. Writing to CCAPnH will set ECOM. For this reason, user software should write CCAPnL first, and then CCAPnH. Of course, the ECOM bit can still be controlled by accessing to CCAPMn register.

14.3 High Speed Output Mode

In this mode, the CEX output (on port 1) associated with the PCA module will toggle each time a match occurs between the PCA counter and the module's capture registers. To activate this mode the TOG, MAT, and ECOM bits in the module's CCAPMn SFR must be set (see Figure 14-5).

A prior write must be done to CCAPnL and CCAPnH before writing the ECOMn bit.

Reset Value = X0XX X000b
Not bit addressable

Table 16-6. IPL1 Register

IPL1 - Interrupt Priority Register (B2h)

7	6	5	4	3	2	1	0
-	PUSBL	-	-	-	PSPIL	PTWIL	PKBDL

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	PUSBL	**USB Interrupt Priority bit** Refer to PUSBH for priority level.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
2	PSPIL	**SPI Interrupt Priority bit** Refer to PSPIH for priority level.
1	PTWIL	**TWI Interrupt Priority bit** Refer to PTWIH for priority level.
0	PKBL	**Keyboard Interrupt Priority bit** Refer to PKBH for priority level.

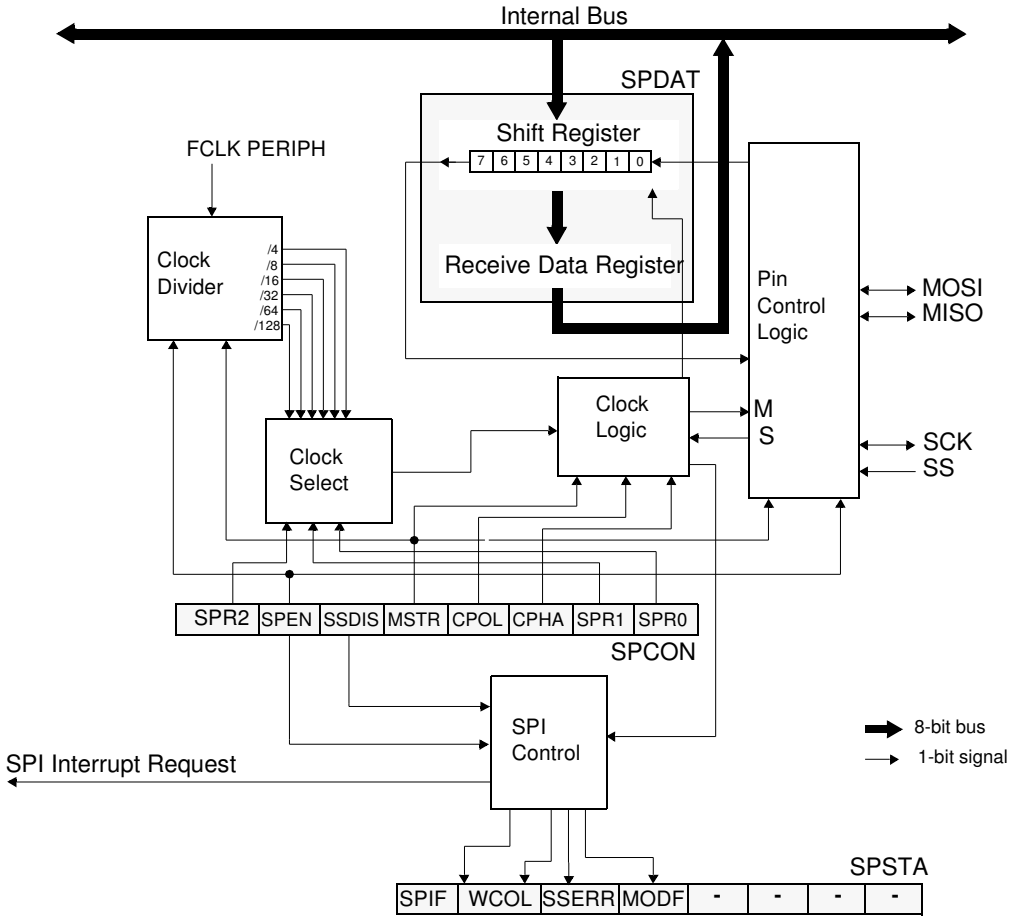
Reset Value = X0XX X000b
Not bit addressable

SPR2	SPR1	SPR0	Clock Rate	Baud Rate Divisor (BD)
1	1	1	Don't Use	No BRG

19.3 Functional Description

Figure 19-2 shows a detailed structure of the SPI module.

Figure 19-2. SPI Module Block Diagram



19.3.1 Operating Modes

The Serial Peripheral Interface can be configured as one of the two modes: Master mode or Slave mode. The configuration and initialization of the SPI module is made through one register:

- The Serial Peripheral CONtrol register (SPCON)

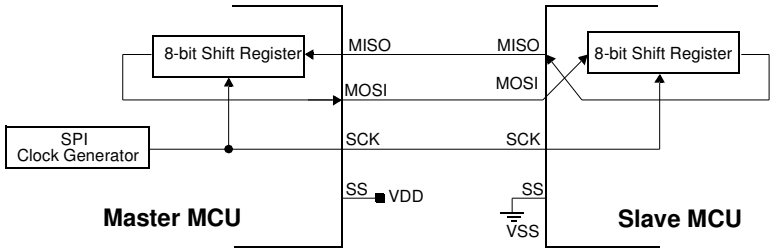
Once the SPI is configured, the data exchange is made using:

- SPCON
- The Serial Peripheral STAtus register (SPSTA)
- The Serial Peripheral DATa register (SPDAT)

During an SPI transmission, data is simultaneously transmitted (shifted out serially) and received (shifted in serially). A serial clock line (SCK) synchronizes shifting and sampling on the two serial data lines (MOSI and MISO). A Slave Select line ($\overline{SS}$) allows individual selection of a Slave SPI device; Slave devices that are not selected do not interfere with SPI bus activities.

When the Master device transmits data to the Slave device via the MOSI line, the Slave device responds by sending data to the Master device via the MISO line. This implies full-duplex transmission with both data out and data in synchronized with the same clock (Figure 19-3).

Figure 19-3. Full-duplex Master/Slave Interconnection



19.3.1.1 Master Mode

The SPI operates in Master mode when the Master bit, MSTR [1], in the SPCON register is set. Only one Master SPI device can initiate transmissions. Software begins the transmission from a Master SPI module by writing to the Serial Peripheral Data Register (SPDAT). If the shift register is empty, the byte is immediately transferred to the shift register. The byte begins shifting out on MOSI pin under the control of the serial clock, SCK. Simultaneously, another byte shifts in from the Slave on the Master's MISO pin. The transmission ends when the Serial Peripheral transfer data flag, SPIF, in SPSTA becomes set. At the same time that SPIF becomes set, the received byte from the Slave is transferred to the receive data register in SPDAT. Software clears SPIF by reading the Serial Peripheral Status register (SPSTA) with the SPIF bit set, and then reading the SPDAT.

19.3.1.2 Slave Mode

The SPI operates in Slave mode when the Master bit, MSTR [2], in the SPCON register is cleared. Before a data transmission occurs, the Slave Select pin, $\overline{SS}$, of the Slave device must be set to'0'. $\overline{SS}$ must remain low until the transmission is complete.

In a Slave SPI module, data enters the shift register under the control of the SCK from the Master SPI module. After a byte enters the shift register, it is immediately transferred to the receive data register in SPDAT, and the SPIF bit is set. To prevent an overflow condition, Slave software must then read the SPDAT before another byte enters the shift register [3]. A Slave SPI must complete the write to the SPDAT (shift register) at least one bus cycle before the Master SPI starts a transmission. If the write to the data register is late, the SPI transmits the data already in the shift register from the previous transmission.

19.3.2 Transmission Formats

Software can select any of four combinations of serial clock (SCK) phase and polarity using two bits in the SPCON: the Clock POLarity (CPOL [4]) and the Clock PHAse (CPHA[4]). CPOL defines the default SCK line level in idle state. It has no significant effect on the transmission format. CPHA defines the edges on which the input data are sampled and the edges on which the

1. The SPI module should be configured as a Master before it is enabled (SPEN set). Also the Master SPI should be configured before the Slave SPI.
2. The SPI module should be configured as a Slave before it is enabled (SPEN set).
3. The maximum frequency of the SCK for an SPI configured as a Slave is $F_{CLK\ PERIPH}/2$.
4. Before writing to the CPOL and CPHA bits, the SPI should be disabled (SPEN ='0').

output data are shifted (Figure 19-4 and Figure 19-5). The clock phase and polarity should be identical for the Master SPI device and the communicating Slave device.

Figure 19-4. Data Transmission Format (CPHA = 0)

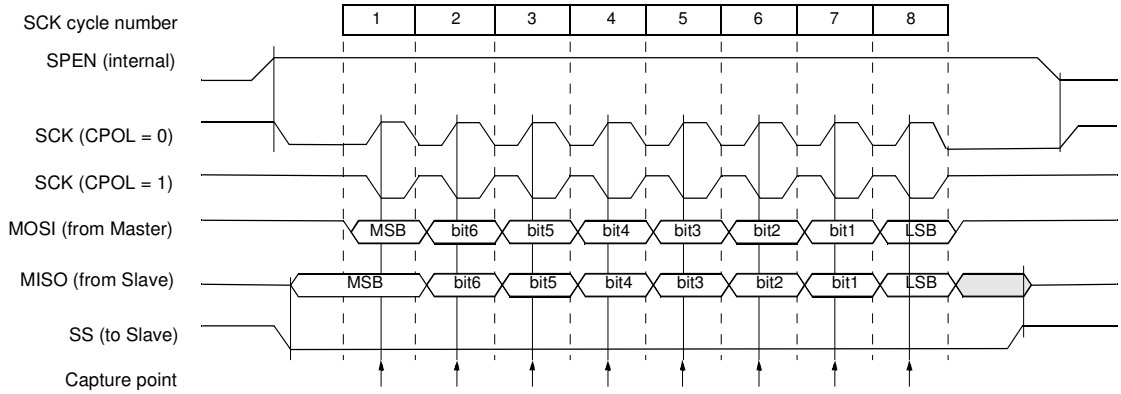


Figure 19-5. Data Transmission Format (CPHA = 1)

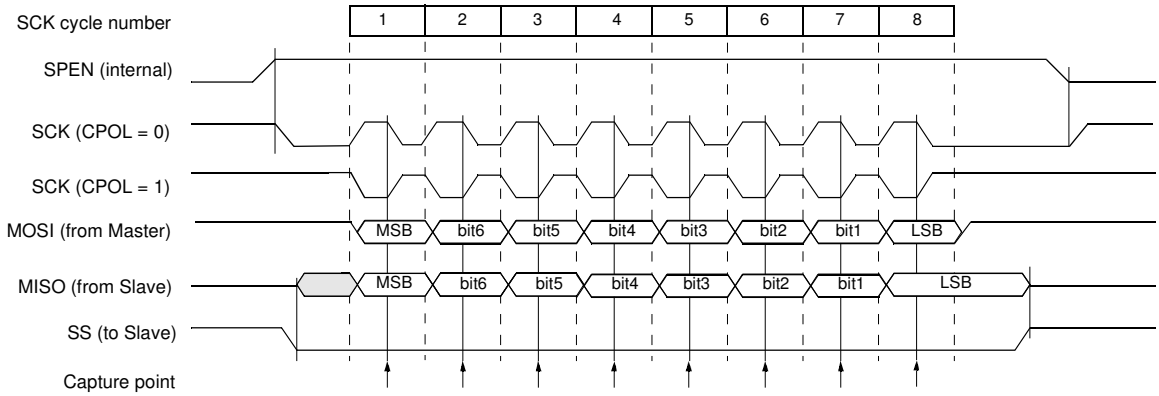
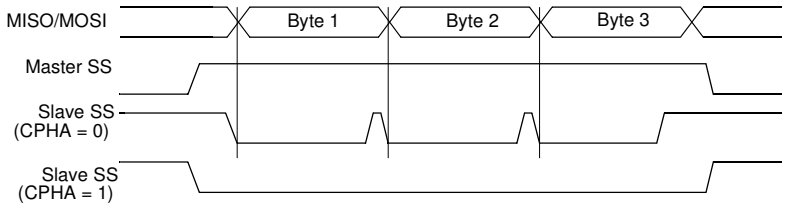


Figure 19-6. CPHA/$\overline{SS}$ Timing



As shown in Figure 19-5, the first SCK edge is the MSB capture strobe. Therefore the Slave must begin driving its data before the first SCK edge, and a falling edge on the $\overline{SS}$ pin is used to start the transmission. The $\overline{SS}$ pin must be toggled high and then low between each byte transmitted (Figure 19-2).

Figure 19-6 shows an SPI transmission in which CPHA is'1'. In this case, the Master begins driving its MOSI pin on the first SCK edge. Therefore the Slave uses the first SCK edge as a start transmission signal. The $\overline{SS}$ pin can remain low between transmissions (Figure 19-1). This format may be preferable in systems having only one Master and only one Slave driving the MISO data line.

address and the data direction bit (SLA+R). The serial interrupt flag SI must then be cleared before the serial transfer can continue.

When the slave address and the direction bit have been transmitted and an acknowledgement bit has been received, the serial interrupt flag is set again and a number of status code in SSCS are possible. There are 40h, 48h or 38h for the master mode and also 68h, 78h or B0h if the slave mode was enabled (AA=logic 1). The appropriate action to be taken for each of these status code is detailed in Table . This scheme is repeated until a STOP condition is transmitted.

SSIE, CR2, CR1 and CR0 are not affected by the serial transfer and are referred to Table 7 to Table 11. After a repeated START condition (state 10h) the TWI module may switch to the master transmitter mode by loading SSDAT with SLA+W.

20.1.3 Slave Receiver Mode

In the slave receiver mode, a number of data bytes are received from a master transmitter (Figure 20-6). To initiate the slave receiver mode, SSADR and SSCON must be loaded as follows:

Table 20-2. SSADR: Slave Receiver Mode Initialization

A6	A5	A4	A3	A2	A1	A0	GC
own slave address							

The upper 7 bits are the address to which the TWI module will respond when addressed by a master. If the LSB (GC) is set the TWI module will respond to the general call address (00h); otherwise it ignores the general call address.

Table 20-3. SSCON: Slave Receiver Mode Initialization

CR2	SSIE	STA	STO	SI	AA	CR1	CR0
bit rate	1	0	0	0	1	bit rate	bit rate

CR0, CR1 and CR2 have no effect in the slave mode. SSIE must be set to enable the TWI. The AA bit must be set to enable the own slave address or the general call address acknowledgement. STA, STO and SI must be cleared.

When SSADR and SSCON have been initialised, the TWI module waits until it is addressed by its own slave address followed by the data direction bit which must be at logic 0 (W) for the TWI to operate in the slave receiver mode. After its own slave address and the W bit have been received, the serial interrupt flag is set and a valid status code can be read from SSCS. This status code is used to vector to an interrupt service routine.The appropriate action to be taken for each of these status code is detailed in Table . The slave receiver mode may also be entered if arbitration is lost while TWI is in the master mode (states 68h and 78h).

If the AA bit is reset during a transfer, TWI module will return a not acknowledge (logic 1) to SDA after the next received data byte. While AA is reset, the TWI module does not respond to its own slave address. However, the 2-wire bus is still monitored and address recognition may be resume at any time by setting AA. This means that the AA bit may be used to temporarily isolate the module from the 2-wire bus.

Table 20-5. Status in Master Transmitter Mode

Status Code SSSTA	Status of the Two-wire Bus and Two-wire Hardware	Application software response					Next Action Taken by Two-wire Hardware
			To SSCON				
		To/From SSDAT	SSSTA	SSSTO	SSI	SSAA	
08h	A START condition has been transmitted	Write SLA+W	X	0	0	X	SLA+W will be transmitted.
10h	A repeated START condition has been transmitted	Write SLA+W	X	0	0	X	SLA+W will be transmitted.
		Write SLA+R	X	0	0	X	SLA+R will be transmitted. Logic will switch to master receiver mode
18h	SLA+W has been transmitted; ACK has been received	Write data byte	0	0	0	X	Data byte will be transmitted.
		No SSDAT action	1	0	0	X	Repeated START will be transmitted.
		No SSDAT action	0	1	0	X	STOP condition will be transmitted and SSSTO flag will be reset.
		No SSDAT action	1	1	0	X	STOP condition followed by a START condition will be transmitted and SSSTO flag will be reset.
20h	SLA+W has been transmitted; NOT ACK has been received	Write data byte	0	0	0	X	Data byte will be transmitted.
		No SSDAT action	1	0	0	X	Repeated START will be transmitted.
		No SSDAT action	0	1	0	X	STOP condition will be transmitted and SSSTO flag will be reset.
		No SSDAT action	1	1	0	X	STOP condition followed by a START condition will be transmitted and SSSTO flag will be reset.
28h	Data byte has been transmitted; ACK has been received	Write data byte	0	0	0	X	Data byte will be transmitted.
		No SSDAT action	1	0	0	X	Repeated START will be transmitted.
		No SSDAT action	0	1	0	X	STOP condition will be transmitted and SSSTO flag will be reset.
		No SSDAT action	1	1	0	X	STOP condition followed by a START condition will be transmitted and SSSTO flag will be reset.
30h	Data byte has been transmitted; NOT ACK has been received	Write data byte	0	0	0	X	Data byte will be transmitted.
		No SSDAT action	1	0	0	X	Repeated START will be transmitted.
		No SSDAT action	0	1	0	X	STOP condition will be transmitted and SSSTO flag will be reset.
		No SSDAT action	1	1	0	X	STOP condition followed by a START condition will be transmitted and SSSTO flag will be reset.
38h	Arbitration lost in SLA+W or data bytes	No SSDAT action	0	0	0	X	Two-wire bus will be released and not addressed slave mode will be entered.
		No SSDAT action	1	0	0	X	A START condition will be transmitted when the bus becomes free.

Table 20-7. Status in Slave Receiver Mode

Status Code (SSCS)	Status of the 2-wire bus and 2-wire hardware	Application Software Response					Next Action Taken By 2-wire Software
		To/from SSDAT	To SSCON				
			STA	STO	SI	AA	
60h	Own SLA+W has been received; ACK has been returned	No SSDAT action or	X	0	0	0	Data byte will be received and NOT ACK will be returned
		No SSDAT action	X	0	0	1	Data byte will be received and ACK will be returned
68h	Arbitration lost in SLA+R/W as master; own SLA+W has been received; ACK has been returned	No SSDAT action or	X	0	0	0	Data byte will be received and NOT ACK will be returned
		No SSDAT action	X	0	0	1	Data byte will be received and ACK will be returned
70h	General call address has been received; ACK has been returned	No SSDAT action or	X	0	0	0	Data byte will be received and NOT ACK will be returned
		No SSDAT action	X	0	0	1	Data byte will be received and ACK will be returned
78h	Arbitration lost in SLA+R/W as master; general call address has been received; ACK has been returned	No SSDAT action or	X	0	0	0	Data byte will be received and NOT ACK will be returned
		No SSDAT action	X	0	0	1	Data byte will be received and ACK will be returned
80h	Previously addressed with own SLA+W; data has been received; ACK has been returned	No SSDAT action or	X	0	0	0	Data byte will be received and NOT ACK will be returned
		No SSDAT action	X	0	0	1	Data byte will be received and ACK will be returned
88h	Previously addressed with own SLA+W; data has been received; NOT ACK has been returned	Read data byte or	0	0	0	0	Switched to the not addressed slave mode; no recognition of own SLA or GCA
		Read data byte or	0	0	0	1	Switched to the not addressed slave mode; own SLA will be recognised; GCA will be recognised if GC=logic 1
		Read data byte or	1	0	0	0	Switched to the not addressed slave mode; no recognition of own SLA or GCA. A START condition will be transmitted when the bus becomes free
		Read data byte	1	0	0	1	Switched to the not addressed slave mode; own SLA will be recognised; GCA will be recognised if GC=logic 1. A START condition will be transmitted when the bus becomes free
90h	Previously addressed with general call; data has been received; ACK has been returned	Read data byte or	X	0	0	0	Data byte will be received and NOT ACK will be returned
		Read data byte	X	0	0	1	Data byte will be received and ACK will be returned

Figure 21-3. UFI Block Diagram

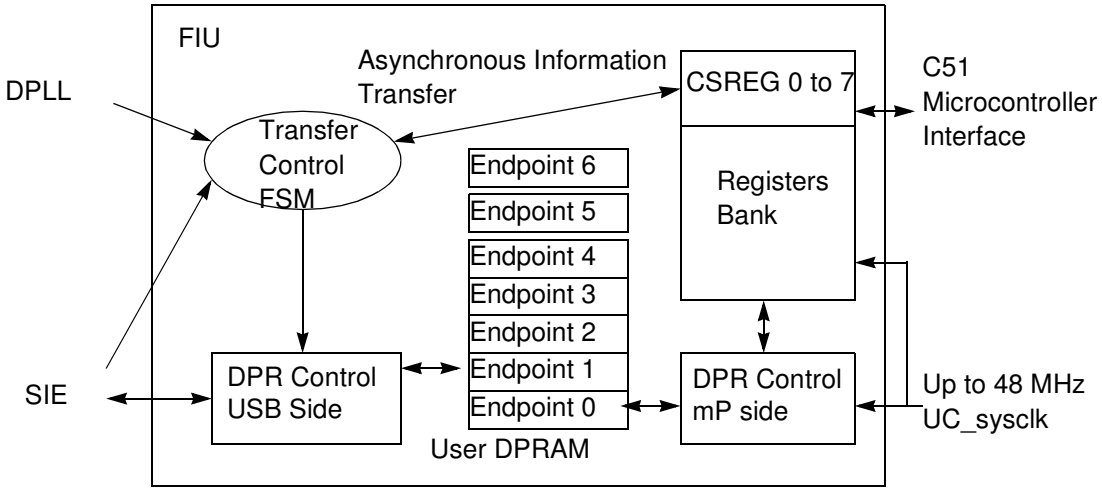
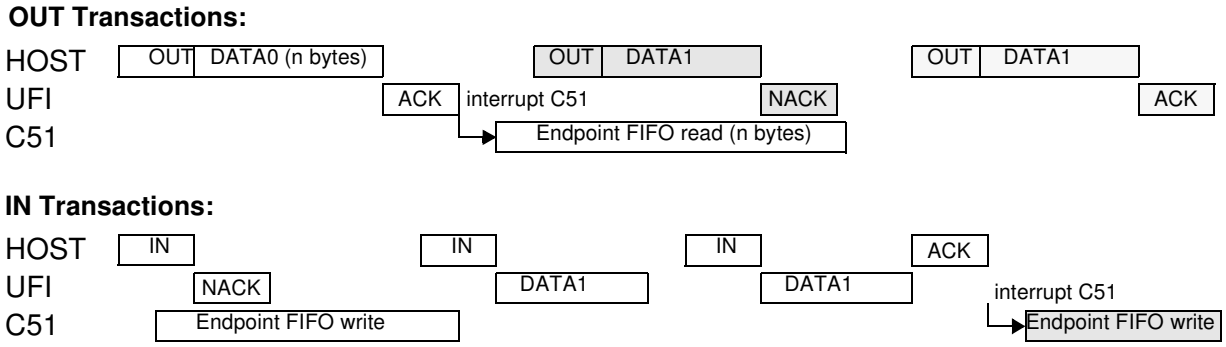


Figure 21-4. Minimum Intervention from the USB Device Firmware



21.2 Configuration

21.2.1 General Configuration

- USB controller enable

  Before any USB transaction, the 48 MHz required by the USB controller must be correctly generated (See “Clock Controller” on page 14.).

  The USB controller will be then enabled by setting the EUSB bit in the USBCON register.

- Set address

  After a Reset or a USB reset, the software has to set the FEN (Function Enable) bit in the USBADDR register. This action will allow the USB controller to answer to the requests sent at the address 0.

  When a SET_ADDRESS request has been received, the USB controller must only answer to the address defined by the request. The new address will be stored in the USBADDR register. The FEN bit and the FADDEN bit in the USBCON register will be set to allow the USB controller to answer only to requests sent at the new address.

The firmware has to clear one of these two bits after having read all the data FIFO to allow a new packet to be stored in the corresponding bank.

If the Host sends more bytes than supported by the endpoint FIFO, the overflow data won't be stored, but the USB controller will consider that the packet is valid if the CRC is correct.

21.6.3 Isochronous IN Transactions in Standard Mode

An endpoint will be first enabled and configured before being able to send Isochronous packets.

The firmware will fill the FIFO with the data to be sent and set the TXRDY bit in the UEPSTAX register to allow the USB controller to send the data stored in FIFO at the next IN request concerning this endpoint.
If the TXRDY bit is not set when the IN request occurs, nothing will be sent by the USB controller.

When the IN packet has been sent, the TXCMPL bit in the UEPSTAX register is set by the USB controller. This triggers a USB interrupt if enabled. The firmware will clear the TXCMPL bit before filling the endpoint FIFO with new data.

The firmware will never write more bytes than supported by the endpoint FIFO

21.6.4 Isochronous IN Transactions in Ping-pong Mode

An endpoint will be first enabled and configured before being able to send Isochronous packets.

The firmware will fill the FIFO bank 0 with the data to be sent and set the TXRDY bit in the UEPSTAX register to allow the USB controller to send the data stored in FIFO at the next IN request concerning the endpoint. The FIFO banks are automatically switched, and the firmware can immediately write into the endpoint FIFO bank 1.
If the TXRDY bit is not set when the IN request occurs, nothing will be sent by the USB controller.

When the IN packet concerning the bank 0 has been sent, the TXCMPL bit is set by the USB controller. This triggers a USB interrupt if enabled. The firmware will clear the TXCMPL bit before filling the endpoint FIFO bank 0 with new data. The FIFO banks are then automatically switched.

When the IN packet concerning the bank 1 has been sent, the TXCMPL bit is set by the USB controller. This triggers a USB interrupt if enabled. The firmware will clear the TXCMPL bit before filling the endpoint FIFO bank 1 with new data.

The bank switch is performed by the USB controller each time the TXRDY bit is set by the firmware. Until the TXRDY bit has been set by the firmware for an endpoint bank, the USB controller won't send anything at each IN requests concerning this bank.

The firmware will never write more bytes than supported by the endpoint FIFO.

21.7 Miscellaneous

21.7.1 USB Reset

The EORINT bit in the USBINT register is set by hardware when a End Of Reset has been detected on the USB bus. This triggers a USB interrupt if enabled. The USB controller is still enabled, but all the USB registers are reset by hardware. The firmware will clear the EORINT bit to allow the next USB reset detection.

Table 21-8. UEPCONX Register
UEPCONX (S:D4h)
USB Endpoint X Control Register

7	6	5	4	3	2	1	0
EPEN	**-**	**-**	**-**	**DTGL**	**EPDIR**	**EPTYPE1**	**EPTYPE0**

Bit Number	Bit Mnemonic	Description
7	EPEN	**Endpoint Enable** Set this bit to enable the endpoint according to the device configuration. Endpoint 0 will always be enabled after a hardware or USB bus reset and participate in the device configuration. Clear this bit to disable the endpoint according to the device configuration.
6	-	**Reserved** The value read from this bit is always 0. Do not set this bit.
5	-	**Reserved** The value read from this bit is always 0. Do not set this bit.
4	-	**Reserved** The value read from this bit is always 0. Do not set this bit.
3	DTGL	**Data Toggle (Read-only)** This bit is set by hardware when a valid DATA0 packet is received and accepted. This bit is cleared by hardware when a valid DATA1 packet is received and accepted.
2	EPDIR	**Endpoint Direction** Set this bit to configure IN direction for Bulk, Interrupt and Isochronous endpoints. Clear this bit to configure OUT direction for Bulk, Interrupt and Isochronous endpoints. This bit has no effect for Control endpoints.
1-0	EPTYPE[1:0]	**Endpoint Type** Set this field according to the endpoint configuration (Endpoint 0 will always be configured as control): 00Control endpoint 01Isochronous endpoint 10Bulk endpoint 11Interrupt endpoint

Note: 1. (X = EPNUM set in UEPNUM Register UEPNUM (S:C7h) USB Endpoint Number)

Reset Value = 80h when UEPNUM = 0 (default Control Endpoint)

Reset Value = 00h otherwise for all other endpoints

Table 21-10. UEPDATX Register
UEPDATX (S:CFh)
USB FIFO Data Endpoint X (X = EPNUM set in UEPNUM Register UEPNUM

7	6	5	4	3	2	1	0
FDAT7	FDAT6	FDAT5	FDAT4	FDAT3	FDAT2	FDAT1	FDAT0

Bit Number	Bit Mnemonic	Description
7 - 0	FDAT[7:0]	**Endpoint X FIFO data** Data byte to be written to FIFO or data byte to be read from the FIFO, for the Endpoint X (see EPNUM).

(S:C7h) USB Endpoint Number)
Reset Value = XXh

Table 21-11. UBYCTLX Register
UBYCTLX (S:E2h)
USB Byte Count Low Register X (X = EPNUM set in UEPNUM Register UEP-

7	6	5	4	3	2	1	0
BYCT7	BYCT6	BYCT5	BYCT4	BYCT3	BYCT2	BYCT1	BYCT0

Bit Number	Bit Mnemonic	Description
7 - 0	BYCT[7:0]	**Byte Count LSB** Least Significant Byte of the byte count of a received data packet. The most significant part is provided by the UBYCTHX Register UBYCTHX (S:E3h) USB Byte Count High Register X (X = EPNUM set in UEPNUM Register UEPNUM (S:C7h) USB Endpoint Number) (see Figure 21-11 on page 145). This byte count is equal to the number of data bytes received after the Data PID.

NUM (S:C7h) USB Endpoint Number)
Reset Value = 00h

Table 25-2. WDTPRG Register

WDTPRG - Watchdog Timer Out Register (0A7h)

7	6	5	4	3	2	1	0
-	-	-	-	-	S2	S1	S0

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is undetermined. Do not try to set this bit.
6	-	
5	-	
4	-	
3	-	
2	S2	WDT Time-out select bit 2
1	S1	WDT Time-out select bit 1
0	S0	WDT Time-out select bit 0
		S2 S1 S0 Selected Time-out 0 0 0 16384x2^(214 - 1) machine cycles, 16.3 ms at FOSC = 12 MHz 0 0 1 16384x2^(215 - 1) machine cycles, 32.7 ms at FOSC = 12 MHz 0 1 0 16384x2^(216 - 1) machine cycles, 65.5 ms at FOSC = 12 MHz 0 1 1 16384x2^(217 - 1) machine cycles, 131 ms at FOSC = 12 MHz 1 0 0 16384x2^(218 - 1) machine cycles, 262 ms at FOSC = 12 MHz 1 0 1 16384x2^(219 - 1) machine cycles, 542 ms at FOSC = 12 MHz 1 1 0 16384x2^(220 - 1) machine cycles, 1.05 s at FOSC = 12 MHz 1 1 1 16384x2^(221 - 1) machine cycles, 2.09 s at FOSC = 12 MHz 16384x2^S machine cycles

Reset value = XXXX X000

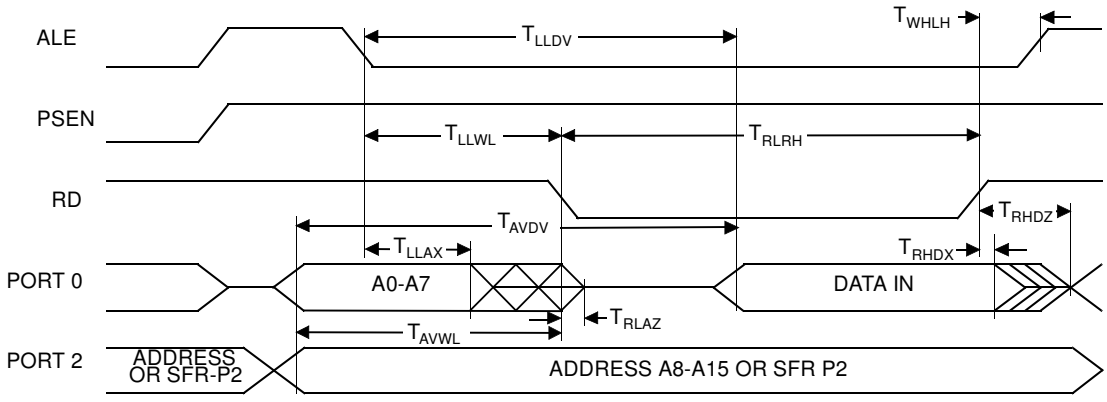
25.2 WDT During Power-down and Idle

In Power-down mode the oscillator stops, which means the WDT also stops. While in Power-down mode the user does not need to service the WDT. There are 2 methods of exiting Power-down mode: by a hardware reset or via a level activated external interrupt which is enabled prior to entering Power-down mode. When Power-down is exited with hardware reset, servicing the WDT should occur as it normally should whenever the AT89C5130A/31A-M is reset. Exiting Power-down with an interrupt is significantly different. The interrupt is held low long enough for the oscillator to stabilize. When the interrupt is brought high, the interrupt is serviced. To prevent the WDT from resetting the device while the interrupt pin is held low, the WDT is not started until the interrupt is pulled high. It is suggested that the WDT be reset during the interrupt service routine.

To ensure that the WDT does not overflow within a few states of exiting of power-down, it is better to reset the WDT just before entering power-down.

In the Idle mode, the oscillator continues to run. To prevent the WDT from resetting the AT89C5130A/31A-M while in Idle mode, the user should always set up a timer that will periodically exit Idle, service the WDT, and re-enter Idle mode.

27.4.6 External Data Memory Read Cycle



27.4.7 Serial Port Timing - Shift Register Mode

Table 27-8. Symbol Description (F = 40 MHz)

Symbol	Parameter
T_{XLXL}	Serial port clock cycle time
T_{QVHX}	Output data set-up to clock rising edge
T_{XHQX}	Output data hold after clock rising edge
T_{XHDX}	Input data hold after clock rising edge
T_{XHDV}	Clock rising edge to input data valid

Table 27-9. AC Parameters for a Fix Clock (F = 40 MHz)

Symbol	Min	Max	Units
T_{XLXL}	300		ns
T_{QVHX}	200		ns
T_{XHQX}	30		ns
T_{XHDX}	0		ns
T_{XHDV}		117	ns

Table 27-10. AC Parameters for a Variable Clock

Symbol	Type	Standard Clock	X2 Clock	X Parameter for -M Range	Units
T_{XLXL}	Min	12 T	6 T		ns
T_{QVHX}	Min	10 T - x	5 T - x	50	ns
T_{XHQX}	Min	2 T - x	T - x	20	ns
T_{XHDX}	Min	x	x	0	ns
T_{XHDV}	Max	10 T - x	5 T- x	133	ns