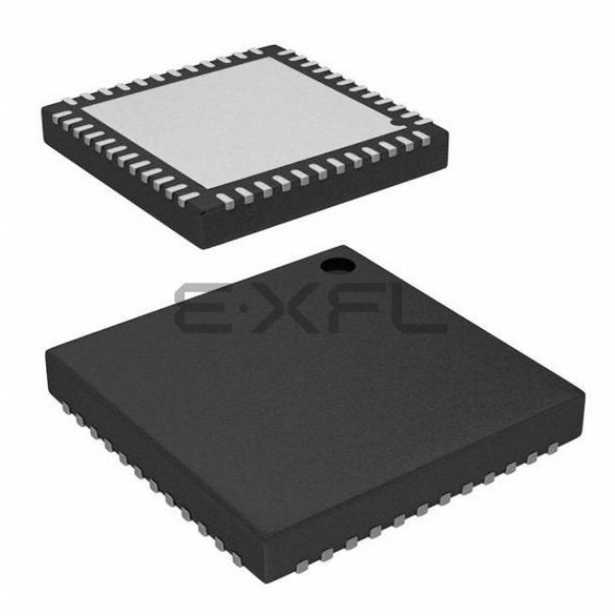

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	CSIO, I²C, LINbus, SmartCard, UART/USART
Peripherals	I²S, LVD, POR, PWM, WDT
Number of I/O	38
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-WFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e1c11c0agn20000

- 16-bit PWM timer
- 16-bit PPG timer
- 16/32-bit reload timer
- 16/32-bit PWC timer

General-Purpose I/O Port

This series can use its pin as a general-purpose I/O port when it is not used for an external bus or a peripheral function. All ports can be set to fast general-purpose I/O ports or slow general-purpose I/O ports. In addition, this series has a port relocate function that can set to which I/O port a peripheral function can be allocated.

- All ports are Fast GPIO which can be accessed by 1cycle
- Capable of controlling the pull-up of each pin
- Capable of reading pin level directly
- Port relocate function
- Up to 54 fast general-purpose I/O ports @64-pin package
- Certain ports are 5 V tolerant.
  See 4.List of Pin Functions and 5.I/O Circuit Type for the corresponding pins.

Dual Timer (32-/16-bit Down Counter)

The Dual Timer consists of two programmable 32-/16-bit down counters. The operation mode of each timer channel can be selected from one of the following.

- Free-running mode
- Periodic mode (= Reload mode)
- One-shot mode

Real-Time Clock

The Real-time Clock counts year/month/day/hour/minute/second/day of the week from year 00 to year 99.

- The RTC can generate an interrupt at a specific time (year/month/day/hour/minute/second/day of the week) and can also generate an interrupt in a specific year, in a specific month, on a specific day, at a specific hour or at a specific minute.
- It has a timer interrupt function generating an interrupt upon a specific time or at specific intervals.
- It can keep counting while rewriting the time.
- It can count leap years automatically.

Watch Counter

The Watch Counter wakes up the microcontroller from the low power consumption mode. The clock source can be selected from the main clock, the sub clock, the built-in high-speed CR clock or the built-in low-speed CR clock.

Interval timer: up to 64 s (sub clock: 32.768 kHz)

External Interrupt Controller Unit

- Up to 12 external interrupt input pins
- Non-maskable interrupt (NMI) input pin: 1

Watchdog Timer (2 Channels)

The watchdog timer generates an interrupt or a reset when the counter reaches a time-out value.

This series consists of two different watchdogs, hardware watchdog and software watchdog.

The hardware watchdog timer is clocked by the built-in low-speed CR oscillator. Therefore, the hardware watchdog is active in any low-power consumption modes except RTC, Stop, Deep standby RTC and Deep standby Stop mode.

CRC (Cyclic Redundancy Check) Accelerator

The CRC accelerator calculates the CRC which has a heavy software processing load, and achieves a reduction of the integrity check processing load for reception data and storage.

- CCITT CRC16 and IEEE-802.3 CRC32 are supported.
  - CCITT CRC16 Generator Polynomial: 0x1021
  - IEEE-802.3 CRC32 Generator Polynomial: 0x04C11DB7

HDMI-CEC/Remote Control Receiver (Up to 2 Channels)

- HDMI-CEC transmitter
  - Header block automatic transmission by judging Signal free
  - Generating status interrupt by detecting Arbitration lost
  - Generating START, EOM, ACK automatically to output CEC transmission by setting 1 byte data
  - Generating transmission status interrupt when transmitting 1 block (1 byte data and EOM/ACK)
- HDMI-CEC receiver
  - Automatic ACK reply function available
  - Line error detection function available
- Remote control receiver
  - 4 bytes reception buffer
  - Repeat code detection function available

Smart Card Interface (Max 1 Channel)

- Compliant with ISO7816-3 specification
- Card Reader only/B class card only
- Available protocols
  - Transmitter: 8E2, 8O2, 8N2
  - Receiver: 8E1, 8O1, 8N2, 8N1, 9N1
  - Inverse mode
- TX/RX FIFO integrated (RX: 16-bytes, TX:16-bytes)

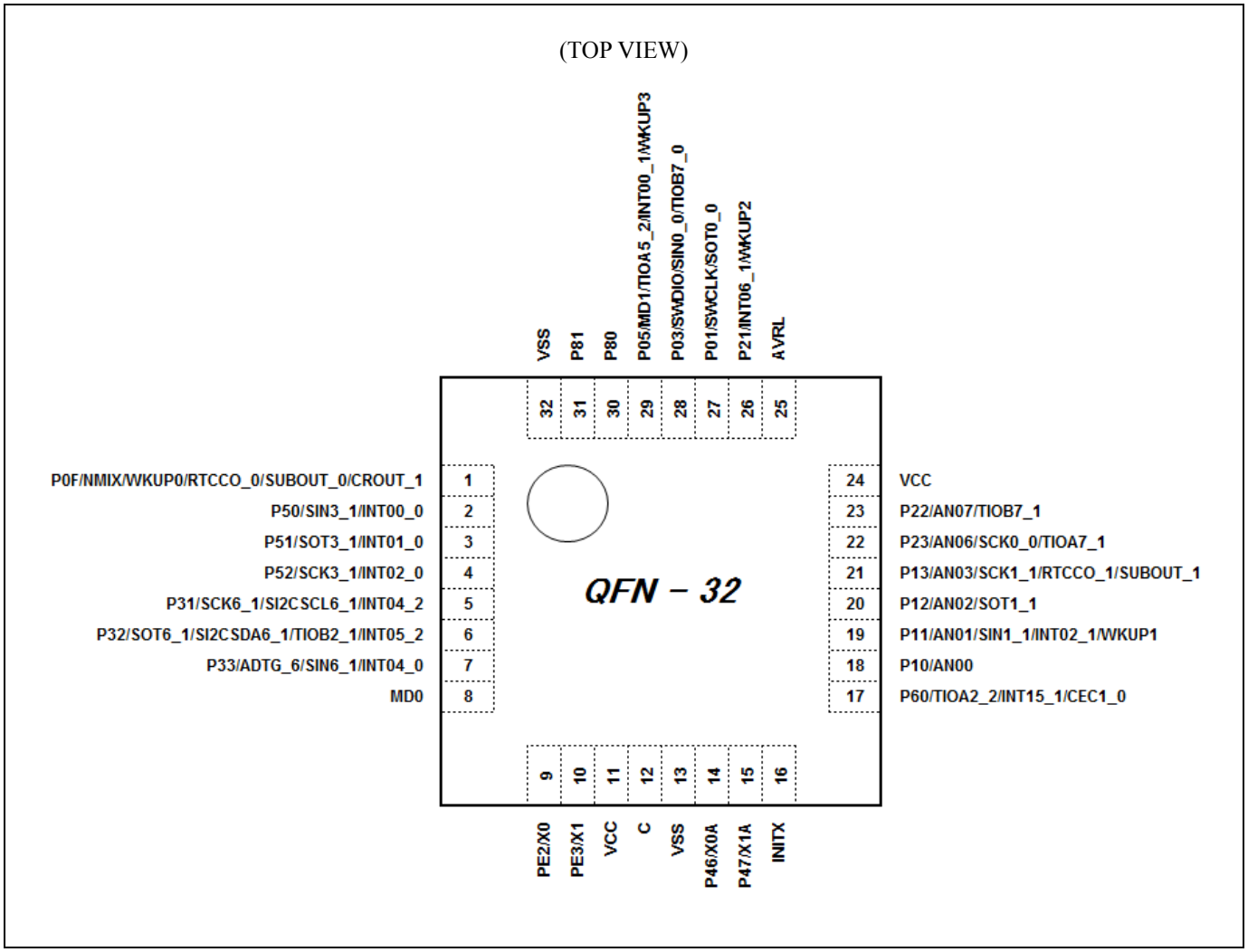
Clock and Reset

- Clocks

A clock can be selected from five clock sources (two external oscillators, two built-in CR oscillator, and main PLL).

  - Main clock: 8 MHz to 48 MHz

LCC-32P-M73



Note:

- *The number after the underscore ("_") in a pin name such as XXX_1 and XXX_2 indicates the relocated port number. The channel on such pin has multiple functions, each of which has its own pin name. Use the Extended Port Function Register (EPFR) to select the pin to be used.*

Pin no.			Pin Function	I/O circuit type	Pin state type
LQFP-64 QFN-64	LQFP-48 QFN-48	LQFP-32 QFN-32			
45	33	-	P15	F	J
			AN05		
			SOT0_1		
			SCS11_1		
46	34	22	P23	F	J
			AN06		
			SCK0_0		
			TIOA7_1		
47	35	23	P22	F	J
			AN07		
			TIOB7_1		
48	36	24	VCC	-	-
49	37	-	AVRH *	-	-
50	38	25	AVRL	-	-
51	39	26	P21	E	K
			INT06_1		
			WKUP2		
52	-	-	P00	E	K
			WKUP4		
53	40	27	P01	D	K
			SWCLK		
			SOT0_0		
54	-	-	P02	E	K
			WKUP5		
55	41	28	P03	D	K
			SWDIO		
			SIN0_0		
			TIOB7_0		
56	42	29	P05	E	K
			MD1		
			TIOA5_2		
			INT00_1		
			WKUP3		
57	43	-	VCC	-	-
58	44	30	P80	J	G
59	45	31	P81	J	G
60	46	32	VSS	-	-
61	47	-	P61	H	K
			TIOB2_2		
62	-	-	P0B	E	K
			TIOB6_1		
			WKUP6		
63	-	-	P0C	E	K
			TIOA6_1		
			WKUP7		

Pin function	Pin name	Function description	Pin no.		
			LQFP-64 QFN-64	LQFP-48 QFN-48	LQFP-32 QFN-32
External Interrupt	INT00_0	External interrupt request 00 input pin	1	1	2
	INT00_1		56	42	29
	INT01_0	External interrupt request 01 input pin	2	2	3
	INT02_0	External interrupt request 02 input pin	3	3	4
	INT02_1		41	29	19
	INT03_0	External interrupt request 03 input pin	11	10	-
	INT03_1		44	32	-
	INT03_2		5	5	-
	INT04_0	External interrupt request 04 input pin	8	8	7
	INT04_2		6	6	5
	INT05_1	External interrupt request 05 input pin	38	27	-
	INT05_2		7	7	6
	INT06_1	External interrupt request 06 input pin	51	39	26
	INT06_2		26	18	-
	INT07_2	External interrupt request 07 input pin	4	4	-
	INT08_1	External interrupt request 08 input pin	10	-	-
	INT12_1	External interrupt request 12 input pin	20	-	-
	INT13_1	External interrupt request 13 input pin	21	-	-
	INT15_1	External interrupt request 15 input pin	33	25	17
	NMIX	Non-Maskable Interrupt input pin	64	48	1
GPIO	P00	General-purpose I/O port 0	52	-	-
	P01		53	40	27
	P02		54	-	-
	P03		55	41	28
	P05		56	42	29
	P0B		62	-	-
	P0C		63	-	-
	P0F		64	48	1
GPIO	P10	General-purpose I/O port 1	40	28	18
	P11		41	29	19
	P12		42	30	20
	P13		43	31	21
	P14		44	32	-
	P15		45	33	-
	P1A		38	27	-
	P1B		37	26	-
	P1C		36	-	-
	P1D		35	-	-
	P1E		34	-	-
	P1F		39	-	-
GPIO	P21	General-purpose I/O port 2	51	39	26
	P22		47	35	23
	P23		46	34	22

Pin function	Pin name	Function description	Pin no.		
			LQFP-64 QFN-64	LQFP-48 QFN-48	LQFP-32 QFN-32
GPIO	P30	General-purpose I/O port 3	5	5	-
	P31		6	6	5
	P32		7	7	6
	P33		8	8	7
	P34		9	9	-
	P35		10	-	-
	P3A		11	10	-
	P3B		12	11	-
	P3C		13	12	-
	P3D		14	-	-
	P3E		15	-	-
	P3F		16	-	-
GPIO	P40	General-purpose I/O port 4	20	-	-
	P41		21	-	-
	P42		22	-	-
	P43		23	-	-
	P46		30	22	14
	P47		31	23	15
	P4C		24	16	-
	P4D		25	17	-
	P4E		26	18	-
GPIO	P50	General-purpose I/O port 5	1	1	2
	P51		2	2	3
	P52		3	3	4
	P53		4	4	-
GPIO	P60	General-purpose I/O port 6	33	25	17
	P61		61	47	-
GPIO	P80	General-purpose I/O port 8	58	44	30
	P81		59	45	31
GPIO	PE2	General-purpose I/O port E	18	14	9
	PE3		19	15	10
Multi-function Serial 0	SIN0_0	Multi-function serial interface ch.0 input pin	55	41	28
	SIN0_1		44	32	-
	SOT0_0 (SDA0_0)	Multi-function serial interface ch.0 output pin. This pin operates as SOT0 when used as a UART/CSIO/LIN pin (operation mode 0 to 3) and as SDA0 when used as an I2C pin (operation mode 4).	53	40	27
	SOT0_1 (SDA0_1)		45	33	-
	SCK0_0 (SCL0_0)	Multi-function serial interface ch.0 clock I/O pin. This pin operates as SCK0 when used as a CSIO pin (operation mode 2) and as SCL0 when used as an I2C pin (operation mode 4).	46	34	22

Pin function	Pin name	Function description	Pin no.		
			LQFP-64 QFN-64	LQFP-48 QFN-48	LQFP-32 QFN-32
Low Power Consumption Mode	WKUP0	Deep Standby mode return signal input pin 0	64	48	1
	WKUP1	Deep Standby mode return signal input pin 1	41	29	19
	WKUP2	Deep Standby mode return signal input pin 2	51	39	26
	WKUP3	Deep Standby mode return signal input pin 3	56	42	29
	WKUP4	Deep Standby mode return signal input pin 4	52	-	-
	WKUP5	Deep Standby mode return signal input pin 5	54	-	-
	WKUP6	Deep Standby mode return signal input pin 6	62	-	-
	WKUP7	Deep Standby mode return signal input pin 7	63	-	-
I2C Slave	SI2CSCL6_1	I2C Clock Pin	6	6	5
	SI2CSDA6_1	I2C Data Pin	7	7	6
RESET	INITX	External Reset Input pin. A reset is valid when INITX="L".	32	24	16
MODE	MD0	Mode 0 pin. During normal operation, input MD0="L". During serial programming to Flash memory, input MD0="H".	17	13	8
	MD1	Mode 1 pin. During normal operation, input is not needed. During serial programming to Flash memory, MD1 = "L" must be input.	56	42	29
CLOCK	X0	Main clock (oscillation) input pin	18	14	9
	X0A	Sub clock (oscillation) input pin	30	22	14
	X1	Main clock (oscillation) I/O pin	19	15	10
	X1A	Sub clock (oscillation) I/O pin	31	23	15
	CROUT_1	Built-in high-speed CR oscillation clock output port	64	48	1
POWER	VCC	Power supply pin	27	19	11
	VCC		48	36	24
	VCC		57	43	-
GND	VSS	GND pin	29	21	13
	VSS		60	46	32
Analog Reference	AVRH *	A/D converter analog reference voltage input pin	49	37	-
	AVRL	A/D converter analog reference voltage input pin	50	38	25
C pin	C	Power supply stabilization capacitance pin	28	20	12

*: In case of 32-pin package, AVRH pin is internally connected to VCC pin.

6.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

(1) Humidity

Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

(2) Discharge of Static Electricity

When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

(3) Corrosive Gases, Dust, or Oil

Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

(4) Radiation, Including Cosmic Radiation

Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

(5) Smoke, Flame

CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Spansion products in other special environmental conditions should consult with sales representatives.

Please check the latest handling precautions at the following URL.
http://www.spansion.com/fjdocuments/fj/datasheet/e-ds/DS00-00004.pdf

Notes on Power-on

Turn power on/off in the following order or at the same time.

Turning on : VCC →AVRH
Turning off : AVRH →VCC

Serial Communication

There is a possibility to receive wrong data due to the noise or other causes on the serial communication.
Therefore, design a printed circuit board so as to avoid noise.
Consider the case of receiving wrong data due to noise; perform error detection such as by applying a checksum of data at the end.
If an error is detected, retransmit the data.

Differences in Features Among the Products with Different Memory Sizes and Between Flash Memory Products and MASK Products

The electric characteristics including power consumption, ESD, latch-up, noise characteristics, and oscillation characteristics among the products with different memory sizes and between Flash memory products and MASK products are different because chip layout and memory structures are different.

If you are switching to use a different product of the same series, please make sure to evaluate the electric characteristics.

Pull-Up Function of 5 V Tolerant I/O

Please do not input the signal more than VCC voltage at the time of Pull-Up function use of 5 V tolerant I/O.

Handling when Using Debug Pins

When debug pins (SWDIO/SWCLK) are set to GPIO or other peripheral functions, set them as output only; do not set them as input.

Peripheral Address Map

Start address	End address	Bus	Peripheral
0x4000_0000	0x4000_0FFF	AHB	Flash memory I/F register
0x4000_1000	0x4000_FFFF		Reserved
0x4001_0000	0x4001_0FFF	APB0	Clock/Reset Control
0x4001_1000	0x4001_1FFF		Hardware Watchdog Timer
0x4001_2000	0x4001_2FFF		Software Watchdog Timer
0x4001_3000	0x4001_4FFF		Reserved
0x4001_5000	0x4001_5FFF		Dual-Timer
0x4001_6000	0x4001_FFFF		Reserved
0x4002_0000	0x4002_0FFF	APB1	Reserved
0x4002_1000	0x4002_3FFF		Reserved
0x4002_4000	0x4002_4FFF		Reserved
0x4002_5000	0x4002_5FFF		Base Timer
0x4002_6000	0x4002_6FFF		Reserved
0x4002_7000	0x4002_7FFF		A/D Converter
0x4002_8000	0x4002_DFFF		Reserved
0x4002_E000	0x4002_EFFF		Built-in CR trimming
0x4002_F000	0x4002_FFFF		Reserved
0x4003_0000	0x4003_0FFF		External Interrupt Controller
0x4003_1000	0x4003_1FFF		Interrupt Request Batch-Read Function
0x4003_2000	0x4003_2FFF		Reserved
0x4003_3000	0x4003_3FFF		GPIO
0x4003_4000	0x4003_4FFF		HDMI-CEC/Remote Control Receiver
0x4003_5000	0x4003_5FFF		Low-Voltage Detection / DS mode / Vref Calibration
0x4003_6000	0x4003_6FFF		Reserved
0x4003_7000	0x4003_77FF		Reserved
0x4003_7800	0x4003_79FF		I2C Slave
0x4003_7A00	0x4003_7FFF		Reserved
0x4003_8000	0x4003_8FFF		Multi-function Serial Interface
0x4003_9000	0x4003_9FFF		CRC
0x4003_A000	0x4003_AFFF		Watch Counter
0x4003_B000	0x4003_BFFF		Real-time clock
0x4003_C000	0x4003_C0FF		Low-speed CR Prescaler
0x4003_C100	0x4003_C7FF		Peripheral Clock Gating
0x4003_C800	0x4003_C8FF		Reserved
0x4003_C900	0x4003_C9FF		Smart Card Interface
0x4003_CA00	0x4003_CAFF		MFS-I2S Clock Generator
0x4003_CB00	0x4003_FFFF		Reserved
0x4004_0000	0x4004_FFFF	AHB	Reserved
0x4005_0000	0x4006_0FFF		Reserved
0x4006_1000	0x4006_1FFF		DSTC
0x4006_2000	0x41FF_FFFF		Reserved

10. Pin Status in Each CPU State

The following table shows pin status in each CPU state.

Type	Selected Pin function		CPU state							
			(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)
A	Main osillation circuit selected *1	Main osillation circuit selected	OS	OS	OE	OE	OE	OS	OS	OS
	Digital I/O slected *2	Main clock external input selected	-	-	IE/IS	IE/IS	IE/IS	IS	IS	IS
		GPIO selected	-	-	PC	HC	IS	HS	IS	HS
B	Main osillation circuit selected *1	Main osillation circuit selected	OS	OS	OE	OE	OE	OS	OS	OS
	Digital I/O slected *2	GPIO selected	-	-	PC	HC	IS	GS	IS	GS
C	Sub osillation circuit selected *1	Sub osillation circuit selected	OS	OE	OE	OE	OE	OE	OE	OE
	Digital I/O slected *2	Sub clock external input selected	-	-	IE/IS	IE/IS	IE/IS	IS	IS	IS
		GPIO selected	-	-	PC	HC	IS	HS	IS	HS
D	Sub osillation circuit selected *1	Sub osillation circuit selected	OS	OE	OE	OE	OE	OE	OE	OE
	Digital I/O slected *2	GPIO selected	-	-	PC	HC	IS	HS	IS	HS
E	Digital I/O slected	INITX input	This pin is digital input pin, pull up register is on, and digital input is not shut off in all CPU state..							
F	Digital I/O slected	MD0 input	This pin is digital input pin, pull up register is none, digital input is not shut off in all CPU state..							
G	Digital I/O slected *6	GPIO selected	IS	IE	CP	HC	IS	HS	IS	HS
H	Digital I/O slected	SW selected	IS	IP *5	PC	IP	IP	IP	IP	IP
		GPIO selected	-	-	PC	HC	IS	HS	IS	HS
I	Digital I/O slected	NMI selected	-	-	IP	IP	IP	-	-	-
		WKUP0 enable and input selected	-	-	IP	IP	IP	IP	IP	IP
		GPIO selected	IS	IE	PC	HC	IS	-	-	-
J	Analog input selected *3	Analog input selected	Analog input is enalbe in all CPU state							
	Digital I/O slected *4	WKUP enable and input selected	-	-	IP	IP	IP	IP	IP	IP
		Exterrnal interrupt enable and input selected	-	-	IP	IP	IP	GS	IS	GS
		GPIO selected	-	-	PC	HC	IS	HS	IS	HS
		Resource other than above selected	-	-	PC	HC	IS	GS	IS	GS
K	Digital I/O slected	CEC pin selected	-	-	CP	CP	CP	CP	CP	CP
		WKUP enable and input selected	-	-	IP	IP	IP	IP	IP	IP
		I2CSLAVE enable selected	-	-	PC	HC	IP	GS	IS	GS
		Exterrnal interrupt enable and input selected	-	-	PC	HC	IP	GS	IS	GS
		GPIO selected	IS	IE	PC	HC	IS	HS	IS	HS
		Resource other than above selected	-	-	PC	HC	IS	GS	IS	GS

Each term in above table have the following meanings.

Additional note

Additional note is described below.

*1 In this type, when internal oscillation function is selected, digital output is disabled. (Hi-Z) pull up register is off, digital input is shut off by fixed 0.

*2 In this type, when Digital I/O function is selected, internal oscillation function is disabled.

*3 In this type, when analog input function is selected, digital output is disabled, (Hi-Z). pull up register is off, digital input is shut off by fixed 0.

*4 In this type, when Digital I/O function is selected, analog input function is not available.

*5 In this case, PCR register is initialized to “1”. Pull up register is on.

*6 This pin does not have pull up register.

11.3.2 Pin Characteristics

(V_{CC} = 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

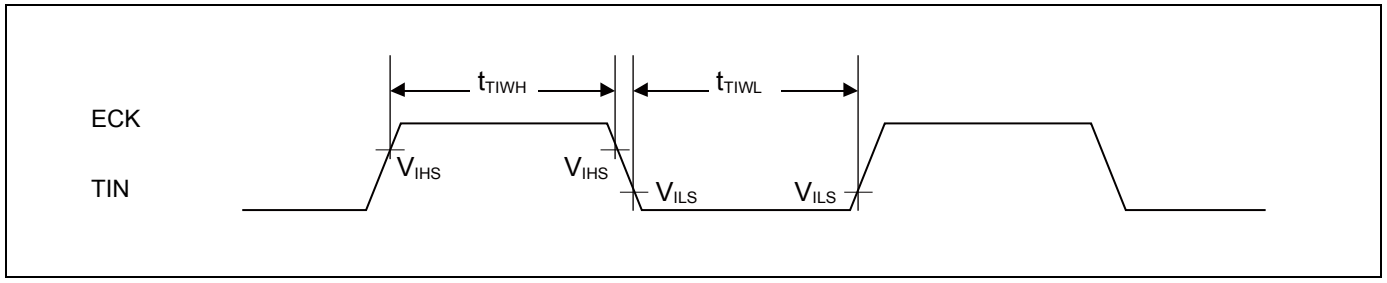
Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
H level input voltage (hysteresis input)	V_{IHS}	CMOS hysteresis input pin, MD0	$V_{CC} \geq 2.7$ V	$V_{CC} \times 0.8$	-	V_{CC} +0.3	V	
			$V_{CC} < 2.7$ V	$V_{CC} \times 0.7$				
		5 V tolerant input pin	$V_{CC} \geq 2.7$ V	$V_{CC} \times 0.8$	-	V_{SS} +5.5	V	
			$V_{CC} < 2.7$ V	$V_{CC} \times 0.7$				
L level input voltage (hysteresis input)	V_{ILS}	CMOS hysteresis input pin, MD0	$V_{CC} \geq 2.7$ V	V_{SS} - 0.3	-	$V_{CC} \times 0.2$	V	
			$V_{CC} < 2.7$ V			$V_{CC} \times 0.3$		
		5 V tolerant input pin	$V_{CC} \geq 2.7$ V	V_{SS} - 0.3	-	$V_{CC} \times 0.2$	V	
			$V_{CC} < 2.7$ V		-	$V_{CC} \times 0.3$		
H level output voltage	V_{OH}	4 mA type	$V_{CC} \geq 2.7$ V, I_{OH} = - 4 mA	V_{CC} - 0.5	-	V_{CC}	V	
			$V_{CC} < 2.7$ V, I_{OH} = - 2 mA	V_{CC} - 0.45				
L level output voltage	V_{OL}	4 mA type	$V_{CC} \geq 2.7$ V, I_{OL} 4 mA	V_{SS}	-	0.4	V	
			$V_{CC} < 2.7$ V, I_{OL}=2 mA					
Input leak current	I_{IL}	-	-	- 5	-	+ 5	µA	
Pull-up resistance value	R_{PU}	Pull-up pin	$V_{CC} \geq 2.7$ V	21	33	48	kΩ	
			$V_{CC} < 2.7$ V	-	-	88		
Input capacitance	C_{IN}	Other than VCC, VSS, AVRH	-	-	5	15	pF	

11.4.8 Base Timer Input Timing

Timer Input Timing

(V_{CC}= 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

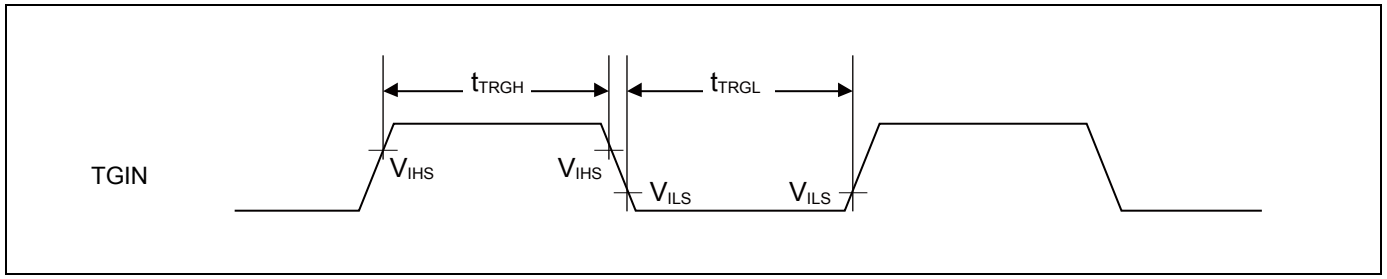
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH}, t_{TIWL}	TIOAn/TIOBn (when using as ECK, TIN)	-	2 t_{CYCP}	-	ns	



Trigger Input Timing

(V_{CC}= 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH}, t_{TRGL}	TIOAn/TIOBn (when using as TGIN)	-	2 t_{CYCP}	-	ns	



Note:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  For the number of the APB bus to which the Base Timer has been connected, see "8. Block Diagram".

CSIO (SPI=0, SCINV=1)

(V_{CC}= 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin name	Conditions	V_{CC} < 2.7V		V_{CC} ≥ 2.7V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	4 t_{CYCP}	-	4 t_{CYCP}	-	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↓ setup time	t_{IVSLI}	SCKx, SINx		50	-	36	-	ns
SCK ↓ → SIN hold time	t_{SLIXI}	SCKx, SINx		0	-	0	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	Slave mode	2 t_{CYCP} - 10	-	2 t_{CYCP} - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCKx, SOTx		-	50	-	33	ns
SIN → SCK ↓ setup time	t_{IVSLE}	SCKx, SINx		10	-	10	-	ns
SCK ↓ → SIN hold time	t_{SLIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	tF	SCKx		-	5	-	5	ns
SCK rising time	tR	SCKx		-	5	-	5	ns

Notes:

- *The above AC characteristics are for clock synchronous mode.*
- *t_{CYCP} represents the APB bus clock cycle time.*
  For the number of the APB bus to which Multi-function Serial has been connected, see "8. Block Diagram".
- *The characteristics are only applicable when the relocate port numbers are the same.*
  For instance, they are not applicable for the combination of SCKx_0 and SOTx_1.
- *External load capacitance C_L=30 pF*

SPI (SPI=1, SCINV=1)

(V_{CC}= 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin name	Conditions	V_{CC} < 2.7 V		V_{CC} ≥ 2.7 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	4 t_{CYCP}	-	4 t_{CYCP}	-	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↑ setup time	t_{IVSHI}	SCKx, SINx		50	-	36	-	ns
SCK ↑ → SIN hold time	t_{SHIXI}	SCKx, SINx		0	-	0	-	ns
SOT → SCK ↑ delay time	t_{SOVHI}	SCKx, SOTx		2 t_{CYCP} - 30	-	2 t_{CYCP} - 30	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	Slave mode	2 t_{CYCP} - 10	-	2 t_{CYCP} - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKx, SOTx		-	50	-	33	ns
SIN → SCK ↑ setup time	t_{IVSHE}	SCKx, SINx		10	-	10	-	ns
SCK ↑ → SIN hold time	t_{SHIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	tF	SCKx		-	5	-	5	ns
SCK rising time	tR	SCKx		-	5	-	5	ns

Notes:

- *The above AC characteristics are for clock synchronous mode.*
- *t_{CYCP} represents the APB bus clock cycle time.*
  For the number of the APB bus to which Multi-function Serial has been connected, see "8. Block Diagram".
- *The characteristics are only applicable when the relocate port numbers are the same.*
  For instance, they are not applicable for the combination of SCKx_0 and SOTx_1.
- *External load capacitance C_L=30 pF*

When Using CSIO/SPI Chip Select (SCINV=0, CSLVL=1)

(V_{CC}= 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Conditions	V_{CC} < 2.7 V		V_{CC} ≥ 2.7 V		Unit
			Min	Max	Min	Max	
SCS↓→SCK↓ setup time	t_{CSSI}	Master mode	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK↑→SCS↑ hold time	t_{CSHI}		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t_{CSDI}		(*3)-50	(*3)+50	(*3)-50	(*3)+50	ns
SCS↓→SCK↓ setup time	t_{CSSE}	Slave mode	$3t_{CYCP}$+30	-	$3t_{CYCP}$+30	-	ns
SCK↑→SCS↑ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		$3t_{CYCP}$+30	-	$3t_{CYCP}$+30	-	ns
SCS↓→SOT delay time	t_{DSE}		-	55	-	40	ns
SCS↑→SOT delay time	t_{DEE}		0	-	0	-	ns

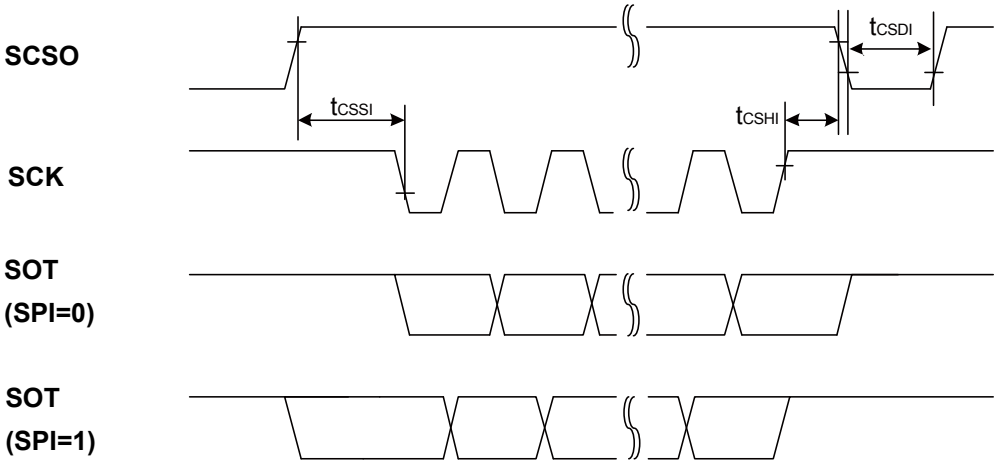
*1: CSSU bit value × serial chip select timing operating clock cycle.

*2: CSHD bit value × serial chip select timing operating clock cycle.

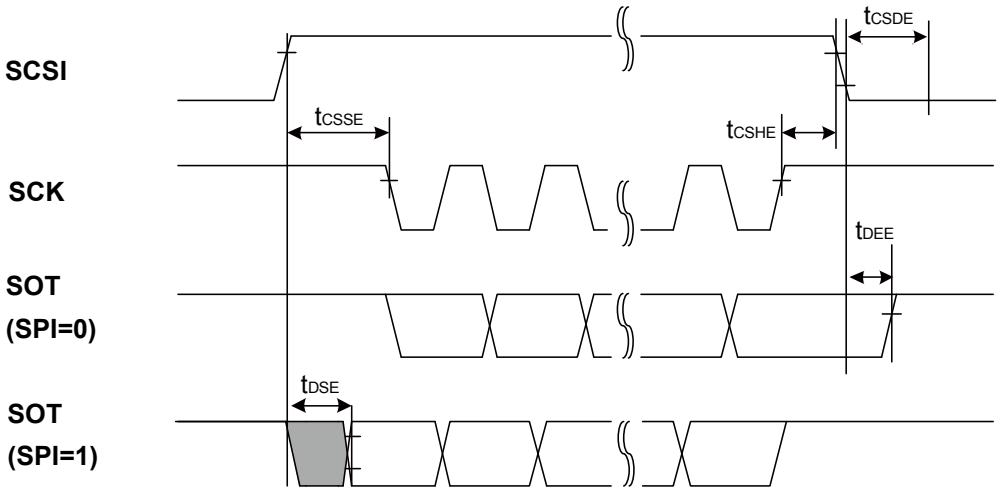
*3: CSDS bit value × serial chip select timing operating clock cycle.
Irrespective of CSDS bit setting, $5t_{CYCP}$ or more are required for the period the time when the serial chip select pin becomes inactive to the time when the serial chip select pin becomes active again.

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  For information about the APB bus number which Multi-function Serial is connected to, see "8. Block Diagram".
- *For information about CSSU, CSHD, CSDS, serial chip select timing operating clock, see "FM0+ Family Peripheral Manual".*
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCKx_0 and SCSIx_1 is not guaranteed.
- *When the external load capacitance C_L=30 pF.*

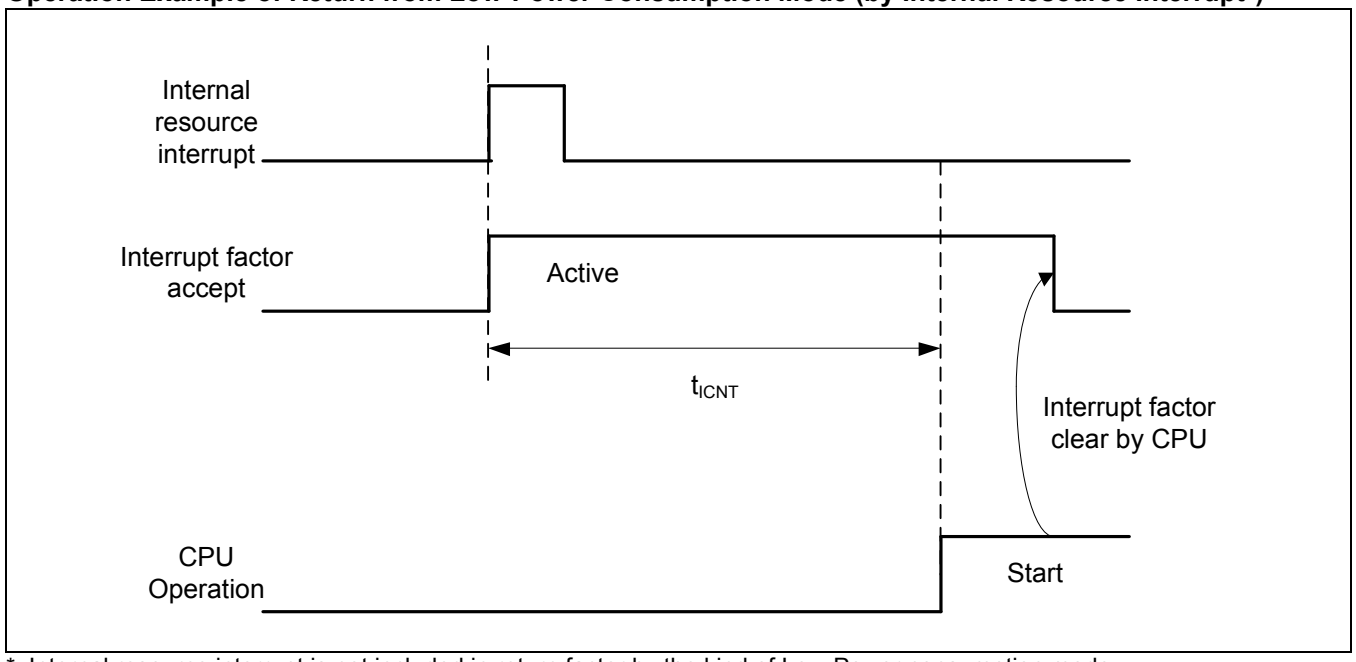


Master mode



Slave mode

Operation Example of Return from Low-Power Consumption Mode (by Internal Resource Interrupt*)

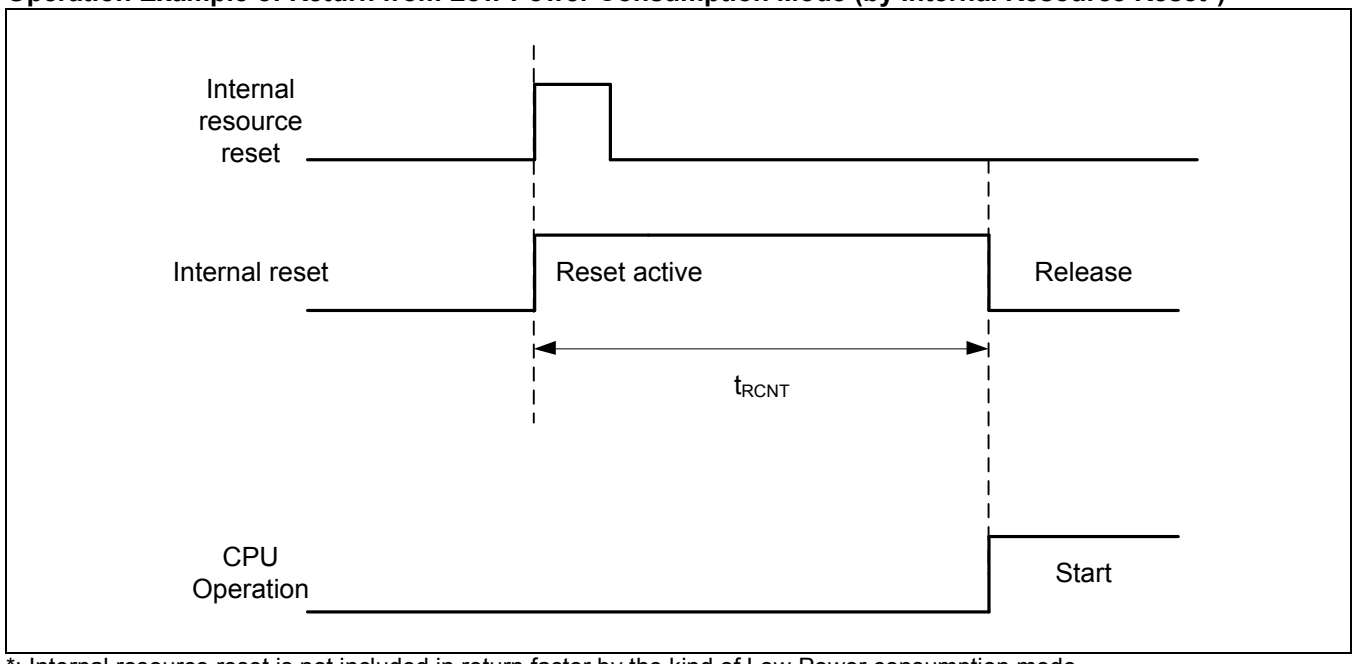


*: Internal resource interrupt is not included in return factor by the kind of Low-Power consumption mode.

Notes:

- *The return factor is different in each Low-Power consumption modes.*
  See "Chapter: Low Power Consumption Mode" and "Operations of Standby Modes" in FM0+ Family Peripheral Manual.
- *When interrupt recoveries, the operation mode that CPU recoveries depends on the state before the Low-Power consumption mode transition. See "Chapter: Low Power Consumption Mode" in "FM0+ Family Peripheral Manual".*

Operation Example of Return from Low Power Consumption Mode (by Internal Resource Reset*)

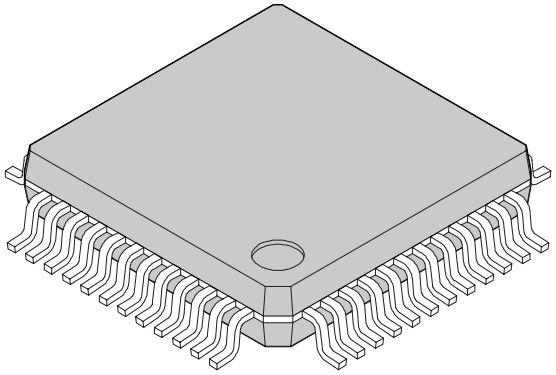


*: Internal resource reset is not included in return factor by the kind of Low-Power consumption mode.

Notes:

- *The return factor is different in each Low-Power consumption modes.*
  See "Chapter: Low Power Consumption Mode" and "Operations of Standby Modes" in FM0+ Family Peripheral Manual.
- *When interrupt recoveries, the operation mode that CPU recoveries depends on the state before the Low-Power consumption mode transition. See "Chapter: Low Power Consumption Mode" in "FM0+ Family Peripheral Manual".*
- *The time during the power-on reset/low-voltage detection reset is excluded. See "11.4.7 Power-on Reset Timing in 11.4 AC Characteristics in 11. Electrical Characteristics" for the detail on the time during the power-on reset/low -voltage detection reset.*
- *When in recovery from reset, CPU changes to the high-speed CR run mode. When using the main clock or the PLL clock, it is necessary to add the main clock oscillation stabilization wait time or the main PLL clock stabilization wait time.*
- *The internal resource reset means the watchdog reset and the CSV reset.*

48-pin plastic LQFP

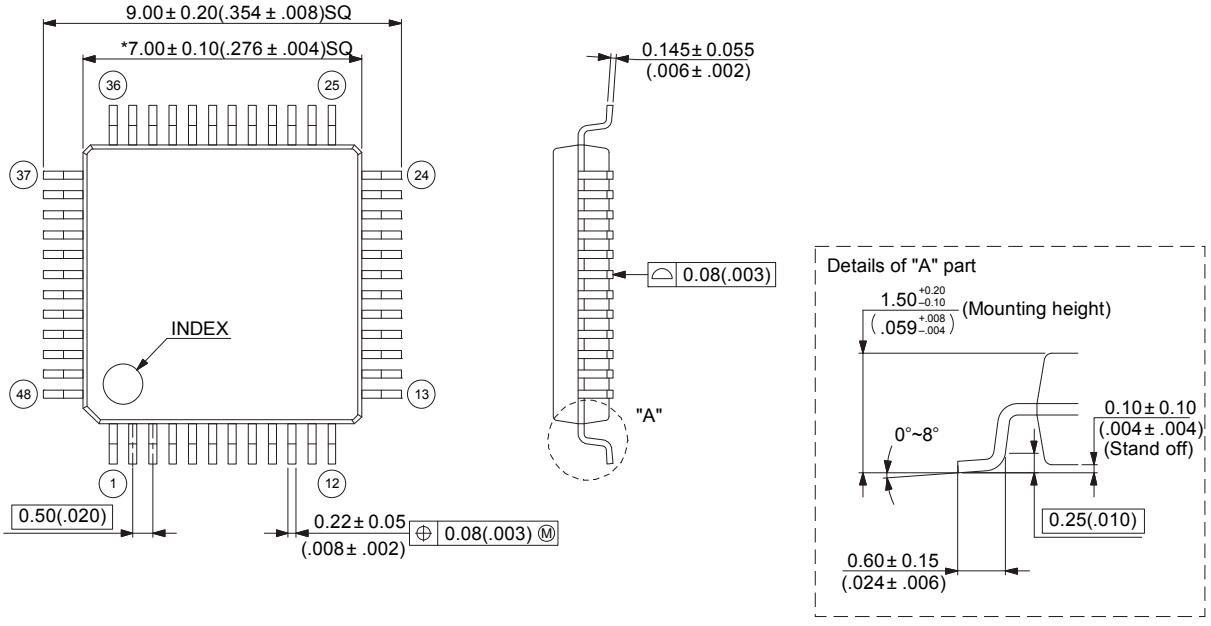


(FPT-48P-M49)

Lead pitch	0.50 mm
Package width × package length	7.00 mm × 7.00 mm
Lead shape	Gullwing
Lead bend direction	Normal bend
Sealing method	Plastic mold
Mounting height	1.70 mm MAX
Weight	0.17 g

48-pin plastic LQFP
(FPT-48P-M49)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.