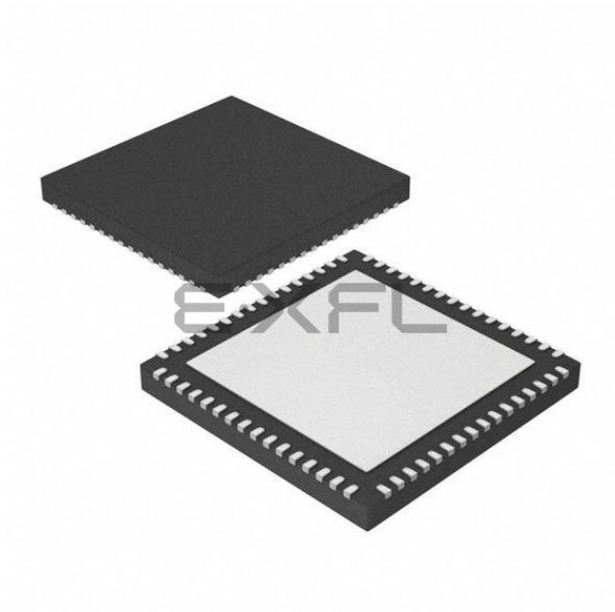
Infineon Technologies - S6E1C11D0AGN20000 Datasheet



Welcome to E-XFL.COM

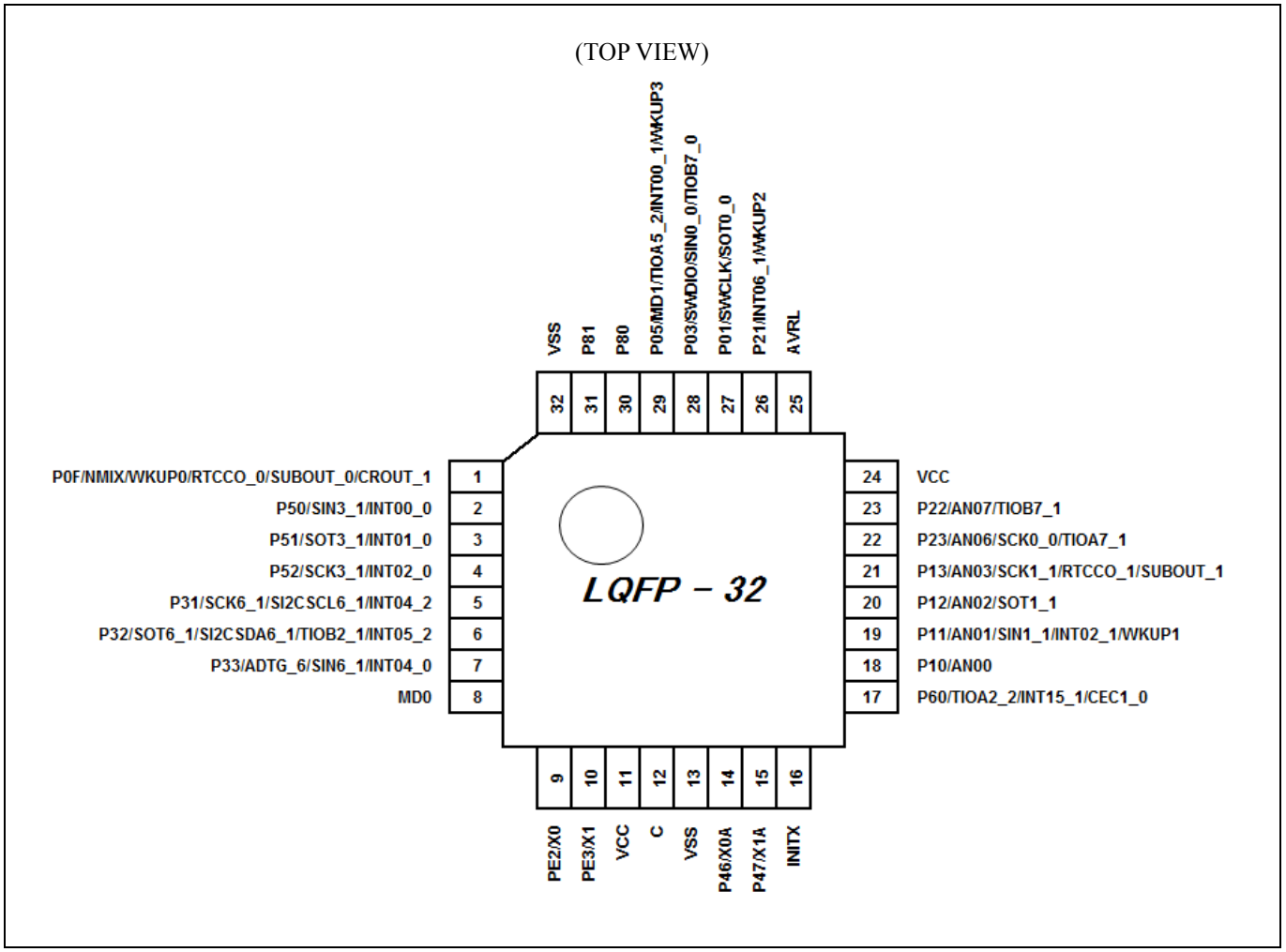
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	CSIO, I²C, LINbus, SmartCard, UART/USART
Peripherals	I²S, LVD, POR, PWM, WDT
Number of I/O	54
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-WFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e1c11d0agn20000

FPT-32P-M30



Note:

- *The number after the underscore ("_") in a pin name such as XXX_1 and XXX_2 indicates the relocated port number. The channel on such pin has multiple functions, each of which has its own pin name. Use the Extended Port Function Register (EPFR) to select the pin to be used.*

4. List of Pin Functions

List of Pin Numbers

The number after the underscore ("_") in a pin name such as XXX_1 and XXX_2 indicates the relocated port number. The channel on such pin has multiple functions, each of which has its own pin name. Use the Extended Port Function Register (EPFR) to select the pin to be used.

Pin no.			Pin Function	I/O circuit type	Pin state type
LQFP-64 QFN-64	LQFP-48 QFN-48	LQFP-32 QFN-32			
1	1	2	P50	D	K
			SIN3_1		
			INT00_0		
2	2	3	P51	D	K
			SOT3_1		
			INT01_0		
3	3	4	P52	D	K
			SCK3_1		
			INT02_0		
4	4	-	P53	D	K
			TIOA1_2		
			INT07_2		
5	5	-	P30	D	K
			SCS60_1		
			TIOB0_1		
			INT03_2		
			MI2SWS6_1		
6	6	-	P31	H	K
			SCK6_1		
			SI2CSCL6_1		
			INT04_2		
			MI2SCK6_1		
-	-	5	P31	H	K
			SCK6_1		
			SI2CSCL6_1		
			INT04_2		
7	7	-	P32	H	K
			SOT6_1		
			SI2CSDA6_1		
			TIOB2_1		
			INT05_2		
			MI2SDO6_1		
-	-	6	P32	H	K
			SOT6_1		
			SI2CSDA6_1		
			TIOB2_1		
			INT05_2		

Pin no.			Pin Function	I/O circuit type	Pin state type
LQFP-64 QFN-64	LQFP-48 QFN-48	LQFP-32 QFN-32			
8	8	-	P33 ADTG_6 SIN6_1 INT04_0 MI2SDI6_1	H	K
-	-	7	P33 ADTG_6 SIN6_1 INT04_0	H	K
9	-	-	P34 SCS61_1 TIOB4_1 MI2SMCK6_1	D	K
-	9	-	P34 SCS61_1 MI2SMCK6_1	D	K
10	-	-	P35 SCS62_1 TIOB5_1 INT08_1	D	K
11	-	-	P3A TIOA0_1 INT03_0 RTCCO_2 SUBOUT_2 IC1_CIN_0	D	K
-	10	-	P3A TIOA0_1 INT03_0 RTCCO_2 SUBOUT_2	D	K
12	-	-	P3B TIOA1_1 IC1_DATA_0	D	K
-	11	-	P3B TIOA1_1	D	K
13	-	-	P3C TIOA2_1 IC1_RST_0	D	K
-	12	-	P3C TIOA2_1	D	K
14	-	-	P3D TIOA3_1 IC1_VPEN_0	D	K

Pin no.			Pin Function	I/O circuit type	Pin state type
LQFP-64 QFN-64	LQFP-48 QFN-48	LQFP-32 QFN-32			
34	-	-	P1E	D	K
			RTS4_1		
			MI2SMCK4_1		
35	-	-	P1D	D	K
			CTS4_1		
			MI2SWS4_1		
36	-	-	P1C	D	K
			SCK4_1		
			MI2SCK4_1		
37	-	-	P1B	D	K
			SOT4_1		
			MI2SDO4_1		
-	26	-	P1B	D	K
			SOT4_1		
38	-	-	P1A	H	K
			SIN4_1		
			INT05_1		
			CEC0_0		
			MI2SDI4_1		
-	27	-	P1A	H	K
			SIN4_1		
			INT05_1		
			CEC0_0		
39	-	-	P1F	D	K
			ADTG_5		
40	28	18	P10	F	J
			AN00		
41	29	19	P11	G	J
			AN01		
			SIN1_1		
			INT02_1		
			WKUP1		
42	30	20	P12	F	J
			AN02		
			SOT1_1		
43	31	21	P13	F	J
			AN03		
			SCK1_1		
			RTCCO_1		
			SUBOUT_1		
44	32	-	P14	F	J
			AN04		
			SIN0_1		
			SCS10_1		
			INT03_1		

Pin no.			Pin Function	I/O circuit type	Pin state type
LQFP-64 QFN-64	LQFP-48 QFN-48	LQFP-32 QFN-32			
45	33	-	P15	F	J
			AN05		
			SOT0_1		
			SCS11_1		
46	34	22	P23	F	J
			AN06		
			SCK0_0		
			TIOA7_1		
47	35	23	P22	F	J
			AN07		
			TIOB7_1		
48	36	24	VCC	-	-
49	37	-	AVRH *	-	-
50	38	25	AVRL	-	-
51	39	26	P21	E	K
			INT06_1		
			WKUP2		
52	-	-	P00	E	K
			WKUP4		
53	40	27	P01	D	K
			SWCLK		
			SOT0_0		
54	-	-	P02	E	K
			WKUP5		
55	41	28	P03	D	K
			SWDIO		
			SIN0_0		
			TIOB7_0		
56	42	29	P05	E	K
			MD1		
			TIOA5_2		
			INT00_1		
			WKUP3		
57	43	-	VCC	-	-
58	44	30	P80	J	G
59	45	31	P81	J	G
60	46	32	VSS	-	-
61	47	-	P61	H	K
			TIOB2_2		
62	-	-	P0B	E	K
			TIOB6_1		
			WKUP6		
63	-	-	P0C	E	K
			TIOA6_1		
			WKUP7		

List of Pin Functions

The number after the underscore ("_") in a pin name such as XXX_1 and XXX_2 indicates the relocated port number. The channel on such pin has multiple functions, each of which has its own pin name. Use the Extended Port Function Register (EPFR) to select the pin to be used.

Pin function	Pin name	Function description	Pin no.		
			LQFP-64 QFN-64	LQFP-48 QFN-48	LQFP-32 QFN-32
ADC	ADTG_5	A/D converter external trigger input pin	39	-	-
	ADTG_6		8	8	7
	ADTG_7		23	-	-
ADC	AN00	A/D converter analog input pin. ANxx describes ADC ch.xx.	40	28	18
	AN01		41	29	19
	AN02		42	30	20
	AN03		43	31	21
	AN04		44	32	-
	AN05		45	33	-
	AN06		46	34	22
	AN07		47	35	23
Base Timer 0	TIOA0_0	Base timer ch.0 TIOA pin	20	-	-
	TIOA0_1		11	10	-
	TIOB0_1	Base timer ch.0 TIOB pin	5	5	-
Base Timer 1	TIOA1_0	Base timer ch.1 TIOA pin	21	-	-
	TIOA1_1		12	11	-
	TIOA1_2		4	4	-
Base Timer 2	TIOA2_0	Base timer ch.2 TIOA pin	22	-	-
	TIOA2_1		13	12	-
	TIOA2_2		33	25	17
	TIOB2_1	Base timer ch.2 TIOB pin	7	7	6
	TIOB2_2		61	47	-
Base Timer 3	TIOA3_0	Base timer ch.3 TIOA pin	23	-	-
	TIOA3_1		14	-	-
	TIOB3_0	Base timer ch.3 TIOB pin	24	-	-
Base Timer 4	TIOA4_1	Base timer ch.4 TIOA pin	15	-	-
	TIOB4_1	Base timer ch.4 TIOB pin	9	-	-
Base Timer 5	TIOA5_1	Base timer ch.5 TIOA pin	16	-	-
	TIOA5_2		56	42	29
	TIOB5_1	Base timer ch.5 TIOB pin	10	-	-
Base Timer 6	TIOA6_1	Base timer ch.6 TIOA pin	63	-	-
	TIOB6_1	Base timer ch.6 TIOB pin	62	-	-
Base Timer 7	TIOA7_1	Base timer ch.7 TIOA pin	46	34	22
	TIOB7_0	Base timer ch.7 TIOB pin	55	41	28
	TIOB7_1		47	35	23
Debugger	SWCLK	Serial wire debug interface clock input pin	53	40	27
	SWDIO	Serial wire debug interface data input / output pin	55	41	28

Pin function	Pin name	Function description	Pin no.		
			LQFP-64 QFN-64	LQFP-48 QFN-48	LQFP-32 QFN-32
External Interrupt	INT00_0	External interrupt request 00 input pin	1	1	2
	INT00_1		56	42	29
	INT01_0	External interrupt request 01 input pin	2	2	3
	INT02_0	External interrupt request 02 input pin	3	3	4
	INT02_1		41	29	19
	INT03_0	External interrupt request 03 input pin	11	10	-
	INT03_1		44	32	-
	INT03_2		5	5	-
	INT04_0	External interrupt request 04 input pin	8	8	7
	INT04_2		6	6	5
	INT05_1	External interrupt request 05 input pin	38	27	-
	INT05_2		7	7	6
	INT06_1	External interrupt request 06 input pin	51	39	26
	INT06_2		26	18	-
	INT07_2	External interrupt request 07 input pin	4	4	-
	INT08_1	External interrupt request 08 input pin	10	-	-
	INT12_1	External interrupt request 12 input pin	20	-	-
	INT13_1	External interrupt request 13 input pin	21	-	-
	INT15_1	External interrupt request 15 input pin	33	25	17
	NMIX	Non-Maskable Interrupt input pin	64	48	1
GPIO	P00	General-purpose I/O port 0	52	-	-
	P01		53	40	27
	P02		54	-	-
	P03		55	41	28
	P05		56	42	29
	P0B		62	-	-
	P0C		63	-	-
	P0F		64	48	1
GPIO	P10	General-purpose I/O port 1	40	28	18
	P11		41	29	19
	P12		42	30	20
	P13		43	31	21
	P14		44	32	-
	P15		45	33	-
	P1A		38	27	-
	P1B		37	26	-
	P1C		36	-	-
	P1D		35	-	-
	P1E		34	-	-
	P1F		39	-	-
GPIO	P21	General-purpose I/O port 2	51	39	26
	P22		47	35	23
	P23		46	34	22

6. Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Spansion semiconductor devices.

6.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

(1) Preventing Over-Voltage and Over-Current Conditions

Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

(2) Protection of Output Pins

Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.

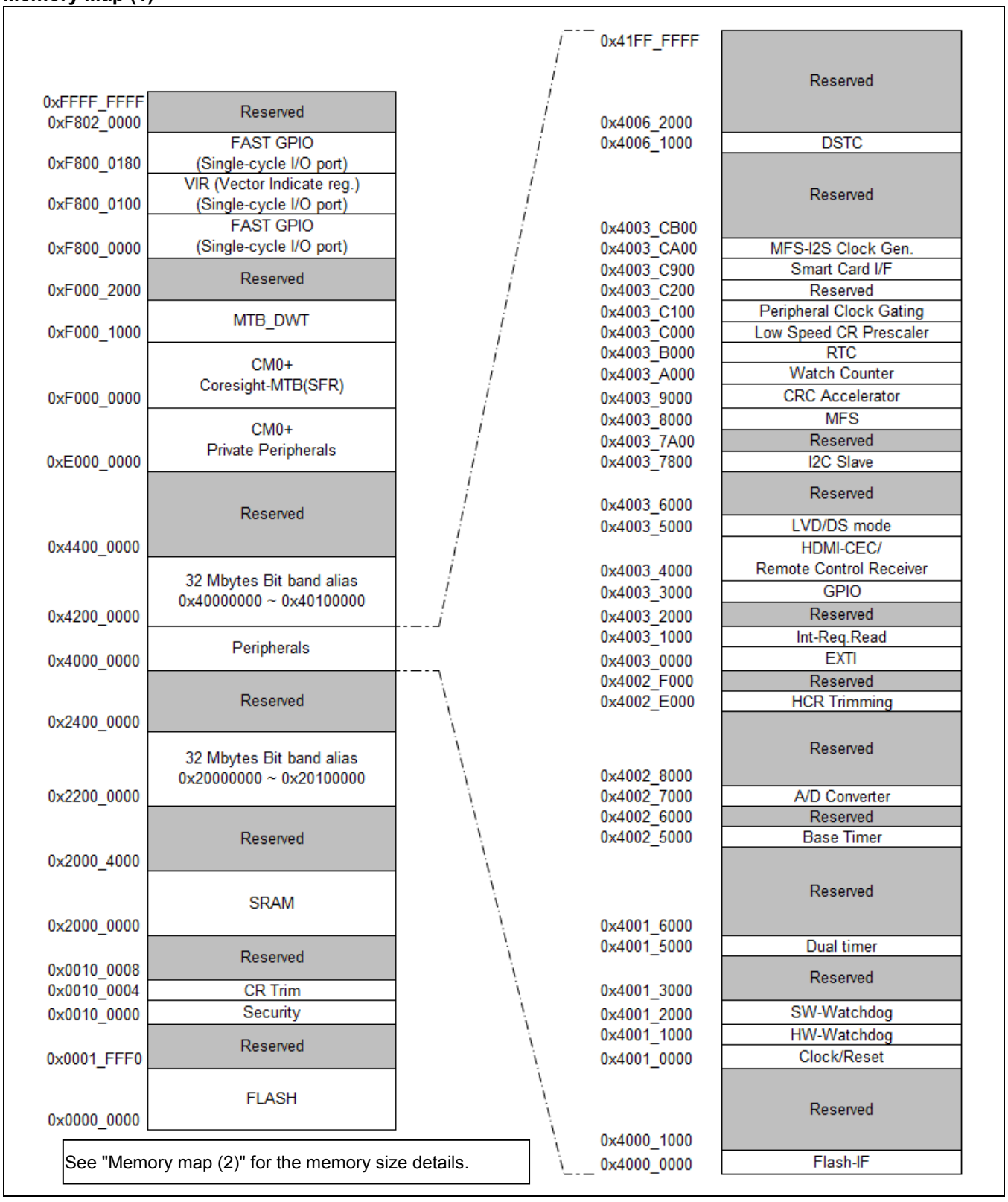
Therefore, avoid this type of connection.

(3) Handling of Unused Input Pins

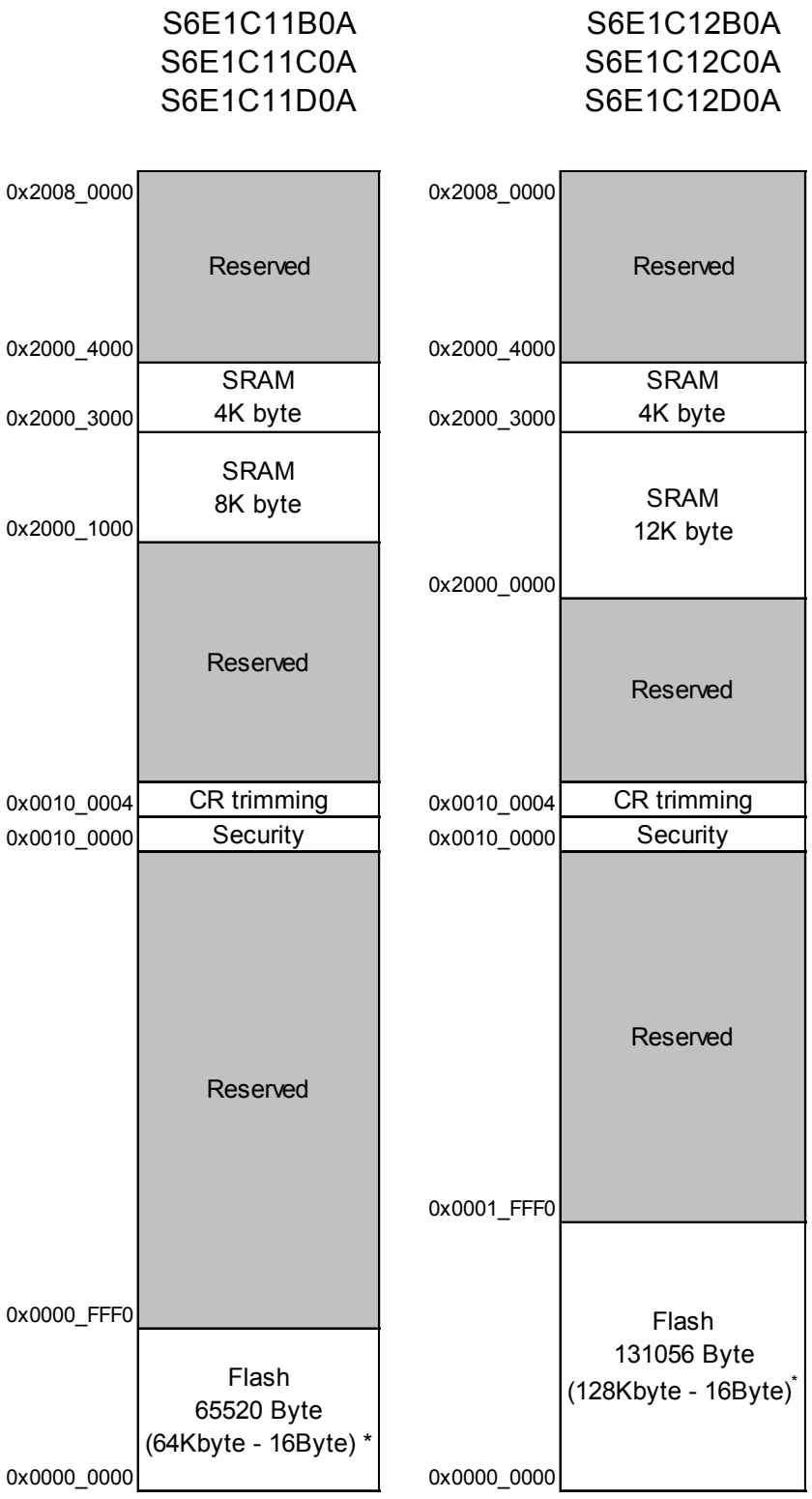
Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

9. Memory Map

Memory Map (1)



Memory Map (2)



*: See "S6E1C1/C3 Series Flash Programming Manual" to check details of the Flash memory.

Peripheral Address Map

Start address	End address	Bus	Peripheral
0x4000_0000	0x4000_0FFF	AHB	Flash memory I/F register
0x4000_1000	0x4000_FFFF		Reserved
0x4001_0000	0x4001_0FFF	APB0	Clock/Reset Control
0x4001_1000	0x4001_1FFF		Hardware Watchdog Timer
0x4001_2000	0x4001_2FFF		Software Watchdog Timer
0x4001_3000	0x4001_4FFF		Reserved
0x4001_5000	0x4001_5FFF		Dual-Timer
0x4001_6000	0x4001_FFFF		Reserved
0x4002_0000	0x4002_0FFF	APB1	Reserved
0x4002_1000	0x4002_3FFF		Reserved
0x4002_4000	0x4002_4FFF		Reserved
0x4002_5000	0x4002_5FFF		Base Timer
0x4002_6000	0x4002_6FFF		Reserved
0x4002_7000	0x4002_7FFF		A/D Converter
0x4002_8000	0x4002_DFFF		Reserved
0x4002_E000	0x4002_EFFF		Built-in CR trimming
0x4002_F000	0x4002_FFFF		Reserved
0x4003_0000	0x4003_0FFF		External Interrupt Controller
0x4003_1000	0x4003_1FFF		Interrupt Request Batch-Read Function
0x4003_2000	0x4003_2FFF		Reserved
0x4003_3000	0x4003_3FFF		GPIO
0x4003_4000	0x4003_4FFF		HDMI-CEC/Remote Control Receiver
0x4003_5000	0x4003_5FFF		Low-Voltage Detection / DS mode / Vref Calibration
0x4003_6000	0x4003_6FFF		Reserved
0x4003_7000	0x4003_77FF		Reserved
0x4003_7800	0x4003_79FF		I2C Slave
0x4003_7A00	0x4003_7FFF		Reserved
0x4003_8000	0x4003_8FFF		Multi-function Serial Interface
0x4003_9000	0x4003_9FFF		CRC
0x4003_A000	0x4003_AFFF		Watch Counter
0x4003_B000	0x4003_BFFF		Real-time clock
0x4003_C000	0x4003_C0FF		Low-speed CR Prescaler
0x4003_C100	0x4003_C7FF		Peripheral Clock Gating
0x4003_C800	0x4003_C8FF		Reserved
0x4003_C900	0x4003_C9FF		Smart Card Interface
0x4003_CA00	0x4003_CAFF		MFS-I2S Clock Generator
0x4003_CB00	0x4003_FFFF		Reserved
0x4004_0000	0x4004_FFFF	AHB	Reserved
0x4005_0000	0x4006_0FFF		Reserved
0x4006_1000	0x4006_1FFF		DSTC
0x4006_2000	0x41FF_FFFF		Reserved

Type
This indicates a pin status type that is shown in “pin list table” in “4. List of Pin Functions”

Selected Pin function
This indicates a pin function that is selected by user program.

CPU state
This indicates a state of the CPU that is shown below.

(1)	Reset state. CPU is initialized by Power-on reset or a reset due to low Power voltage supply.
(2)	Reset state. CPU is initialized by INITX input signal or system initialization after power on reset.
(3)	Run mode or SLEEP mode state.
(4)	Timer mode, RTC mode or STOP mode state. The standby pin level setting bit (SPL) in the Standby Mode Control Register (STB_CTL) is set to "0".
(5)	Timer mode, RTC mode or STOP mode state. The standby pin level setting bit (SPL) in the Standby Mode Control Register (STB_CTL) is set to "1".
(6)	Deep standby STOP mode or Deep standby RTC mode state, The standby pin level setting bit (SPL) in the Standby Mode Control Register (STB_CTL) is set to "0"
(7)	Deep standby STOP mode or Deep standby RTC mode state, The standby pin level setting bit (SPL) in the Standby Mode Control Register (STB_CTL) is set to "1"
(8)	Run mode state after returning from Deep Standby mode. (I/O state hold function(CONTX) is fixed at 1)

Each pin status
The meaning of the symbols in the pin status table is as follows.

IS	Digital output is disabled. (Hi-Z) Pull up register is off. Digital input is shut off by fixed 0.
IE	Digital output is disabled. (Hi-Z) Pull up register is off. Digital input is not shut off.
IP	Digital output is disabled. (Hi-Z) Pull up register is defined by the value of the PCR register. Digital input is not shut off.
IE/IS	Digital output is disabled. (Hi-Z) Pull up register is off. Digital input is shut off in case of the OSC stop. Digital input is not shut off in case of the OSC operation.
OE	The OSC is in operation state. However, it may be stopped in some operation mode of the CPU. For detail, see chapter “Low Power Consumption Mode” in peripheral manual.
OS	The OSC is in stop state. (Hi-Z)
PC	Digital output and pull up register is controlled by the register in the GPIO or peripheral function. Digital input is not shut off
CP	Digital output is controlled by the register in the GPIO or peripheral function. Pull up register is off. Digital input is not shut off.
HC	Digital output and pull up register is maintained the status that is immediately prior to entering the current CPU state. Digital input is not shut off
HS	Digital output and pull up register is maintained the status that is immediately prior to entering the current CPU state. Digital input is shut off
GS	Digital output and pull up register is copied the GPIO status that is immediately prior to entering the current CPU state and the status is maintained. Digital input is shut off

11.2 Recommended Operating Conditions

(V_{SS}= 0.0 V)

Parameter	Symbol	Conditions	Value		Unit	Remarks
			Min	Max		
Power supply voltage	V_{CC}	-	1.65 *2	3.6	V	
Analog reference voltage	AVRH	-	2.7	V_{CC}	V	V_{CC} ≥ 2.7 V
			V_{CC}	V_{CC}	V	V_{CC} < 2.7 V
	AVRL	-	VSS	VSS	V	
Smoothing capacitor	C_S	-	1	10	µF	For regulator*1
Operating temperature	Ta	-	- 40	+ 105	°C	

*1: See "C Pin" in "7. Handling Devices" for the connection of the smoothing capacitor.

*2: In between less than the minimum power supply voltage reset / interrupt detection voltage or more, instruction execution and low voltage detection function by built-in High-speed CR (including Main PLL is used) or built-in Low-speed CR is possible to operate only.

<WARNING>

1. *The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.*
2. *Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.*
3. *No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet.*
4. *Users considering application outside the listed conditions are advised to contact their representatives beforehand.*

Peripheral Current Dissipation

(V_{CC}=1.65 V to 3.6 V, V_{SS}=0 V, T_A=- 40°C to +105°C)

Clock System	Peripheral	Conditions	Frequency (MHz)			Unit	Remarks
			8	20	40		
HCLK	GPIO	At all ports operation	0.05	0.12	0.23	mA	
	DSTC	At 2ch operation	0.02	0.06	0.10		
PCLK1	Base timer	At 4ch operation	0.02	0.05	0.10	mA	
	ADC	At 1 unit operation	0.04	0.10	0.21		
	Multi-function serial	At 1ch operation	0.01	0.03	0.06		
	MFS-I2S	At 1ch operation	0.02	0.05	0.08		
	Smart Card I/F	At 1ch operation	0.04	0.08	0.18		

11.4.4 Operating Conditions of Main PLL (In the Case of Using the Main Clock as the Input Clock of the PLL)

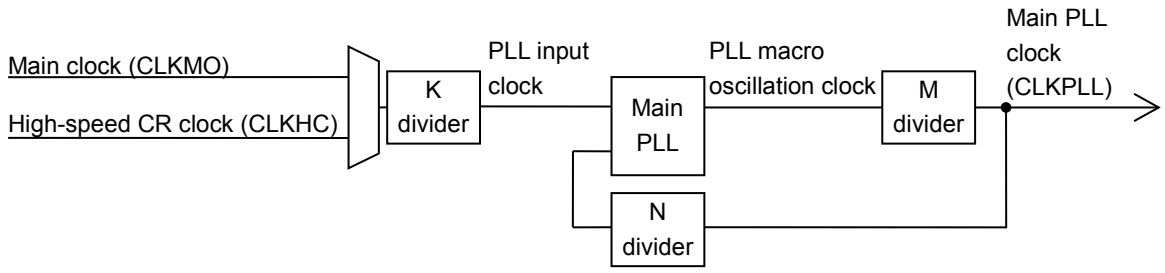
(V_{CC}= 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (LOCK UP time)	t_{LOCK}	50	-	-	µs	
PLL input clock frequency	F_{PLLI}	8	-	16	MHz	
PLL multiple rate	-	5	-	18	multiple	
PLL macro oscillation clock frequency	F_{PLLO}	75	-	150	MHz	
Main PLL clock frequency*2	F_{CLKPLL}	-	-	40	MHz	

*1: The wait time is the time it takes for PLL oscillation to stabilize.

*2: For details of the main PLL clock (CLKPLL), refer to "Chapter: Clock" in "FM0+ Family Peripheral Manual".

Main PLL connection



11.4.5 Operating Conditions of Main PLL (In the Case of Using the Built-in High-Speed CR Clock as the Input Clock of the Main PLL)

(V_{CC}= 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (LOCK UP time)	t_{LOCK}	50	-	-	µs	
PLL input clock frequency	F_{PLLI}	7.84	8	8.16	MHz	
PLL multiple rate	-	9	-	18	multiple	
PLL macro oscillation clock frequency	F_{PLLO}	75	-	150	MHz	
Main PLL clock frequency*2	F_{CLKPLL}	-	-	40.8	MHz	

*1: The wait time is the time it takes for PLL oscillation to stabilize.

*2: For details of the main PLL clock (CLKPLL), refer to "Chapter: Clock" in "FM0+ Family Peripheral Manual".

Note:

- *For the main PLL source clock, input the high-speed CR clock (CLKHC) whose frequency and temperature have been trimmed. When setting PLL multiple rate, please take the accuracy of the built-in High-speed CR clock into account and prevent the master clock from exceeding the maximum frequency.*

When Using CSIO/SPI Chip Select (SCINV=1, CSLVL=1)

(V_{CC}= 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Conditions	V_{CC} < 2.7 V		V_{CC} ≥ 2.7 V		Unit
			Min	Max	Min	Max	
SCS↓→SCK↑ setup time	t_{CSSI}	Master mode	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK↓→SCS↑ hold time	t_{CSHI}		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t_{CSDI}		(*3)-50	(*3)+50	(*3)-50	(*3)+50	ns
SCS↓→SCK↑ setup time	t_{CSSE}	Slave mode	$3t_{CYCP}$+30	-	$3t_{CYCP}$+30	-	ns
SCK↓→SCS↑ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		$3t_{CYCP}$+30	-	$3t_{CYCP}$+30	-	ns
SCS↓→SOT delay time	t_{DSE}		-	55	-	40	ns
SCS↑→SOT delay time	t_{DEE}		0	-	0	-	ns

*1: CSSU bit value × serial chip select timing operating clock cycle.

*2: CSHD bit value × serial chip select timing operating clock cycle.

*3: CSDS bit value × serial chip select timing operating clock cycle.
Irrespective of CSDS bit setting, $5t_{CYCP}$ or more are required for the period the time when the serial chip select pin becomes inactive to the time when the serial chip select pin becomes active again.

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  For information about the APB bus number which Multi-function Serial is connected to, see "8. Block Diagram".
- *For information about CSSU, CSHD, CSDS, serial chip select timing operating clock, see "FM0+ Family Peripheral Manual".*
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCKx_0 and SCSIx_1 is not guaranteed.
- *When the external load capacitance C_L=30 pF.*

11.4.10 External Input Timing

(V_{CC}= 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

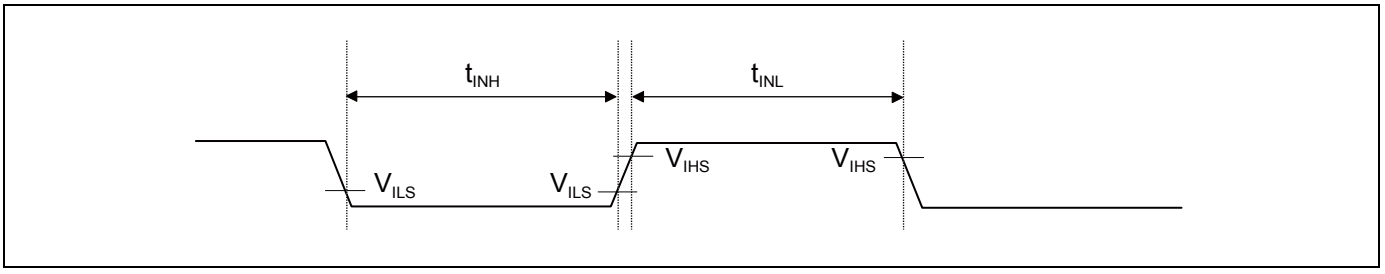
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{INH}, t_{INL}	ADTGx	-	2 t_{CYCP}*1	-	ns	A/D converter trigger input
		INT00 to INT08, INT12, INT13, INT15, NMIX	*2	2 t_{CYCP} +100*1	-	ns	External interrupt, NMI
			*3	500	-	ns	
		WKUPx	*4	500	-	ns	Deep standby wake up

*1: t_{CYCP} represents the APB bus clock cycle time.
For the number of the APB bus to which the Multi-function Timer is connected and that of the APB bus to which the External Interrupt Controller is connected, see "8. Block Diagram".

*2: In Run mode and Sleep mode

*3: In Timer mode, RTC mode and Stop mode

*4: In Deep Standby RTC mode and Deep Standby Stop mode



11.5 12-bit A/D Converter

Electrical Characteristics of A/D Converter (Preliminary Values)

(V_{CC}= 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	12	bit	
Integral Nonlinearity	-	-	- 4.5	-	4.5	LSB	
Differential Nonlinearity	-	-	- 2.5	-	+ 2.5	LSB	
Zero transition voltage	V_{ZT}	ANxx	- 15	-	+ 15	mV	
Full-scale transition voltage	V_{FST}	ANxx	AVRH - 15	-	AVRH + 15	mV	
Conversion time*1	-	-	1.0	-	-	µs	$V_{CC} \geq 2.7$ V
			4.0	-	-		1.8 ≤ V_{CC} < 2.7 V
			10	-	-		1.65 ≤ V_{CC} < 1.8 V
Sampling time *2	Ts	-	0.3	-	10	µs	$V_{CC} \geq 2.7$ V
			1.2	-			1.8 ≤ V_{CC} < 2.7 V
			3.0	-			1.65 ≤ V_{CC} < 1.8 V
Compare clock cycle *3	Tcck	-	50	-	1000	ns	$V_{CC} \geq 2.7$ V
			200	-			1.8 ≤ V_{CC} < 2.7 V
			500	-			1.65 ≤ V_{CC} < 1.8 V
State transition time to operation permission	Tstt	-	-	-	1.0	µs	
Analog input capacity	C_{AIN}	-	-	-	7.5	pF	
Analog input resistance	R_{AIN}	-	-	-	2.2	kΩ	$V_{CC} \geq 2.7$ V
					5.5		1.8 ≤ V_{CC} < 2.7 V
					10.5		1.65 ≤ V_{CC} < 1.8 V
Interchannel disparity	-	-	-	-	4	LSB	
Analog port input leak current	-	ANxx	-	-	5	µA	
Analog input voltage	-	ANxx	V_{SS}	-	AVRH	V	
Reference voltage	-	AVRH	2.7	-	V_{CC}	V	VCC ≥ 2.7V
			V_{CC}				VCC < 2.7V
	-	AVRL	V_{SS}	-	V_{SS}	V	

*1: The conversion time is the value of sampling time (t_S) + compare time (t_C).
The minimum conversion time is computed according to the following conditions:
$V_{CC} \geq 2.7$ V sampling time=0.3 µs, compare time=0.7 µs
1.8 ≤ V_{CC} < 2.7 V sampling time=1.2 µs, compare time=2.8 µs
1.65 ≤ V_{CC} < 1.8 V sampling time=3.0 µs, compare time=7.0 µs
Ensure that the conversion time satisfies the specifications of the sampling time (t_S) and compare clock cycle (t_{CCK}).
For details of the settings of the sampling time and compare clock cycle, refer to "Chapter: A/D Converter" in "FM0+ Family Peripheral Manual Analog Macro Part".
The register settings of the A/D Converter are reflected in the operation according to the APB bus clock timing.
For the number of the APB bus to which the A/D Converter is connected, see "8. Block Diagram".
The base clock (HCLK) is used to generate the sampling time and the compare clock cycle.

*2: The required sampling time varies according to the external impedance.
Set a sampling time that satisfies (Equation 1).

*3: The compare time (t_C) is the result of (Equation 2).

11.8.2 Return Factor: Reset

The return time from Low-Power consumption mode is indicated as follows. It is from releasing reset to starting the program operation.

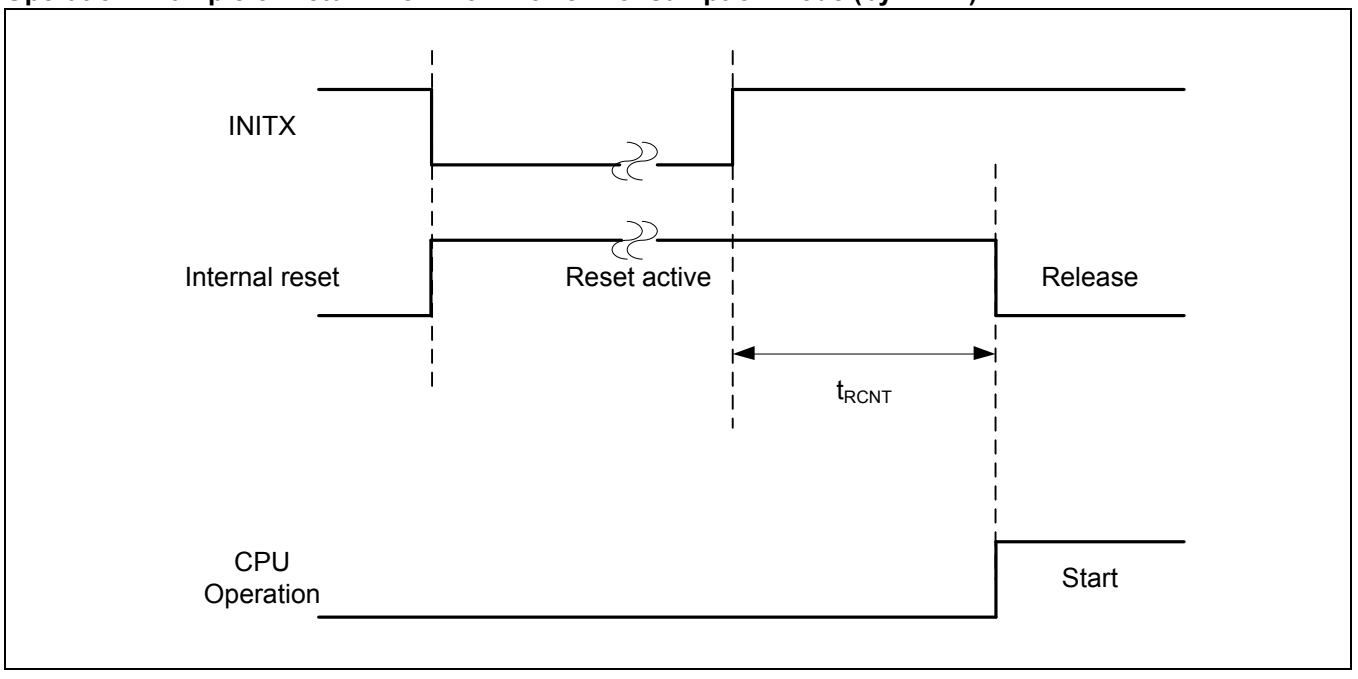
Return Count Time

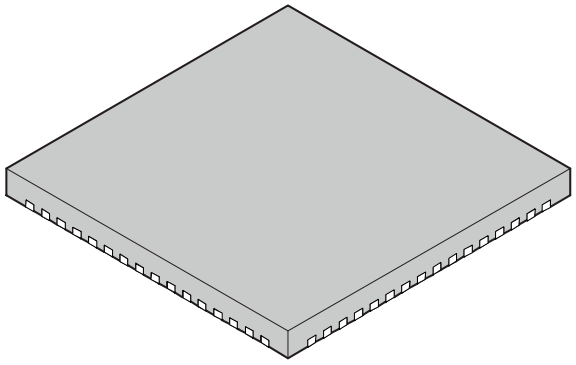
(V_{CC}=1.65 V to 3.6 V, T_A=-40°C to +105°C)

Parameter		Symbol	Value		Unit	Remarks
Current Mode	Mode to return		Typ	Max*		
High-speed CR Sleep mode Main Sleep mode PLL Sleep mode	High-speed CR Run mode	t_{RCNT}	20	22	µs	When High-speed CR is enabled
Low-speed CR Sleep mode			50	106	µs	When High-speed CR is enabled
Sub Sleep mode			112	137	µs	When High-speed CR is enabled
High-speed CR Timer mode Main Timer mode PLL Timer mode			20	22	µs	When High-speed CR is enabled
Low-speed CR Timer mode			87	159	µs	
Sub Timer mode			148	209	µs	
Stop mode RTC mode			45	68	µs	
Deep Standby RTC mode Deep Standby Stop mode			43	281	µs	

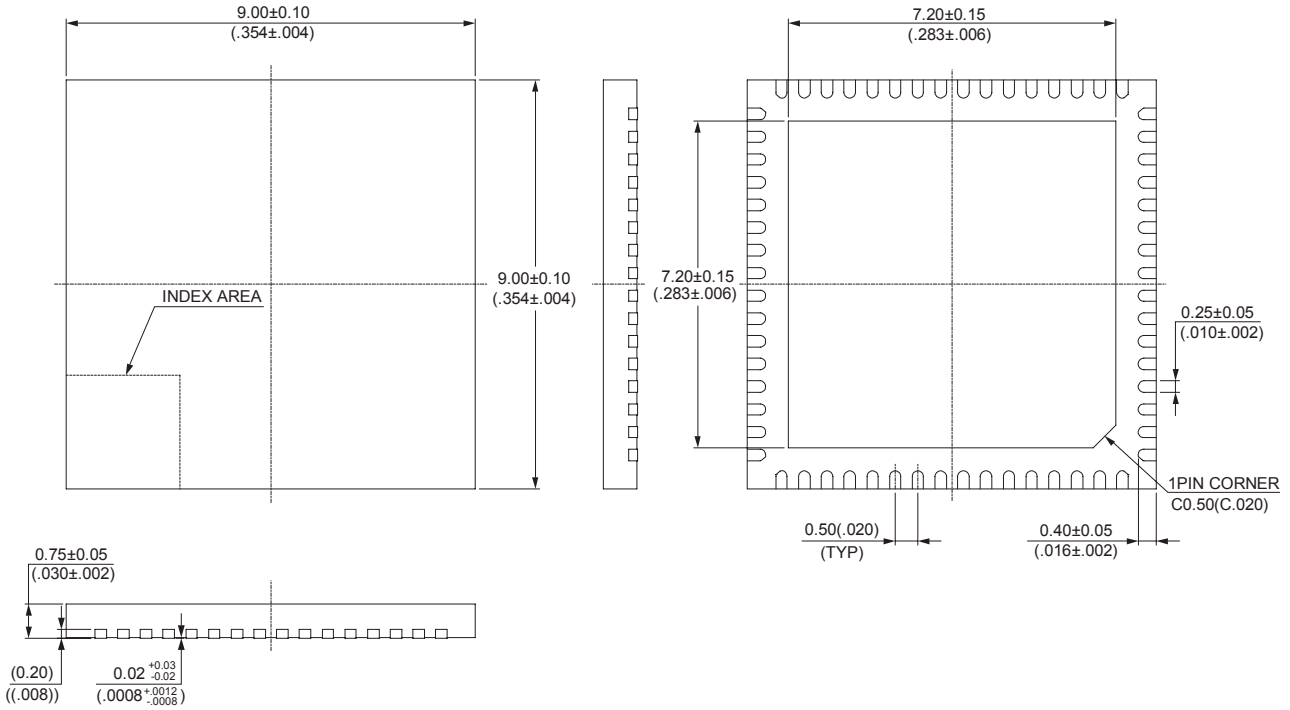
*: The maximum value depends on the accuracy of built-in CR.

Operation Example of Return from Low-Power Consumption Mode (by INITX)



64-pin plastic QFN		
	Lead pitch	0.50 mm
	Package width × package length	9.00 mm × 9.00 mm
	Sealing method	Plastic mold
	Mounting height	0.80 mm MAX
	Weight	0.21 g
(LCC-64P-M25)		

64-pin plastic QFN
(LCC-64P-M25)



Dimensions in mm (inches).
Note: The values in parentheses are reference values.