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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	CSIO, I²C, LINbus, SmartCard, UART/USART
Peripherals	I²S, LVD, POR, PWM, WDT
Number of I/O	54
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e1c11d0agv20000

- 16-bit PWM timer
- 16-bit PPG timer
- 16/32-bit reload timer
- 16/32-bit PWC timer

General-Purpose I/O Port

This series can use its pin as a general-purpose I/O port when it is not used for an external bus or a peripheral function. All ports can be set to fast general-purpose I/O ports or slow general-purpose I/O ports. In addition, this series has a port relocate function that can set to which I/O port a peripheral function can be allocated.

- All ports are Fast GPIO which can be accessed by 1cycle
- Capable of controlling the pull-up of each pin
- Capable of reading pin level directly
- Port relocate function
- Up to 54 fast general-purpose I/O ports @64-pin package
- Certain ports are 5 V tolerant.
  See 4.List of Pin Functions and 5.I/O Circuit Type for the corresponding pins.

Dual Timer (32-/16-bit Down Counter)

The Dual Timer consists of two programmable 32-/16-bit down counters. The operation mode of each timer channel can be selected from one of the following.

- Free-running mode
- Periodic mode (= Reload mode)
- One-shot mode

Real-Time Clock

The Real-time Clock counts year/month/day/hour/minute/second/day of the week from year 00 to year 99.

- The RTC can generate an interrupt at a specific time (year/month/day/hour/minute/second/day of the week) and can also generate an interrupt in a specific year, in a specific month, on a specific day, at a specific hour or at a specific minute.
- It has a timer interrupt function generating an interrupt upon a specific time or at specific intervals.
- It can keep counting while rewriting the time.
- It can count leap years automatically.

Watch Counter

The Watch Counter wakes up the microcontroller from the low power consumption mode. The clock source can be selected from the main clock, the sub clock, the built-in high-speed CR clock or the built-in low-speed CR clock.

Interval timer: up to 64 s (sub clock: 32.768 kHz)

External Interrupt Controller Unit

- Up to 12 external interrupt input pins
- Non-maskable interrupt (NMI) input pin: 1

Watchdog Timer (2 Channels)

The watchdog timer generates an interrupt or a reset when the counter reaches a time-out value.

This series consists of two different watchdogs, hardware watchdog and software watchdog.

The hardware watchdog timer is clocked by the built-in low-speed CR oscillator. Therefore, the hardware watchdog is active in any low-power consumption modes except RTC, Stop, Deep standby RTC and Deep standby Stop mode.

CRC (Cyclic Redundancy Check) Accelerator

The CRC accelerator calculates the CRC which has a heavy software processing load, and achieves a reduction of the integrity check processing load for reception data and storage.

- CCITT CRC16 and IEEE-802.3 CRC32 are supported.
  - CCITT CRC16 Generator Polynomial: 0x1021
  - IEEE-802.3 CRC32 Generator Polynomial: 0x04C11DB7

HDMI-CEC/Remote Control Receiver (Up to 2 Channels)

- HDMI-CEC transmitter
  - Header block automatic transmission by judging Signal free
  - Generating status interrupt by detecting Arbitration lost
  - Generating START, EOM, ACK automatically to output CEC transmission by setting 1 byte data
  - Generating transmission status interrupt when transmitting 1 block (1 byte data and EOM/ACK)
- HDMI-CEC receiver
  - Automatic ACK reply function available
  - Line error detection function available
- Remote control receiver
  - 4 bytes reception buffer
  - Repeat code detection function available

Smart Card Interface (Max 1 Channel)

- Compliant with ISO7816-3 specification
- Card Reader only/B class card only
- Available protocols
  - Transmitter: 8E2, 8O2, 8N2
  - Receiver: 8E1, 8O1, 8N2, 8N1, 9N1
  - Inverse mode
- TX/RX FIFO integrated (RX: 16-bytes, TX:16-bytes)

Clock and Reset

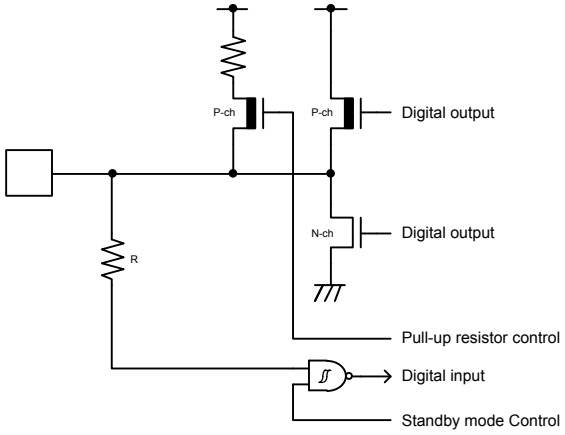
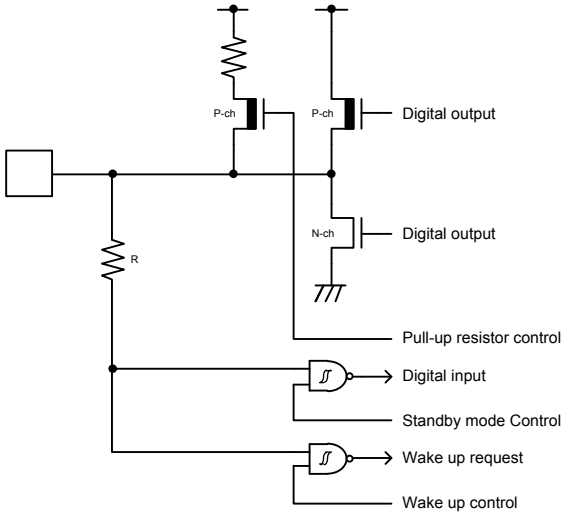
- Clocks

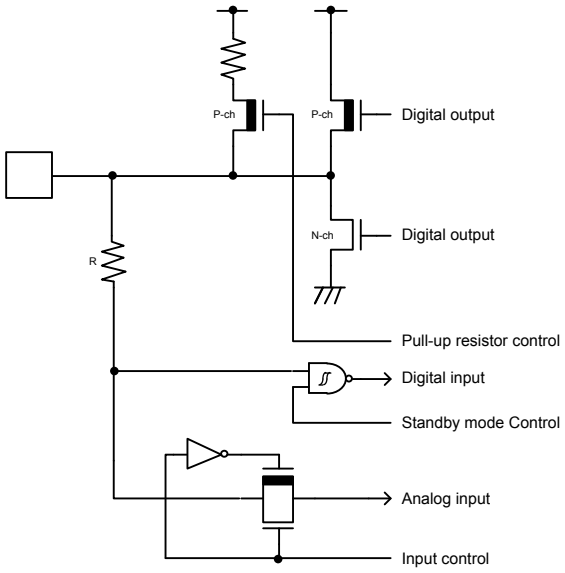
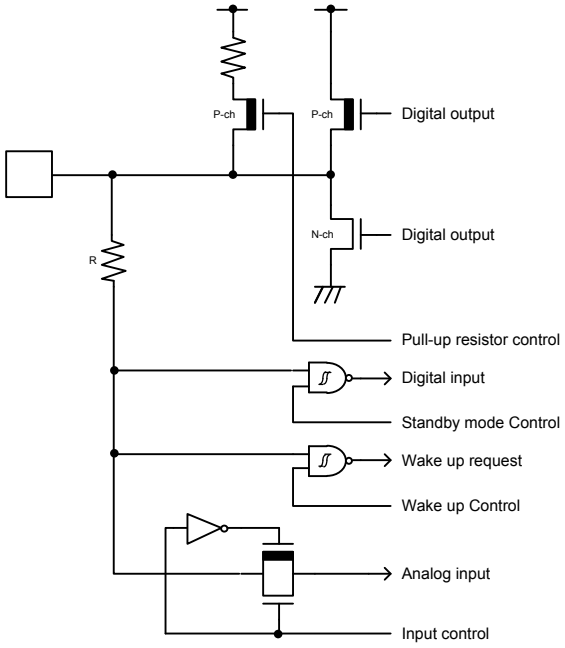
A clock can be selected from five clock sources (two external oscillators, two built-in CR oscillator, and main PLL).

  - Main clock: 8 MHz to 48 MHz

Pin no.			Pin Function	I/O circuit type	Pin state type
LQFP-64 QFN-64	LQFP-48 QFN-48	LQFP-32 QFN-32			
45	33	-	P15	F	J
			AN05		
			SOT0_1		
			SCS11_1		
46	34	22	P23	F	J
			AN06		
			SCK0_0		
			TIOA7_1		
47	35	23	P22	F	J
			AN07		
			TIOB7_1		
48	36	24	VCC	-	-
49	37	-	AVRH *	-	-
50	38	25	AVRL	-	-
51	39	26	P21	E	K
			INT06_1		
			WKUP2		
52	-	-	P00	E	K
			WKUP4		
53	40	27	P01	D	K
			SWCLK		
			SOT0_0		
54	-	-	P02	E	K
			WKUP5		
55	41	28	P03	D	K
			SWDIO		
			SIN0_0		
			TIOB7_0		
56	42	29	P05	E	K
			MD1		
			TIOA5_2		
			INT00_1		
			WKUP3		
57	43	-	VCC	-	-
58	44	30	P80	J	G
59	45	31	P81	J	G
60	46	32	VSS	-	-
61	47	-	P61	H	K
			TIOB2_2		
62	-	-	P0B	E	K
			TIOB6_1		
			WKUP6		
63	-	-	P0C	E	K
			TIOA6_1		
			WKUP7		

Pin function	Pin name	Function description	Pin no.		
			LQFP-64 QFN-64	LQFP-48 QFN-48	LQFP-32 QFN-32
GPIO	P30	General-purpose I/O port 3	5	5	-
	P31		6	6	5
	P32		7	7	6
	P33		8	8	7
	P34		9	9	-
	P35		10	-	-
	P3A		11	10	-
	P3B		12	11	-
	P3C		13	12	-
	P3D		14	-	-
	P3E		15	-	-
	P3F		16	-	-
GPIO	P40	General-purpose I/O port 4	20	-	-
	P41		21	-	-
	P42		22	-	-
	P43		23	-	-
	P46		30	22	14
	P47		31	23	15
	P4C		24	16	-
	P4D		25	17	-
	P4E		26	18	-
GPIO	P50	General-purpose I/O port 5	1	1	2
	P51		2	2	3
	P52		3	3	4
	P53		4	4	-
GPIO	P60	General-purpose I/O port 6	33	25	17
	P61		61	47	-
GPIO	P80	General-purpose I/O port 8	58	44	30
	P81		59	45	31
GPIO	PE2	General-purpose I/O port E	18	14	9
	PE3		19	15	10
Multi-function Serial 0	SIN0_0	Multi-function serial interface ch.0 input pin	55	41	28
	SIN0_1		44	32	-
	SOT0_0 (SDA0_0)	Multi-function serial interface ch.0 output pin. This pin operates as SOT0 when used as a UART/CSIO/LIN pin (operation mode 0 to 3) and as SDA0 when used as an I2C pin (operation mode 4).	53	40	27
	SOT0_1 (SDA0_1)		45	33	-
	SCK0_0 (SCL0_0)	Multi-function serial interface ch.0 clock I/O pin. This pin operates as SCK0 when used as a CSIO pin (operation mode 2) and as SCL0 when used as an I2C pin (operation mode 4).	46	34	22

Type	Circuit	Remarks
D		・CMOS level output ・CMOS level hysteresis input ・With pull-up resistor control ・With standby mode control ・Pull-up resistor : Approximately 33kΩ ・IOH= -4mA, IOL= 4mA ・When this pin is used as an I2C pin, the digital output P-ch transistor is always off
E		・CMOS level output ・CMOS level hysteresis input ・With pull-up resistor control ・With standby mode control ・Pull-up resistor : Approximately 33kΩ ・IOH= -4mA, IOL= 4mA ・When this pin is used as an I2C pin, the digital output P-ch transistor is always off

Type	Circuit	Remarks
F		・CMOS level output ・CMOS level hysteresis input ・With input control ・Analog input ・With pull-up resistor control ・With standby mode control ・Pull-up resistor : Approximately 33kΩ ・IOH= -4mA, IOL= 4mA ・When this pin is used as an I2C pin, the digital output P-ch transistor is always off
G		・CMOS level output ・CMOS level hysteresis input ・With input control ・Analog input ・With pull-up resistor control ・With standby mode control ・Pull-up resistor : Approximately 33kΩ ・IOH= -4mA, IOL= 4mA ・When this pin is used as an I2C pin, the digital output P-ch transistor is always off

6. Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Spansion semiconductor devices.

6.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

(1) Preventing Over-Voltage and Over-Current Conditions

Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

(2) Protection of Output Pins

Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.

Therefore, avoid this type of connection.

(3) Handling of Unused Input Pins

Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

Latch-Up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

(1) Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.

(2) Be sure that abnormal current flows do not occur during the power-on sequence.

Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

Precautions Related to Usage of Devices

Spansion semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

6.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Spansion's recommended conditions. For detailed information about mount conditions, contact your sales representative.

Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Spansion recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

7. Handling Devices

Power Supply Pins

In products with multiple VCC and VSS pins, respective pins at the same potential are interconnected within the device in order to prevent malfunctions such as latch-up. However, all of these pins should be connected externally to the power supply or ground lines in order to reduce electromagnetic emission levels, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Moreover, connect the current supply source with each Power supply pin and GND pin of this device at low impedance. It is also advisable that a ceramic capacitor of approximately 0.1 µF be connected as a bypass capacitor between each Power supply pin and GND pin, between AVRH pin and AVRL pin near this device.

Stabilizing Supply Voltage

A malfunction may occur when the power supply voltage fluctuates rapidly even though the fluctuation is within the recommended operating conditions of the VCC power supply voltage. As a rule, with voltage stabilization, suppress the voltage fluctuation so that the fluctuation in VCC ripple (peak-to-peak value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the VCC value in the recommended operating conditions, and the transient fluctuation rate does not exceed 0.1 V/µs when there is a momentary fluctuation on switching the power supply.

Crystal Oscillator Circuit

Noise near the X0/X1 and X0A/X1A pins may cause the device to malfunction. Design the printed circuit board so that X0/X1, X0A/X1A pins, the crystal oscillator, and the bypass capacitor to ground are located as close to the device as possible.

It is strongly recommended that the PC board artwork be designed such that the X0/X1 and X0A/X1A pins are surrounded by ground plane as this is expected to produce stable operation.

Evaluate oscillation of your using crystal oscillator by your mount board.

Sub Crystal Oscillator

This series sub oscillator circuit is low gain to keep the low current consumption. The crystal oscillator to fill the following conditions is recommended for sub crystal oscillator to stabilize the oscillation.

■Surface mount type

Size: More than 3.2 mm × 1.5 mm

Load capacitance: Approximately 6 pF to 7 pF

■Lead type

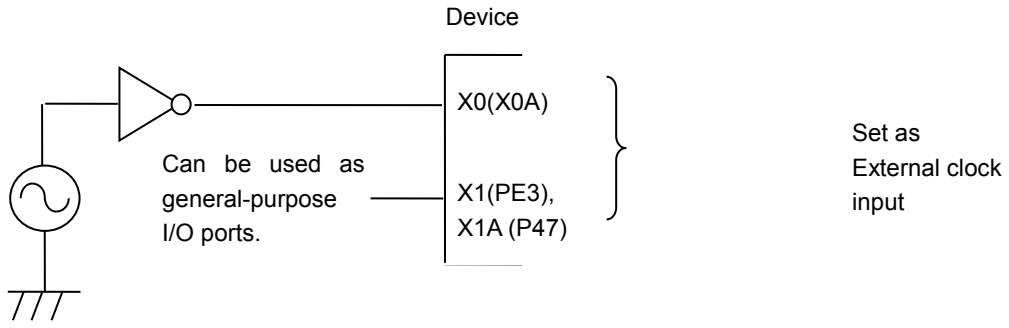
Load capacitance: Approximately 6 pF to 7 pF

Using an External Clock

When using an external clock as an input of the main clock, set X0/X1 to the external clock input, and input the clock to X0. X1(PE3) can be used as a general-purpose I/O port.
Similarly, when using an external clock as an input of the sub clock, set X0A/X1A to the external clock input, and input the clock to X0A. X1A (P47) can be used as a general-purpose I/O port.

However in the Deep Standby mode, an external clock as an input of the sub clock cannot be used.

Example of Using an External Clock



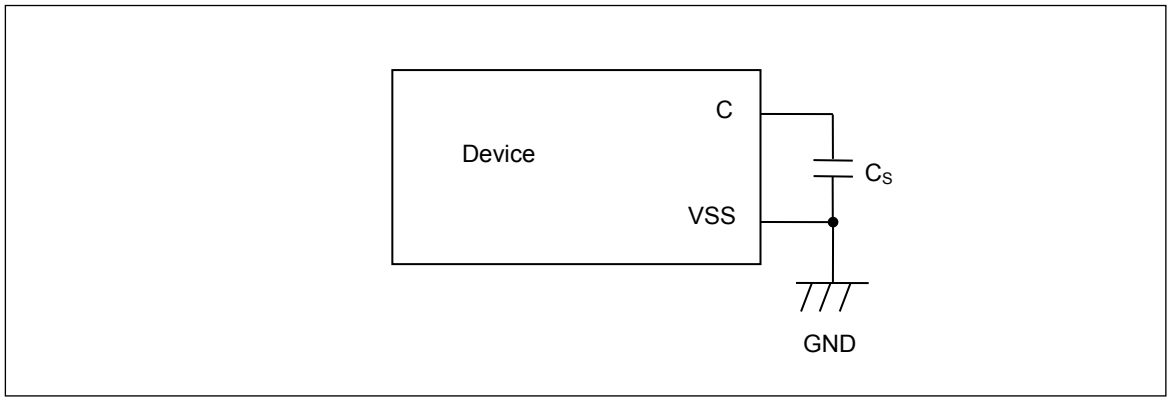
Handling when Using Multi-Function Serial Pin as I²C Pin

If it is using the multi-function serial pin as I²C pins, P-ch transistor of digital output is always disabled. However, I²C pins need to keep the electrical characteristic like other pins and not to connect to the external I²C bus system with power OFF.

C Pin

This series contains the regulator. Be sure to connect a smoothing capacitor (C_S) for the regulator between the C pin and the GND pin. Please use a ceramic capacitor or a capacitor of equivalent frequency characteristics as a smoothing capacitor.
However, some laminated ceramic capacitors have the characteristics of capacitance variation due to thermal fluctuation (F characteristics and Y5V characteristics). Please select the capacitor that meets the specifications in the operating conditions to use by evaluating the temperature characteristics of a capacitor.
A smoothing capacitor of about 4.7 µF would be recommended for this series.

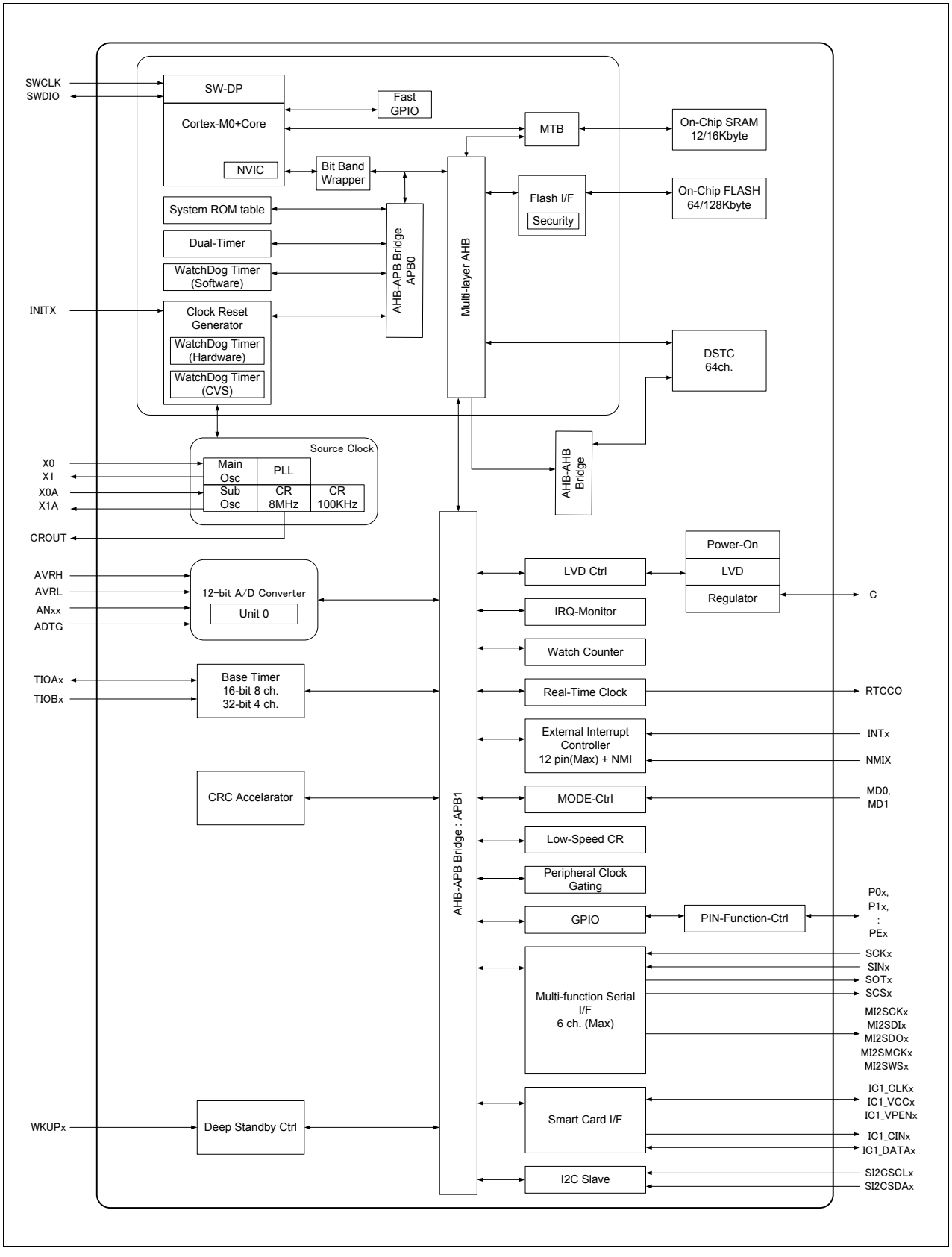
Incidentally, the C pin becomes floating in Deep standby mode.



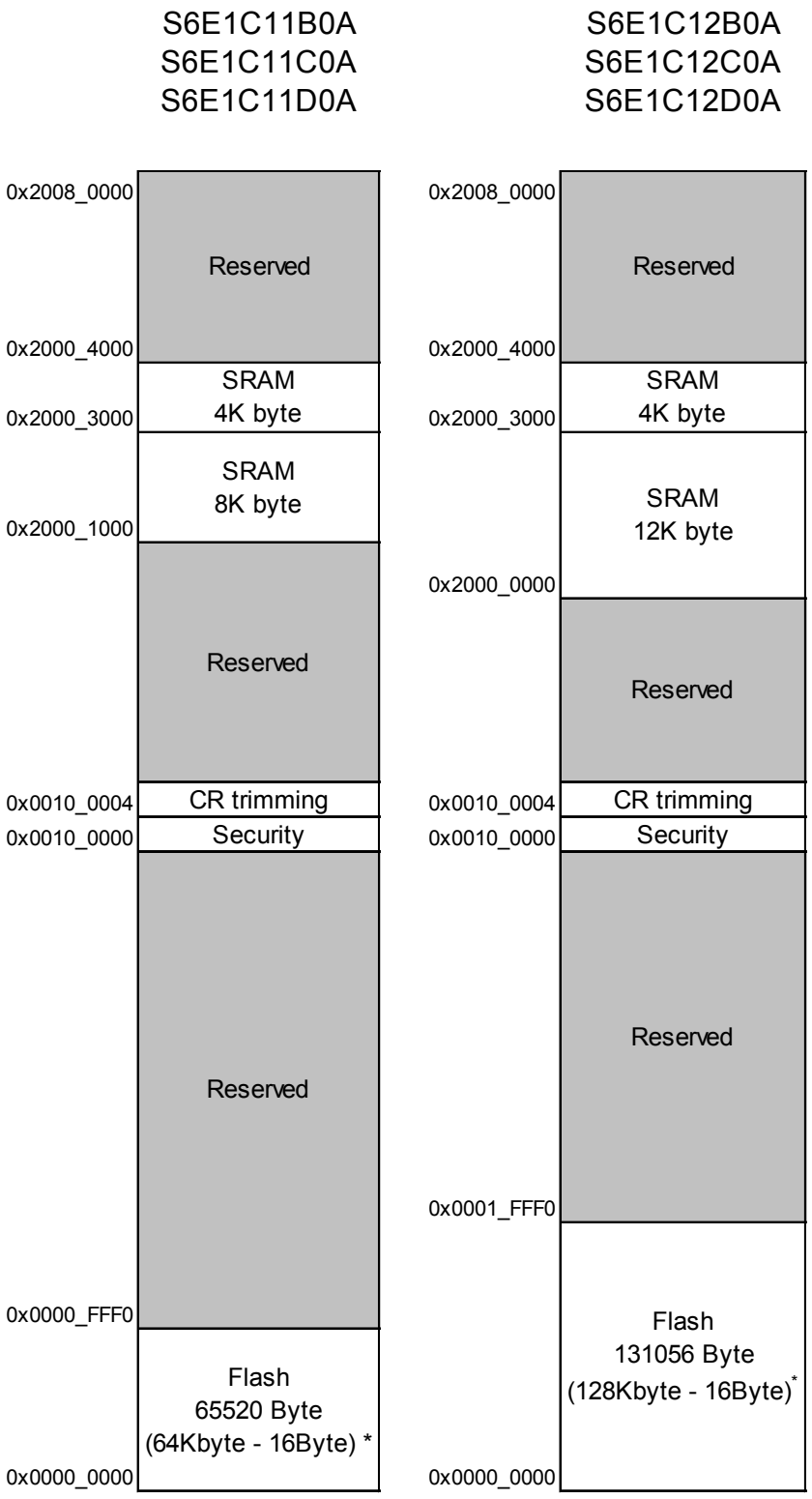
Mode Pins (MD0)

Connect the MD pin (MD0) directly to VCC or VSS pins. Design the printed circuit board such that the pull-up/down resistance stays low, as well as the distance between the mode pins and VCC pins or VSS pins is as short as possible and the connection impedance is low, when the pins are pulled-up/down such as for switching the pin level and rewriting the Flash memory data. It is because of preventing the device erroneously switching to test mode due to noise.

8. Block Diagram



Memory Map (2)



*: See "S6E1C1/C3 Series Flash Programming Manual" to check details of the Flash memory.

Additional note

Additional note is described below.

*1 In this type, when internal oscillation function is selected, digital output is disabled. (Hi-Z) pull up register is off, digital input is shut off by fixed 0.

*2 In this type, when Digital I/O function is selected, internal oscillation function is disabled.

*3 In this type, when analog input function is selected, digital output is disabled, (Hi-Z). pull up register is off, digital input is shut off by fixed 0.

*4 In this type, when Digital I/O function is selected, analog input function is not available.

*5 In this case, PCR register is initialized to “1”. Pull up register is on.

*6 This pin does not have pull up register.

11.3 DC Characteristics

11.3.1 Current Rating

Symbol (Pin Name)	Conditions		HCLK Frequency*4	Value Typ*1	Value Max*2	Unit	Remarks
Icc (VCC)	Run mode, code executed from Flash	8 MHz external clock input, PLL ON*8 NOP code executed Built-in high speed CR stopped	8 MHZ	1.4	2.7	mA	*3
			20 MHZ	2.6	4.1		
			40 MHZ	3.9	5.6		
		8 MHz external clock input, PLL ON*8 Benchmark code executed Built-in high speed CR stopped	8 MHZ	1.3	2.6	mA	*3
			20 MHZ	2.3	3.8		
			40 MHZ	3.4	5.1		
		8 MHz crystal oscillation, PLL ON*8 NOP code executed Built-in high speed CR stopped	8 MHZ	1.6	3.0	mA	*3
			20 MHZ	2.8	4.4		
			40 MHZ	4.1	5.9		
	Run mode, code executed from RAM	8 MHz external clock input, PLL ON*8 NOP code executed Built-in high speed CR stopped	8 MHZ	1.0	2.1	mA	*3
			20 MHZ	1.7	2.9		
			40 MHZ	2.7	4.0		
	Run mode, code executed from Flash	8 MHz external clock input, PLL ON NOP code executed Built-in high speed CR stopped PCLK1 stopped	40 MHZ	1.6	3.1	mA	*3,*6,*7
	Run mode, code executed from Flash	Built-in high speed CR*5 NOP code executed All peripheral clock stopped by CKENx	8 MHZ	1.1	2.4	mA	*3
		32 kHz crystal oscillation NOP code executed All peripheral clock stopped by CKENx	32 kHZ	240	1264	µA	*3
		Built-in low speed CR NOP code executed All peripheral clock stopped by CKENx	100 kHZ	246	1271	µA	*3
Iccs (VCC)	Sleep operation	8 MHz external clock input, PLL ON*8 All peripheral clock stopped by CKENx	8 MHZ	0.8	1.9	mA	*3
			20 MHZ	1.3	2.4		
			40 MHZ	1.8	3.0		
		Built-in high speed CR*5 All peripheral clock stopped by CKENx	8 MHZ	0.6	1.7	mA	*3
		32 kHz crystal oscillation All peripheral clock stopped by CKENx	32 kHZ	237	1261	µA	*3
		Built-in low speed CR All peripheral clock stopped by CKENx	100 kHZ	238	1262	µA	*3

*1 : T_A=+25°C,V_{CC}=3.3 V
*2 : T_A=+105°C,V_{CC}=3.6 V
*3 : All ports are fixed
*4 : PCLK0 is set to divided rate 8
*5 : The frequency is set to 8 MHz by trimming
*6 : Flash sync down is set to FRWTR.RWT=111 and FSYNDN.SD=1111
*7 : VCC=1.65 V
*8 : When HCLK=8 MHz, PLL OFF

11.3.2 Pin Characteristics

(V_{CC} = 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
H level input voltage (hysteresis input)	V_{IHS}	CMOS hysteresis input pin, MD0	$V_{CC} \geq 2.7$ V	$V_{CC} \times 0.8$	-	V_{CC} +0.3	V	
			$V_{CC} < 2.7$ V	$V_{CC} \times 0.7$				
		5 V tolerant input pin	$V_{CC} \geq 2.7$ V	$V_{CC} \times 0.8$	-	V_{SS} +5.5	V	
			$V_{CC} < 2.7$ V	$V_{CC} \times 0.7$				
L level input voltage (hysteresis input)	V_{ILS}	CMOS hysteresis input pin, MD0	$V_{CC} \geq 2.7$ V	V_{SS} - 0.3	-	$V_{CC} \times 0.2$	V	
			$V_{CC} < 2.7$ V			$V_{CC} \times 0.3$		
		5 V tolerant input pin	$V_{CC} \geq 2.7$ V	V_{SS} - 0.3	-	$V_{CC} \times 0.2$	V	
			$V_{CC} < 2.7$ V		-	$V_{CC} \times 0.3$		
H level output voltage	V_{OH}	4 mA type	$V_{CC} \geq 2.7$ V, I_{OH} = - 4 mA	V_{CC} - 0.5	-	V_{CC}	V	
			$V_{CC} < 2.7$ V, I_{OH} = - 2 mA	V_{CC} - 0.45				
L level output voltage	V_{OL}	4 mA type	$V_{CC} \geq 2.7$ V, I_{OL} 4 mA	V_{SS}	-	0.4	V	
			$V_{CC} < 2.7$ V, I_{OL}=2 mA					
Input leak current	I_{IL}	-	-	- 5	-	+ 5	µA	
Pull-up resistance value	R_{PU}	Pull-up pin	$V_{CC} \geq 2.7$ V	21	33	48	kΩ	
			$V_{CC} < 2.7$ V	-	-	88		
Input capacitance	C_{IN}	Other than VCC, VSS, AVRH	-	-	5	15	pF	

CSIO (SPI=0, SCINV=1)

(V_{CC}= 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin name	Conditions	V_{CC} < 2.7V		V_{CC} ≥ 2.7V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	4 t_{CYCP}	-	4 t_{CYCP}	-	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↓ setup time	t_{IVSLI}	SCKx, SINx		50	-	36	-	ns
SCK ↓ → SIN hold time	t_{SLIXI}	SCKx, SINx		0	-	0	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	Slave mode	2 t_{CYCP} - 10	-	2 t_{CYCP} - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCKx, SOTx		-	50	-	33	ns
SIN → SCK ↓ setup time	t_{IVSLE}	SCKx, SINx		10	-	10	-	ns
SCK ↓ → SIN hold time	t_{SLIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	tF	SCKx		-	5	-	5	ns
SCK rising time	tR	SCKx		-	5	-	5	ns

Notes:

- *The above AC characteristics are for clock synchronous mode.*
- *t_{CYCP} represents the APB bus clock cycle time.*
  For the number of the APB bus to which Multi-function Serial has been connected, see "8. Block Diagram".
- *The characteristics are only applicable when the relocate port numbers are the same.*
  For instance, they are not applicable for the combination of SCKx_0 and SOTx_1.
- *External load capacitance C_L=30 pF*

When Using CSIO/SPI Chip Select (SCINV=0, CSLVL=1)

(V_{CC}= 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Conditions	V_{CC} < 2.7 V		V_{CC} ≥ 2.7 V		Unit
			Min	Max	Min	Max	
SCS↓→SCK↓ setup time	t_{CSSI}	Master mode	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK↑→SCS↑ hold time	t_{CSHI}		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t_{CSDI}		(*3)-50	(*3)+50	(*3)-50	(*3)+50	ns
SCS↓→SCK↓ setup time	t_{CSSE}	Slave mode	$3t_{CYCP}$+30	-	$3t_{CYCP}$+30	-	ns
SCK↑→SCS↑ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		$3t_{CYCP}$+30	-	$3t_{CYCP}$+30	-	ns
SCS↓→SOT delay time	t_{DSE}		-	55	-	40	ns
SCS↑→SOT delay time	t_{DEE}		0	-	0	-	ns

*1: CSSU bit value × serial chip select timing operating clock cycle.

*2: CSHD bit value × serial chip select timing operating clock cycle.

*3: CSDS bit value × serial chip select timing operating clock cycle.
Irrespective of CSDS bit setting, $5t_{CYCP}$ or more are required for the period the time when the serial chip select pin becomes inactive to the time when the serial chip select pin becomes active again.

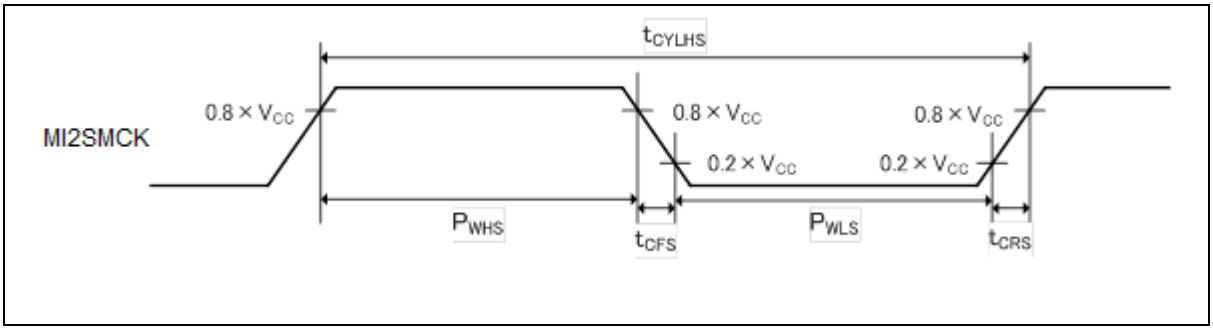
Notes:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  For information about the APB bus number which Multi-function Serial is connected to, see "8. Block Diagram".
- *For information about CSSU, CSHD, CSDS, serial chip select timing operating clock, see "FM0+ Family Peripheral Manual".*
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCKx_0 and SCSIx_1 is not guaranteed.
- *When the external load capacitance C_L=30 pF.*

MI2SMCK Input Characteristics

(V_{CC}= 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	f_{CHS}	MI2SMCK	-	-	12.288	MHz	
Input clock cycle	t_{CYLHS}	-	-	81.3	-	ns	
Input clock pulse width	-	-	P_{WHS}/t_{CYLHS} P_{WLS}/t_{CYLHS}	45	55	%	When using external clock
Input clock rise time and fall time	t_{CFS} t_{CRS}	-	-	-	5	ns	When using external clock

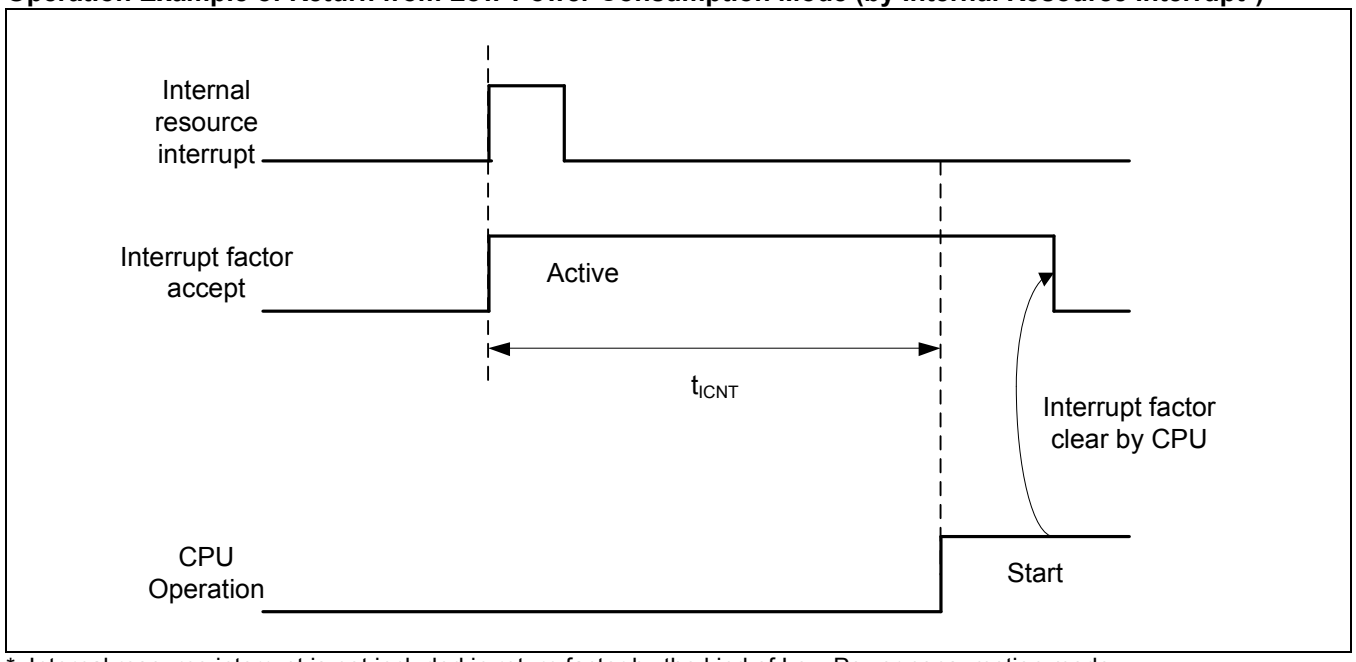


MI2SMCK Output Characteristics

(V_{CC}= 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Output frequency	f_{CHS}	MI2SMCK	-	-	25	MHz	$V_{CC} \geq 2.7$ V
				-	20	MHz	$V_{CC} < 2.7$ V

Operation Example of Return from Low-Power Consumption Mode (by Internal Resource Interrupt*)



*: Internal resource interrupt is not included in return factor by the kind of Low-Power consumption mode.

Notes:

- *The return factor is different in each Low-Power consumption modes.*
  See "Chapter: Low Power Consumption Mode" and "Operations of Standby Modes" in FM0+ Family Peripheral Manual.
- *When interrupt recoveries, the operation mode that CPU recoveries depends on the state before the Low-Power consumption mode transition. See "Chapter: Low Power Consumption Mode" in "FM0+ Family Peripheral Manual".*

Document History

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	4896074	TEKA	08/31/2015	New Spec.
*A	4955136	TEKA	10/9/2015	AC/DC characteristics updated. Typo fixed in “List of Pin Functions”.

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