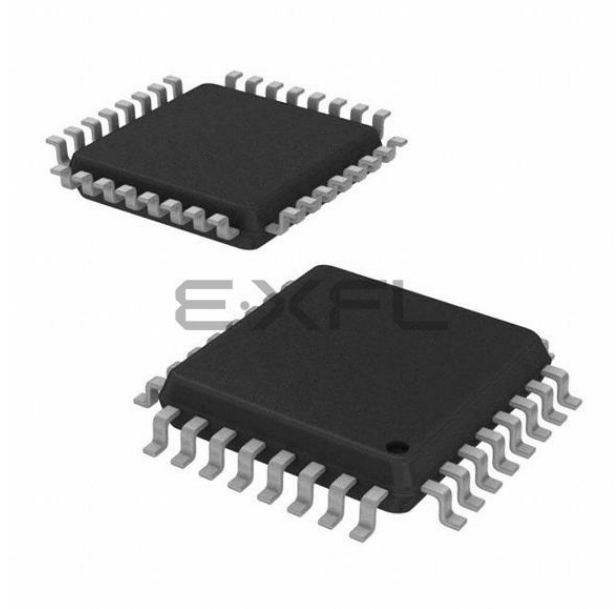

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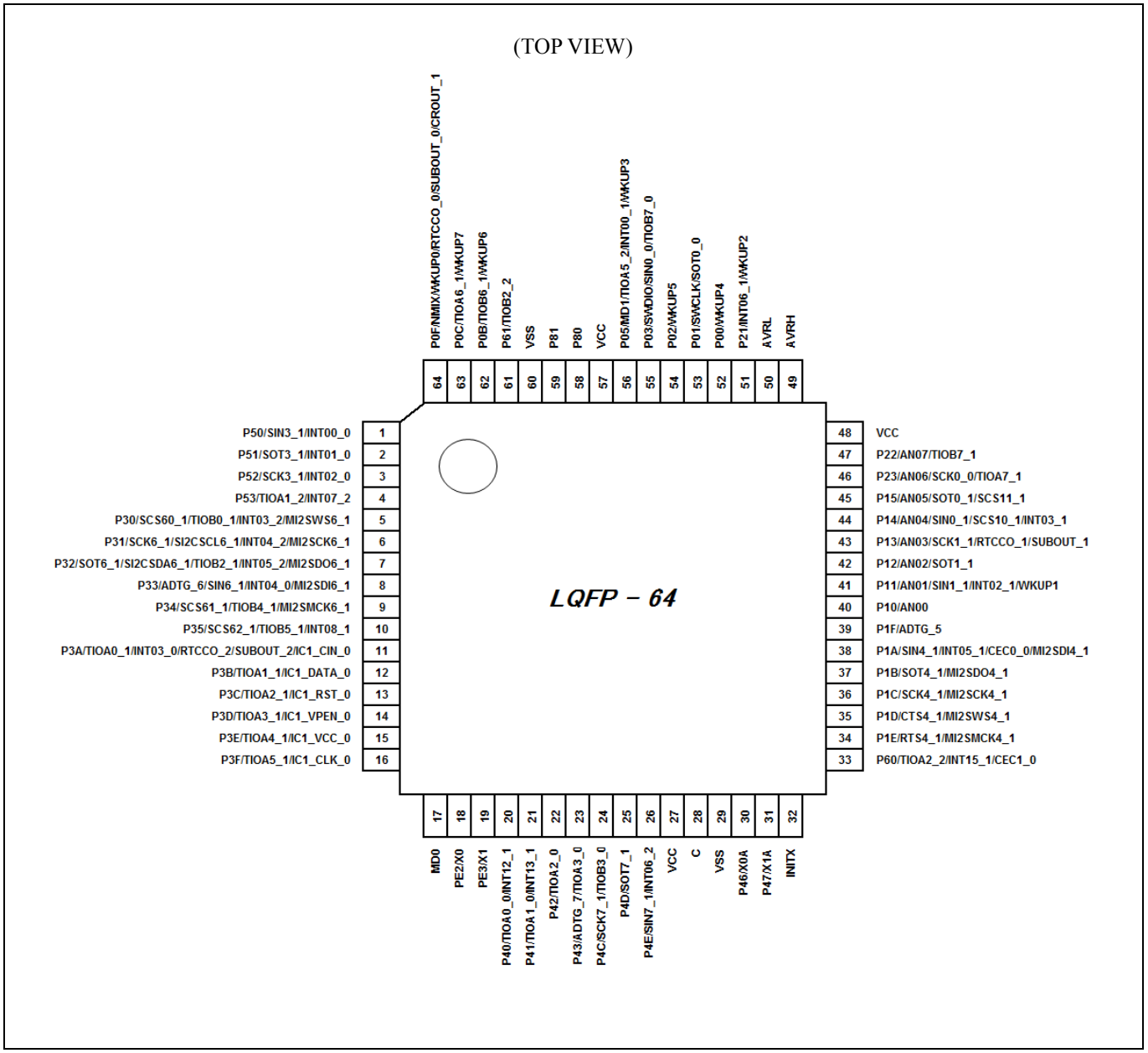
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	CSIO, I²C, LINbus, SmartCard, UART/USART
Peripherals	I²S, LVD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 6x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e1c12b0agp20000

3. Pin Assignment

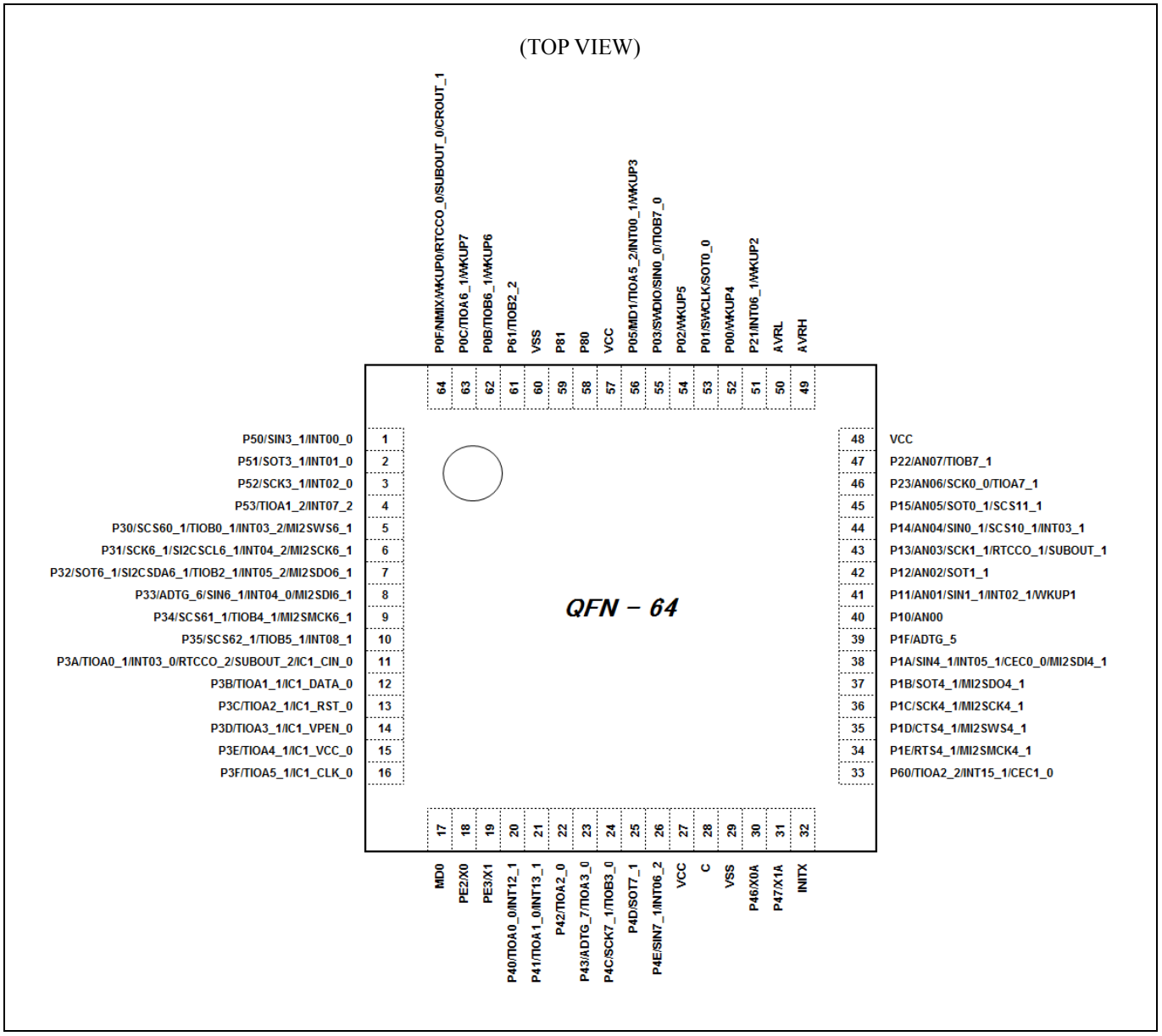
FPT-64P-M38



Note:

- *The number after the underscore ("_") in a pin name such as XXX_1 and XXX_2 indicates the relocated port number. The channel on such pin has multiple functions, each of which has its own pin name. Use the Extended Port Function Register (EPFR) to select the pin to be used.*

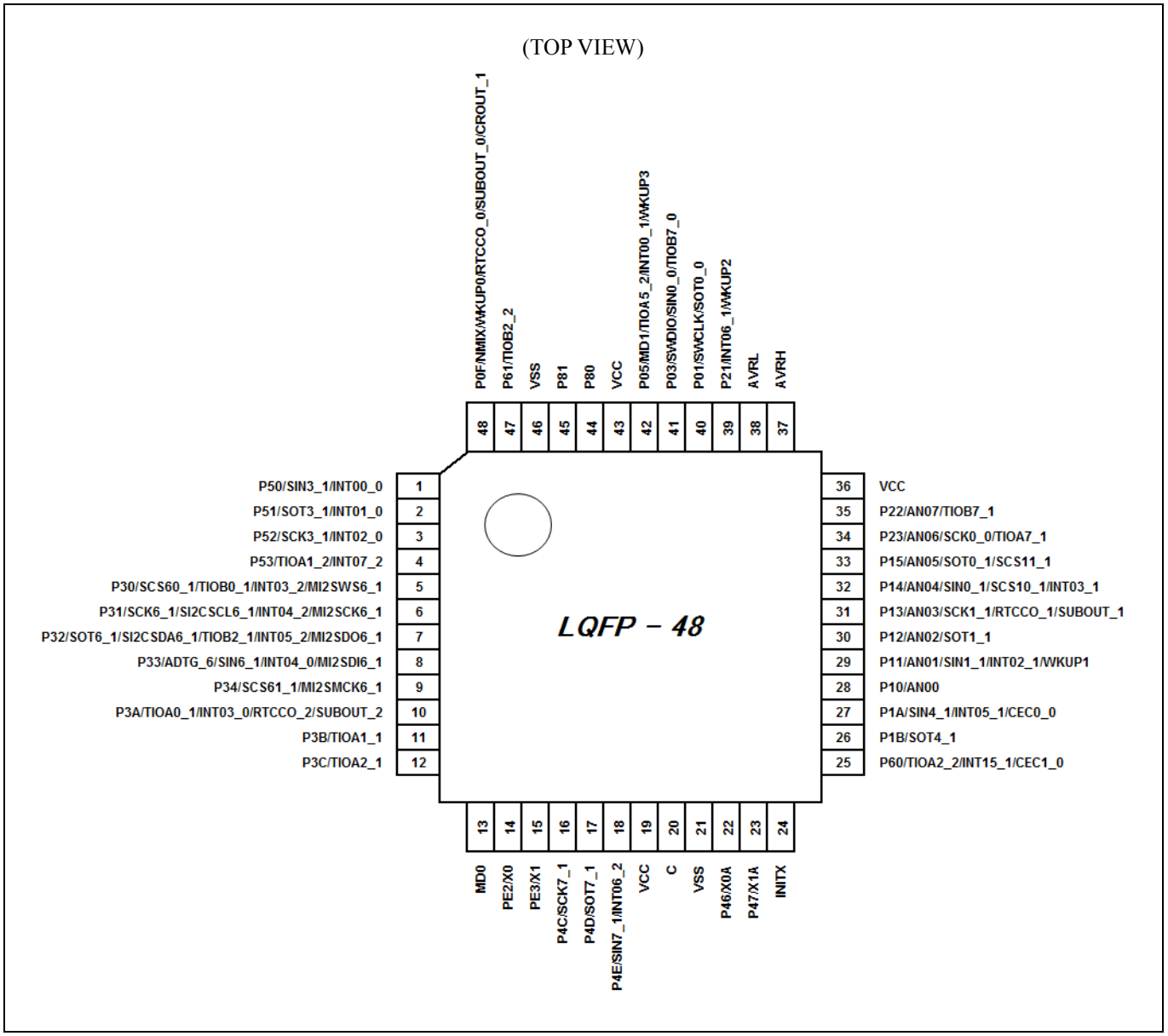
LCC-64P-M25



Note:

- *The number after the underscore ("_") in a pin name such as XXX_1 and XXX_2 indicates the relocated port number. The channel on such pin has multiple functions, each of which has its own pin name. Use the Extended Port Function Register (EPFR) to select the pin to be used.*

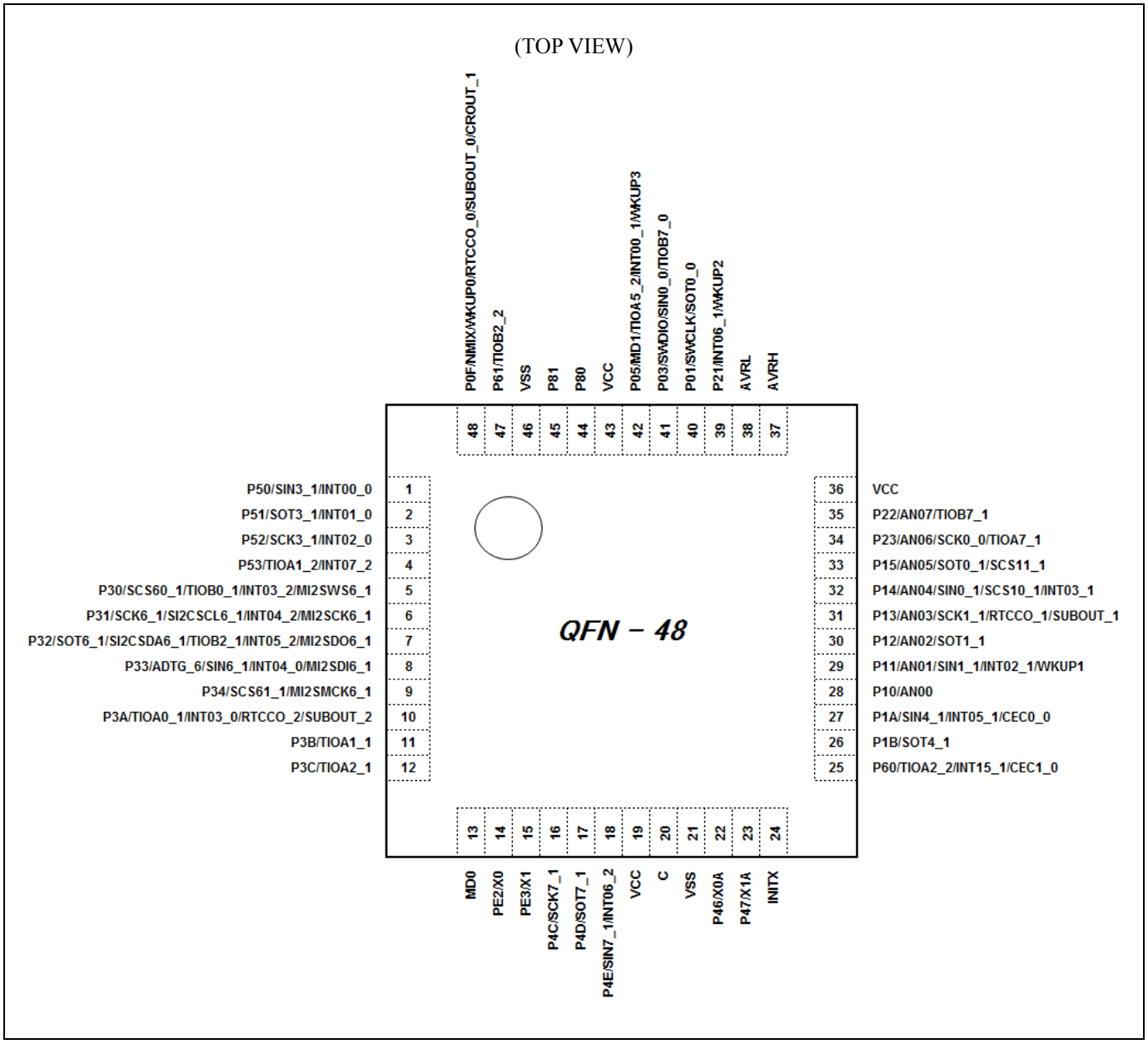
FPT-48P-M49



Note:

- *The number after the underscore ("_") in a pin name such as XXX_1 and XXX_2 indicates the relocated port number. The channel on such pin has multiple functions, each of which has its own pin name. Use the Extended Port Function Register (EPFR) to select the pin to be used.*

LCC-48P-M74

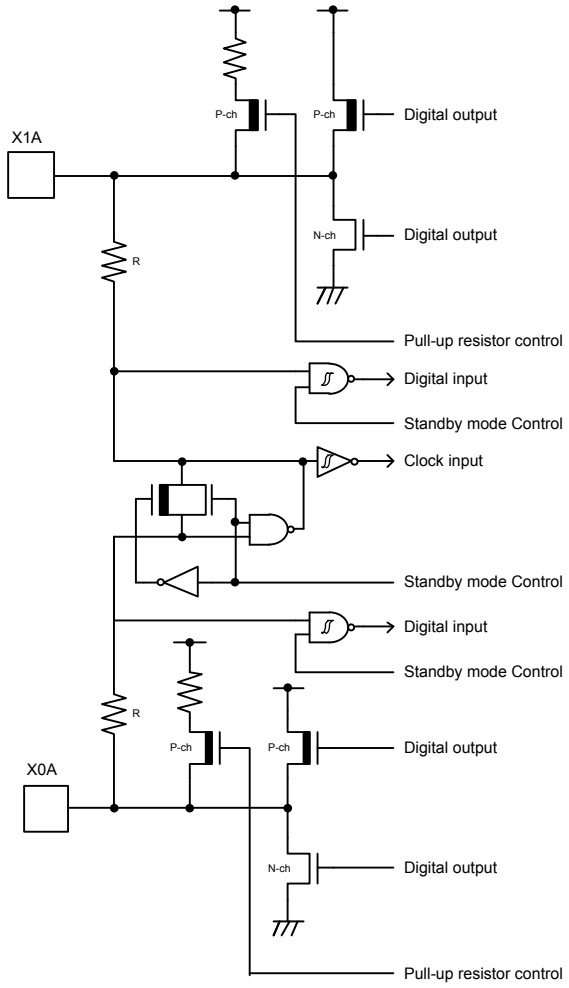


Note:

- *The number after the underscore ("_") in a pin name such as XXX_1 and XXX_2 indicates the relocated port number. The channel on such pin has multiple functions, each of which has its own pin name. Use the Extended Port Function Register (EPFR) to select the pin to be used.*

Pin no.			Pin Function	I/O circuit type	Pin state type
LQFP-64 QFN-64	LQFP-48 QFN-48	LQFP-32 QFN-32			
8	8	-	P33 ADTG_6 SIN6_1 INT04_0 MI2SDI6_1	H	K
-	-	7	P33 ADTG_6 SIN6_1 INT04_0	H	K
9	-	-	P34 SCS61_1 TIOB4_1 MI2SMCK6_1	D	K
-	9	-	P34 SCS61_1 MI2SMCK6_1	D	K
10	-	-	P35 SCS62_1 TIOB5_1 INT08_1	D	K
11	-	-	P3A TIOA0_1 INT03_0 RTCCO_2 SUBOUT_2 IC1_CIN_0	D	K
-	10	-	P3A TIOA0_1 INT03_0 RTCCO_2 SUBOUT_2	D	K
12	-	-	P3B TIOA1_1 IC1_DATA_0	D	K
-	11	-	P3B TIOA1_1	D	K
13	-	-	P3C TIOA2_1 IC1_RST_0	D	K
-	12	-	P3C TIOA2_1	D	K
14	-	-	P3D TIOA3_1 IC1_VPEN_0	D	K

Pin function	Pin name	Function description	Pin no.		
			LQFP-64 QFN-64	LQFP-48 QFN-48	LQFP-32 QFN-32
GPIO	P30	General-purpose I/O port 3	5	5	-
	P31		6	6	5
	P32		7	7	6
	P33		8	8	7
	P34		9	9	-
	P35		10	-	-
	P3A		11	10	-
	P3B		12	11	-
	P3C		13	12	-
	P3D		14	-	-
	P3E		15	-	-
	P3F		16	-	-
GPIO	P40	General-purpose I/O port 4	20	-	-
	P41		21	-	-
	P42		22	-	-
	P43		23	-	-
	P46		30	22	14
	P47		31	23	15
	P4C		24	16	-
	P4D		25	17	-
	P4E		26	18	-
GPIO	P50	General-purpose I/O port 5	1	1	2
	P51		2	2	3
	P52		3	3	4
	P53		4	4	-
GPIO	P60	General-purpose I/O port 6	33	25	17
	P61		61	47	-
GPIO	P80	General-purpose I/O port 8	58	44	30
	P81		59	45	31
GPIO	PE2	General-purpose I/O port E	18	14	9
	PE3		19	15	10
Multi-function Serial 0	SIN0_0	Multi-function serial interface ch.0 input pin	55	41	28
	SIN0_1		44	32	-
	SOT0_0 (SDA0_0)	Multi-function serial interface ch.0 output pin. This pin operates as SOT0 when used as a UART/CSIO/LIN pin (operation mode 0 to 3) and as SDA0 when used as an I2C pin (operation mode 4).	53	40	27
	SOT0_1 (SDA0_1)		45	33	-
	SCK0_0 (SCL0_0)	Multi-function serial interface ch.0 clock I/O pin. This pin operates as SCK0 when used as a CSIO pin (operation mode 2) and as SCL0 when used as an I2C pin (operation mode 4).	46	34	22

Type	Circuit	Remarks
C		It is possible to select the sub oscillation / GPIO function When the sub oscillation is selected. • Oscillation feedback resistor : Approximately 5MΩ • With Standby mode control When the GPIO is selected. • CMOS level output. • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 33kΩ I_{OH}= -4mA, I_{OL}= 4mA

Type
This indicates a pin status type that is shown in “pin list table” in “4. List of Pin Functions”

Selected Pin function
This indicates a pin function that is selected by user program.

CPU state
This indicates a state of the CPU that is shown below.

(1)	Reset state. CPU is initialized by Power-on reset or a reset due to low Power voltage supply.
(2)	Reset state. CPU is initialized by INITX input signal or system initialization after power on reset.
(3)	Run mode or SLEEP mode state.
(4)	Timer mode, RTC mode or STOP mode state. The standby pin level setting bit (SPL) in the Standby Mode Control Register (STB_CTL) is set to "0".
(5)	Timer mode, RTC mode or STOP mode state. The standby pin level setting bit (SPL) in the Standby Mode Control Register (STB_CTL) is set to "1".
(6)	Deep standby STOP mode or Deep standby RTC mode state, The standby pin level setting bit (SPL) in the Standby Mode Control Register (STB_CTL) is set to "0"
(7)	Deep standby STOP mode or Deep standby RTC mode state, The standby pin level setting bit (SPL) in the Standby Mode Control Register (STB_CTL) is set to "1"
(8)	Run mode state after returning from Deep Standby mode. (I/O state hold function(CONTX) is fixed at 1)

Each pin status
The meaning of the symbols in the pin status table is as follows.

IS	Digital output is disabled. (Hi-Z) Pull up register is off. Digital input is shut off by fixed 0.
IE	Digital output is disabled. (Hi-Z) Pull up register is off. Digital input is not shut off.
IP	Digital output is disabled. (Hi-Z) Pull up register is defined by the value of the PCR register. Digital input is not shut off.
IE/IS	Digital output is disabled. (Hi-Z) Pull up register is off. Digital input is shut off in case of the OSC stop. Digital input is not shut off in case of the OSC operation.
OE	The OSC is in operation state. However, it may be stopped in some operation mode of the CPU. For detail, see chapter “Low Power Consumption Mode” in peripheral manual.
OS	The OSC is in stop state. (Hi-Z)
PC	Digital output and pull up register is controlled by the register in the GPIO or peripheral function. Digital input is not shut off
CP	Digital output is controlled by the register in the GPIO or peripheral function. Pull up register is off. Digital input is not shut off.
HC	Digital output and pull up register is maintained the status that is immediately prior to entering the current CPU state. Digital input is not shut off
HS	Digital output and pull up register is maintained the status that is immediately prior to entering the current CPU state. Digital input is shut off
GS	Digital output and pull up register is copied the GPIO status that is immediately prior to entering the current CPU state and the status is maintained. Digital input is shut off

11.2 Recommended Operating Conditions

(V_{SS}= 0.0 V)

Parameter	Symbol	Conditions	Value		Unit	Remarks
			Min	Max		
Power supply voltage	V_{CC}	-	1.65 *2	3.6	V	
Analog reference voltage	AVRH	-	2.7	V_{CC}	V	V_{CC} ≥ 2.7 V
			V_{CC}	V_{CC}	V	V_{CC} < 2.7 V
	AVRL	-	VSS	VSS	V	
Smoothing capacitor	C_S	-	1	10	µF	For regulator*1
Operating temperature	Ta	-	- 40	+ 105	°C	

*1: See "C Pin" in "7. Handling Devices" for the connection of the smoothing capacitor.

*2: In between less than the minimum power supply voltage reset / interrupt detection voltage or more, instruction execution and low voltage detection function by built-in High-speed CR (including Main PLL is used) or built-in Low-speed CR is possible to operate only.

<WARNING>

1. *The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.*
2. *Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.*
3. *No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet.*
4. *Users considering application outside the listed conditions are advised to contact their representatives beforehand.*

11.4.6 Reset Input Characteristics

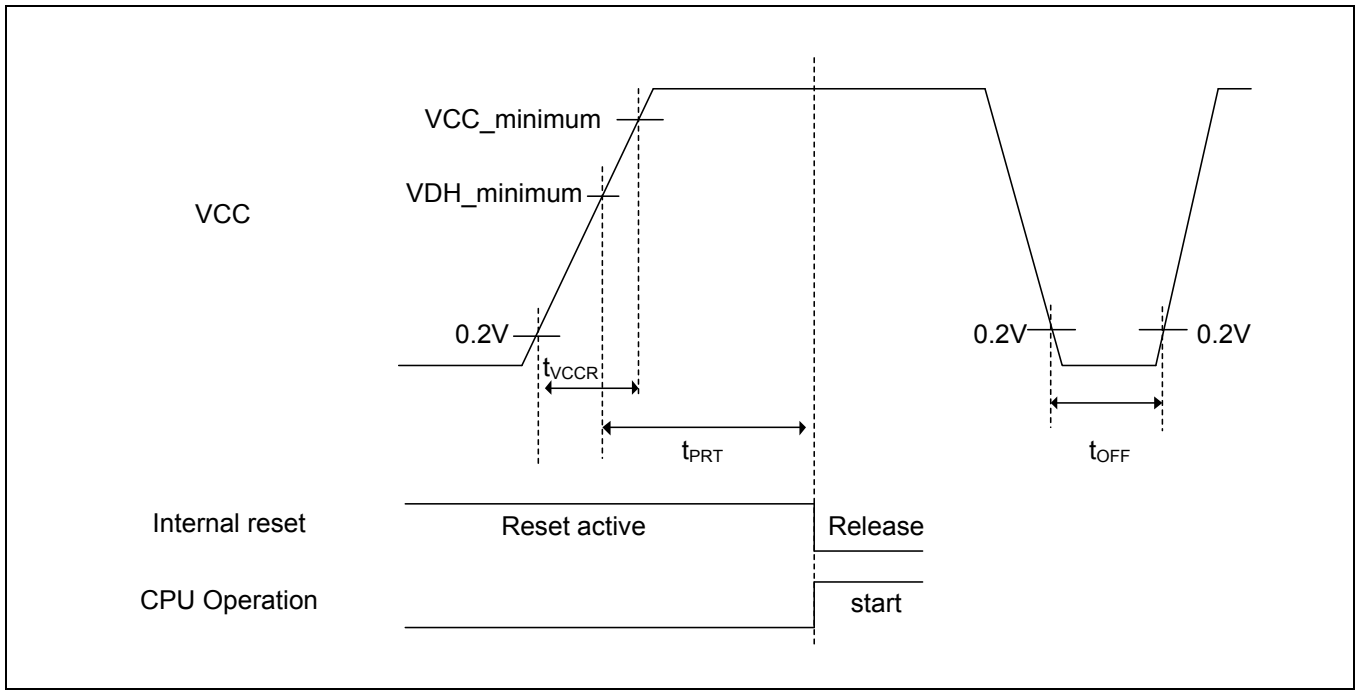
(V_{CC} = 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Reset input time	t_{INITX}	INITX	-	500	-	ns	

11.4.7 Power-on Reset Timing

(V_{CC}= 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Value		Unit	Remarks
			Min	Max		
Power supply rising time	t_{VCCR}	VCC	0	-	ms	
Power supply shut down time	t_{OFF}		1	-	ms	
Time until releasing Power-on reset	t_{PRT}		0.43	3.4	ms	



Glossary

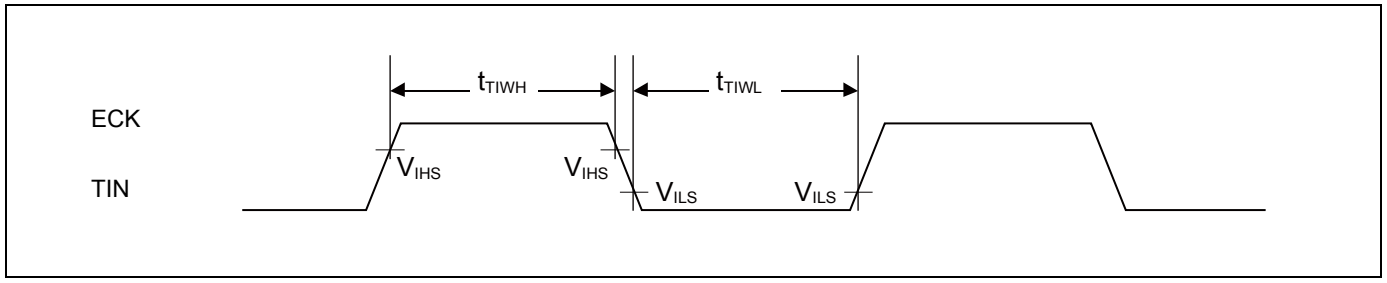
- VCC_minimum : Minimum V_{CC} of recommended operating conditions.
- VDH_minimum : Minimum detection voltage of Low-Voltage detection reset.
  See "11.6 Low-Voltage Detection Characteristics".

11.4.8 Base Timer Input Timing

Timer Input Timing

(V_{CC}= 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

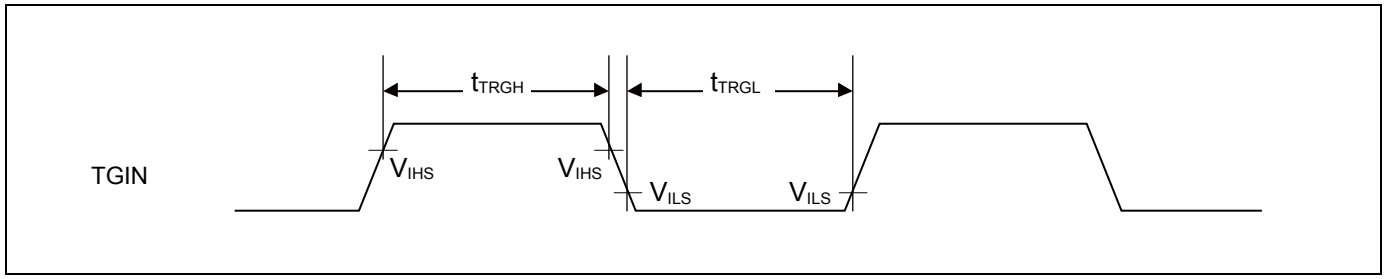
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH}, t_{TIWL}	TIOAn/TIOBn (when using as ECK, TIN)	-	2 t_{CYCP}	-	ns	



Trigger Input Timing

(V_{CC}= 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH}, t_{TRGL}	TIOAn/TIOBn (when using as TGIN)	-	2 t_{CYCP}	-	ns	



Note:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  For the number of the APB bus to which the Base Timer has been connected, see "8. Block Diagram".

11.4.9 CSIO/SPI/UART Timing

CSIO (SPI=0, SCINV=0)

(V_{CC}= 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin name	Conditions	V_{CC} < 2.7 V		V_{CC} ≥ 2.7 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	4 t_{CYCP}	-	4 t_{CYCP}	-	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↑ setup time	t_{IVSHI}	SCKx, SINx		50	-	36	-	ns
SCK ↑ → SIN hold time	t_{SHIXI}	SCKx, SINx		0	-	0	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	Slave mode	2 t_{CYCP} - 10	-	2 t_{CYCP} - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKx, SOTx		-	50	-	30	ns
SIN → SCK ↑ setup time	t_{IVSHE}	SCKx, SINx		10	-	10	-	ns
SCK ↑ → SIN hold time	t_{SHIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	tF	SCKx		-	5	-	5	ns
SCK rising time	tR	SCKx		-	5	-	5	ns

Notes:

- *The above AC characteristics are for clock synchronous mode.*
- *t_{CYCP} represents the APB bus clock cycle time.*
  For the number of the APB bus to which Multi-function Serial has been connected, see "8. Block Diagram".
- *The characteristics are only applicable when the relocate port numbers are the same.*
  For instance, they are not applicable for the combination of SCKx_0 and SOTx_1.
- *External load capacitance C_L=30 pF*

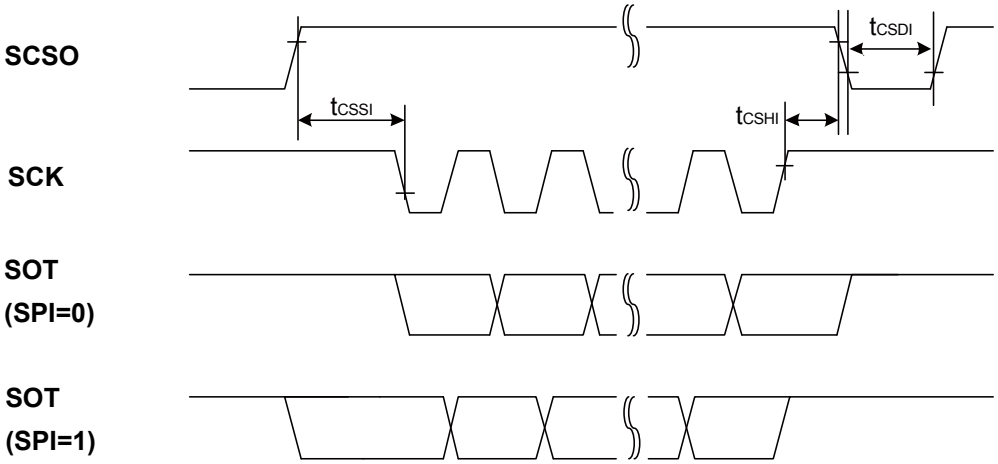
SPI (SPI=1, SCINV=1)

(V_{CC}= 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

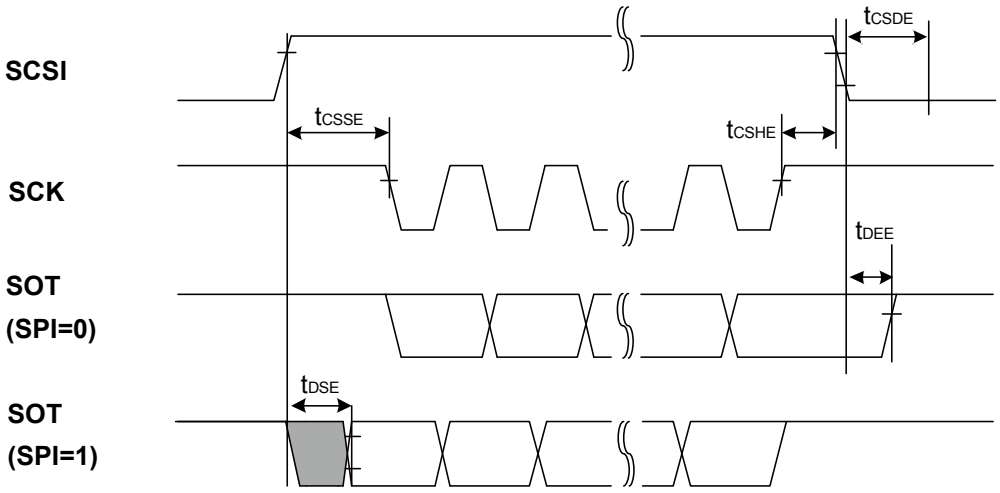
Parameter	Symbol	Pin name	Conditions	V_{CC} < 2.7 V		V_{CC} ≥ 2.7 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	4 t_{CYCP}	-	4 t_{CYCP}	-	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↑ setup time	t_{IVSHI}	SCKx, SINx		50	-	36	-	ns
SCK ↑ → SIN hold time	t_{SHIXI}	SCKx, SINx		0	-	0	-	ns
SOT → SCK ↑ delay time	t_{SOVHI}	SCKx, SOTx		2 t_{CYCP} - 30	-	2 t_{CYCP} - 30	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	Slave mode	2 t_{CYCP} - 10	-	2 t_{CYCP} - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKx, SOTx		-	50	-	33	ns
SIN → SCK ↑ setup time	t_{IVSHE}	SCKx, SINx		10	-	10	-	ns
SCK ↑ → SIN hold time	t_{SHIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	tF	SCKx		-	5	-	5	ns
SCK rising time	tR	SCKx		-	5	-	5	ns

Notes:

- *The above AC characteristics are for clock synchronous mode.*
- *t_{CYCP} represents the APB bus clock cycle time.*
  For the number of the APB bus to which Multi-function Serial has been connected, see "8. Block Diagram".
- *The characteristics are only applicable when the relocate port numbers are the same.*
  For instance, they are not applicable for the combination of SCKx_0 and SOTx_1.
- *External load capacitance C_L=30 pF*



Master mode



Slave mode

When Using CSIO/SPI Chip Select (SCINV=1, CSLVL=0)

(V_{CC}= 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Conditions	V_{CC} < 2.7 V		V_{CC} ≥ 2.7 V		Unit
			Min	Max	Min	Max	
SCS↑→SCK↑ setup time	t_{CSSI}	Master mode	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK↓→SCS↓ hold time	t_{CSHI}		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t_{CSDI}		(*3)-50	(*3)+50	(*3)-50	(*3)+50	ns
SCS↑→SCK↑ setup time	t_{CSSE}	Slave mode	$3t_{CYCP}$+30	-	$3t_{CYCP}$+30	-	ns
SCK↓→SCS↓ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		$3t_{CYCP}$+30	-	$3t_{CYCP}$+30	-	ns
SCS↑→SOT delay time	t_{DSE}		-	55	-	40	ns
SCS↓→SOT delay time	t_{DEE}		0	-	0	-	ns

*1: CSSU bit value × serial chip select timing operating clock cycle.

*2: CSHD bit value × serial chip select timing operating clock cycle.

*3: CSDS bit value × serial chip select timing operating clock cycle.
Irrespective of CSDS bit setting, $5t_{CYCP}$ or more are required for the period the time when the serial chip select pin becomes inactive to the time when the serial chip select pin becomes active again.

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  For information about the APB bus number which Multi-function Serial is connected to, see "8. Block Diagram".
- *For information about CSSU, CSHD, CSDS, serial chip select timing operating clock, see "FM0+ Family Peripheral Manual".*
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCKx_0 and SCSIx_1 is not guaranteed.
- *When the external load capacitance C_L=30 pF.*

11.6.2 Low-Voltage Detection Interrupt

(T_A=-40°C to +105°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	SVHI=00100	1.56	1.70	1.84	V	When voltage drops
Released voltage	VDH		1.61	1.75	1.89	V	When voltage rises
Detected voltage	VDL	SVHI=00101	1.61	1.75	1.89	V	When voltage drops
Released voltage	VDH		1.66	1.80	1.94	V	When voltage rises
Detected voltage	VDL	SVHI=00110	1.66	1.80	1.94	V	When voltage drops
Released voltage	VDH		1.70	1.85	2.00	V	When voltage rises
Detected voltage	VDL	SVHI=00111	1.70	1.85	2.00	V	When voltage drops
Released voltage	VDH		1.75	1.90	2.05	V	When voltage rises
Detected voltage	VDL	SVHI=01000	1.75	1.90	2.05	V	When voltage drops
Released voltage	VDH		1.79	1.95	2.11	V	When voltage rises
Detected voltage	VDL	SVHI=01001	1.79	1.95	2.11	V	When voltage drops
Released voltage	VDH		1.84	2.00	2.16	V	When voltage rises
Detected voltage	VDL	SVHI=01010	1.84	2.00	2.16	V	When voltage drops
Released voltage	VDH		1.89	2.05	2.21	V	When voltage rises
Detected voltage	VDL	SVHI=01011	1.89	2.05	2.21	V	When voltage drops
Released voltage	VDH		1.93	2.10	2.27	V	When voltage rises
Detected voltage	VDL	SVHI=01100	2.30	2.50	2.70	V	When voltage drops
Released voltage	VDH		2.39	2.60	2.81	V	When voltage rises
Detected voltage	VDL	SVHI=01101	2.39	2.60	2.81	V	When voltage drops
Released voltage	VDH		2.48	2.70	2.92	V	When voltage rises
Detected voltage	VDL	SVHI=01110	2.48	2.70	2.92	V	When voltage drops
Released voltage	VDH		2.58	2.80	3.02	V	When voltage rises
Detected voltage	VDL	SVHI=01111	2.58	2.80	3.02	V	When voltage drops
Released voltage	VDH		2.67	2.90	3.13	V	When voltage rises
Detected voltage	VDL	SVHI=10000	2.67	2.90	3.13	V	When voltage drops
Released voltage	VDH		2.76	3.00	3.24	V	When voltage rises
Detected voltage	VDL	SVHI=10001	2.76	3.00	3.24	V	When voltage drops
Released voltage	VDH		2.85	3.10	3.35	V	When voltage rises
Detected voltage	VDL	SVHI=10010	2.85	3.10	3.35	V	When voltage drops
Released voltage	VDH		2.94	3.20	3.46	V	When voltage rises
Detected voltage	VDL	SVHI=10011	2.94	3.20	3.46	V	When voltage drops
Released voltage	VDH		3.04	3.30	3.56	V	When voltage rises
LVD stabilization wait time	T_{LVDW}	-	-	-	8160 × t_{CYCP}*	µs	
LVD detection delay time	T_{LVDDL}	-	-	-	200	µs	

*: t_{CYCP} represents the APB1 bus clock cycle time.

11.7 Flash Memory Write/Erase Characteristics

(V_{CC}=1.65 V to 3.6 V, T_A=- 40°C to +105°C)

Parameter		Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	Large sector	-	1.1	2.7	s	The sector erase time includes the time of writing prior to internal erase.
	Small sector	-	0.3	0.9		
Halfword (16-bit) write time		-	30	528	µs	The halfword (16-bit) write time excludes the system-level overhead.
Chip erase time		-	4.5	11.7	s	The chip erase time includes the time of writing prior to internal erase.

*: The typical value is immediately after shipment, the maximum value is guarantee value under 10,000 cycle of erase/write.

Write/Erase Cycle and Data Hold Time

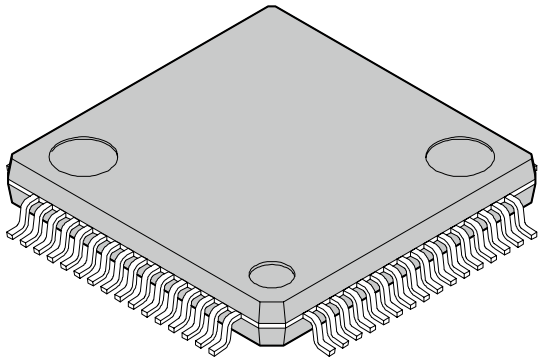
Write/Erase Cycle	Data Hold Time (Year)	Remarks
1,000	20*	
10,000	10*	

*: This value comes from the technology qualification (using Arrhenius equation to translate high temperature acceleration test result into average temperature value at + 85°C).

12. Ordering Information

Part number	On-chip Flash memory [Kbyte]	On-Chip SRAM [Kbyte]	Package	Packing
S6E1C12D0AGV20000	128	16	Plastic • LQFP (0.50 mm pitch), 64 pins (FPT-64P-M38)	Tray
S6E1C11D0AGV20000	64	12		
S6E1C12C0AGV20000	128	16	Plastic • LQFP (0.50 mm pitch), 48 pins (FPT-48P-M49)	Tray
S6E1C11C0AGV20000	64	12		
S6E1C12B0AGP20000	128	16	Plastic • LQFP (0.80 mm pitch), 32 pins (FPT-32P-M30)	Tray
S6E1C11B0AGP20000	64	12		
S6E1C12D0AGN20000	128	16	Plastic • QFN64 (0.50 mm pitch), 64 pins (LCC-64P-M25)	Tray
S6E1C11D0AGN20000	64	12		
S6E1C12C0AGN20000	128	16	Plastic • QFN48 (0.50 mm pitch), 48 pins (LCC-48P-M74)	Tray
S6E1C11C0AGN20000	64	12		
S6E1C12B0AGN20000	128	16	Plastic • QFN32 (0.50 mm pitch), 32 pins (LCC-32P-M73)	Tray
S6E1C11B0AGN20000	64	12		

64-pin plastic LQFP

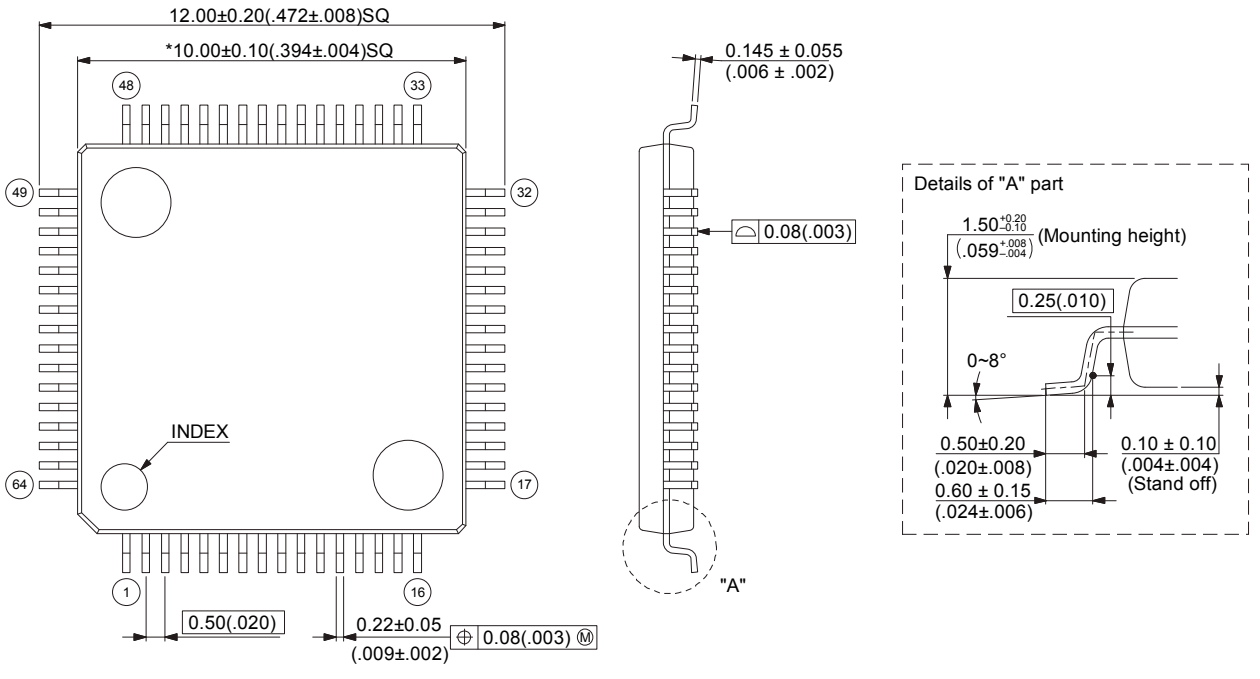


(FPT-64P-M38)

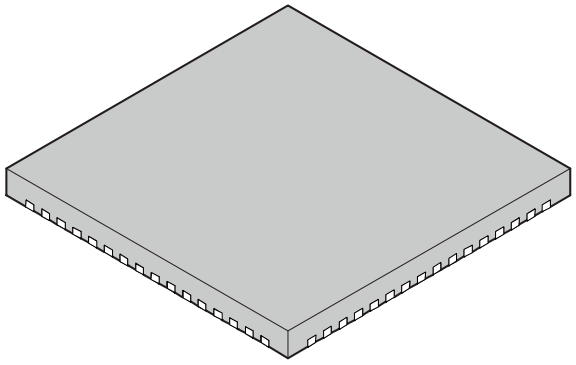
Lead pitch	0.50 mm
Package width × package length	10.00 mm × 10.00 mm
Lead shape	Gullwing
Lead bend direction	Normal bend
Sealing method	Plastic mold
Mounting height	1.70 mm MAX
Weight	0.32 g

64-pin plastic LQFP
(FPT-64P-M38)

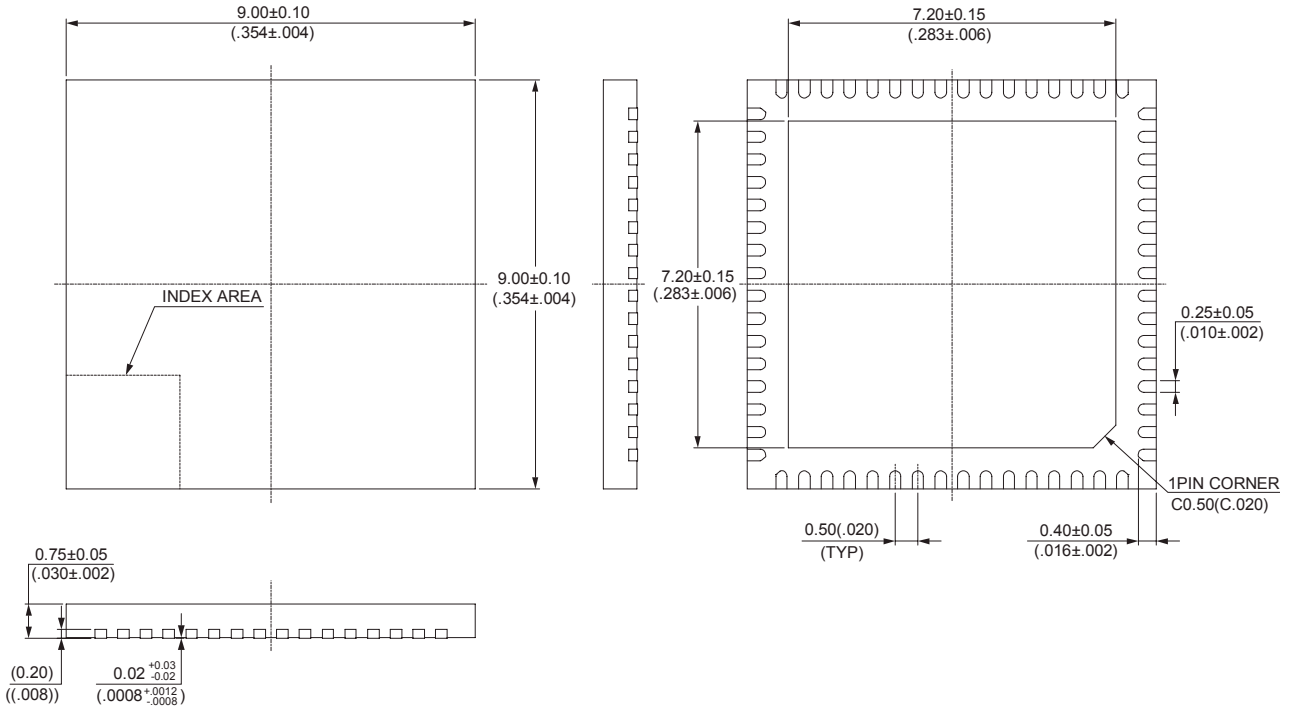
Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

64-pin plastic QFN		
	Lead pitch	0.50 mm
	Package width × package length	9.00 mm × 9.00 mm
	Sealing method	Plastic mold
	Mounting height	0.80 mm MAX
	Weight	0.21 g
(LCC-64P-M25)		

64-pin plastic QFN
(LCC-64P-M25)



Dimensions in mm (inches).
Note: The values in parentheses are reference values.