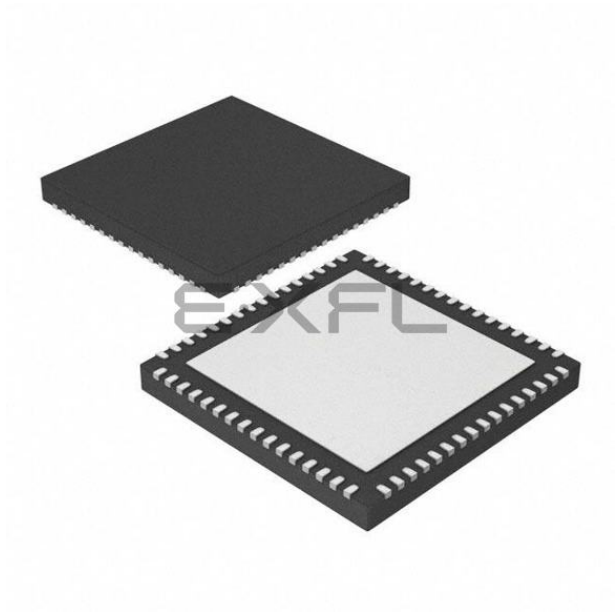

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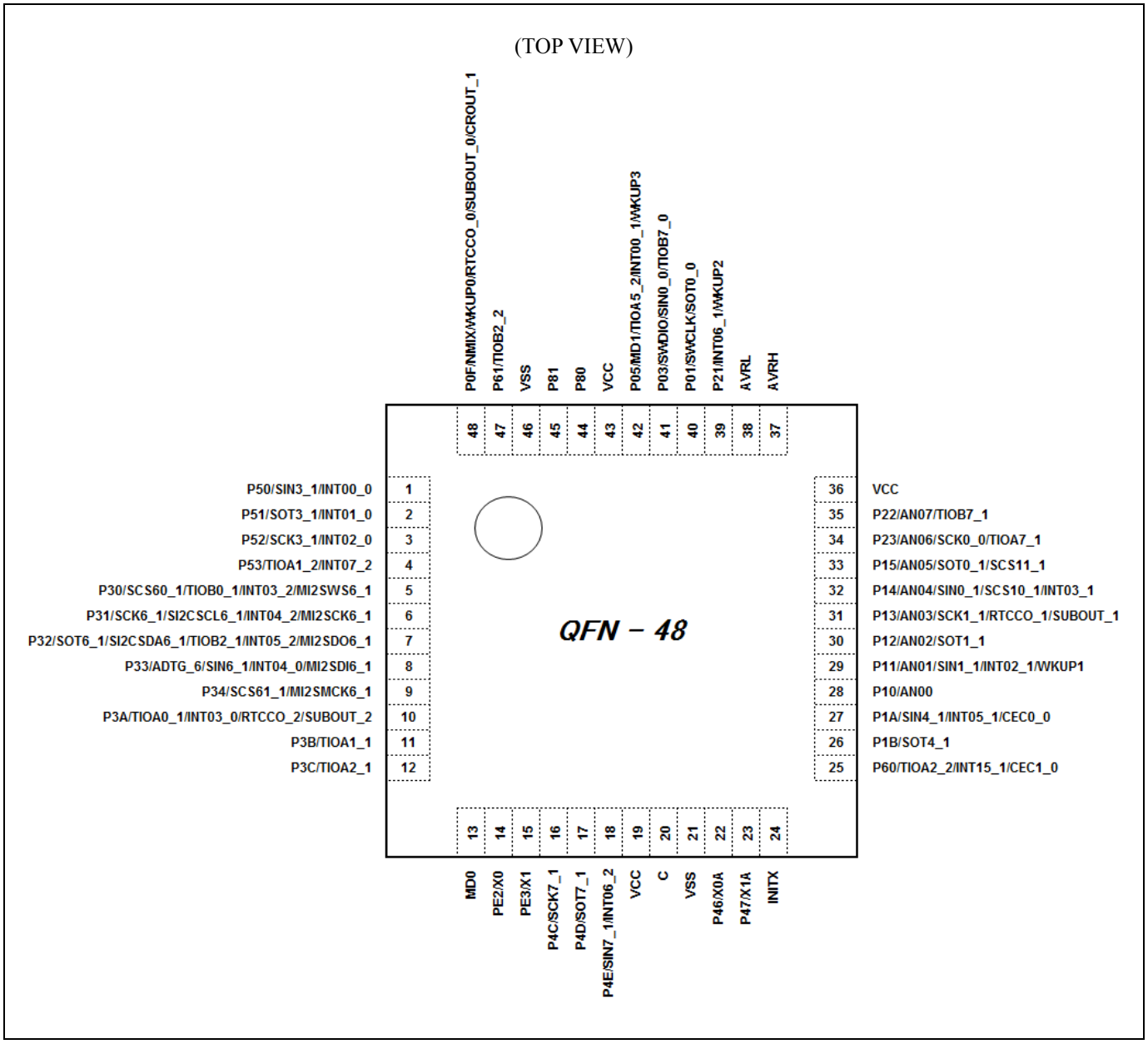
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	CSIO, I²C, LINbus, SmartCard, UART/USART
Peripherals	I²S, LVD, POR, PWM, WDT
Number of I/O	54
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-WFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e1c12d0agn20000

LCC-48P-M74



Note:

- *The number after the underscore ("_") in a pin name such as XXX_1 and XXX_2 indicates the relocated port number. The channel on such pin has multiple functions, each of which has its own pin name. Use the Extended Port Function Register (EPFR) to select the pin to be used.*

4. List of Pin Functions

List of Pin Numbers

The number after the underscore ("_") in a pin name such as XXX_1 and XXX_2 indicates the relocated port number. The channel on such pin has multiple functions, each of which has its own pin name. Use the Extended Port Function Register (EPFR) to select the pin to be used.

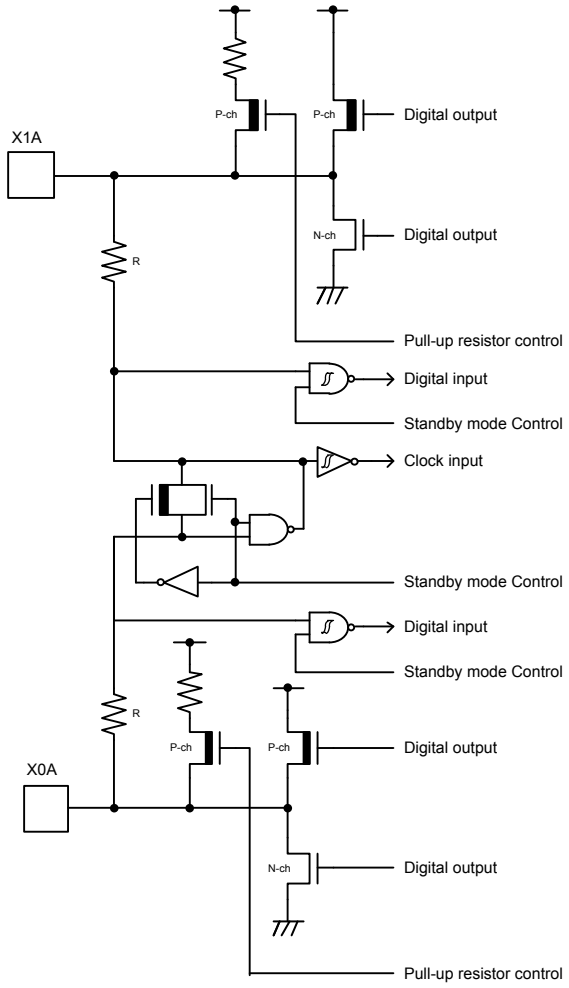
Pin no.			Pin Function	I/O circuit type	Pin state type
LQFP-64 QFN-64	LQFP-48 QFN-48	LQFP-32 QFN-32			
1	1	2	P50	D	K
			SIN3_1		
			INT00_0		
2	2	3	P51	D	K
			SOT3_1		
			INT01_0		
3	3	4	P52	D	K
			SCK3_1		
			INT02_0		
4	4	-	P53	D	K
			TIOA1_2		
			INT07_2		
5	5	-	P30	D	K
			SCS60_1		
			TIOB0_1		
			INT03_2		
			MI2SWS6_1		
6	6	-	P31	H	K
			SCK6_1		
			SI2CSCL6_1		
			INT04_2		
			MI2SCK6_1		
-	-	5	P31	H	K
			SCK6_1		
			SI2CSCL6_1		
			INT04_2		
7	7	-	P32	H	K
			SOT6_1		
			SI2CSDA6_1		
			TIOB2_1		
			INT05_2		
			MI2SDO6_1		
-	-	6	P32	H	K
			SOT6_1		
			SI2CSDA6_1		
			TIOB2_1		
			INT05_2		

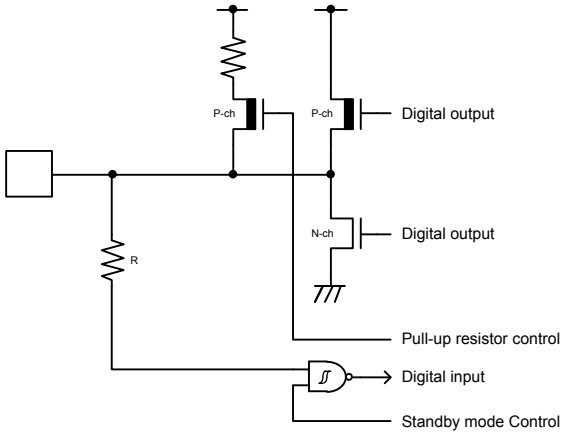
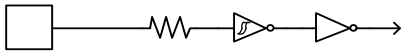
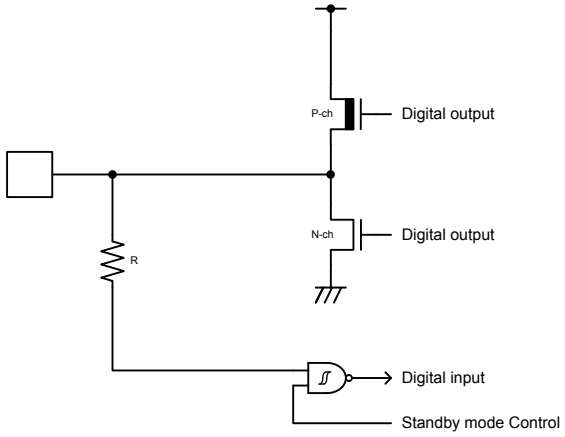
Pin no.			Pin Function	I/O circuit type	Pin state type
LQFP-64 QFN-64	LQFP-48 QFN-48	LQFP-32 QFN-32			
45	33	-	P15	F	J
			AN05		
			SOT0_1		
			SCS11_1		
46	34	22	P23	F	J
			AN06		
			SCK0_0		
			TIOA7_1		
47	35	23	P22	F	J
			AN07		
			TIOB7_1		
48	36	24	VCC	-	-
49	37	-	AVRH *	-	-
50	38	25	AVRL	-	-
51	39	26	P21	E	K
			INT06_1		
			WKUP2		
52	-	-	P00	E	K
			WKUP4		
53	40	27	P01	D	K
			SWCLK		
			SOT0_0		
54	-	-	P02	E	K
			WKUP5		
55	41	28	P03	D	K
			SWDIO		
			SIN0_0		
			TIOB7_0		
56	42	29	P05	E	K
			MD1		
			TIOA5_2		
			INT00_1		
			WKUP3		
57	43	-	VCC	-	-
58	44	30	P80	J	G
59	45	31	P81	J	G
60	46	32	VSS	-	-
61	47	-	P61	H	K
			TIOB2_2		
62	-	-	P0B	E	K
			TIOB6_1		
			WKUP6		
63	-	-	P0C	E	K
			TIOA6_1		
			WKUP7		

Pin function	Pin name	Function description	Pin no.		
			LQFP-64 QFN-64	LQFP-48 QFN-48	LQFP-32 QFN-32
I2S(MFS)	MI2SDI4_1	I2S Serial Data Input pin (operation mode 2).	38	-	-
	MI2SDO4_1	I2S Serial Data Output pin (operation mode 2).	37	-	-
	MI2SCK4_1	I2S Serial Clock Output pin (operation mode 2).	36	-	-
	MI2SWS4_1	I2S Word Select Output pin (operation mode 2).	35	-	-
	MI2SMCK4_1	I2S Master Clock Input/output pin (operation mode 2).	34	-	-
	MI2SDI6_1	I2S Serial Data Input pin (operation mode 2).	8	8	-
	MI2SDO6_1	I2S Serial Data Output pin (operation mode 2).	7	7	-
	MI2SCK6_1	I2S Serial Clock Output pin (operation mode 2).	6	6	-
	MI2SWS6_1	I2S Word Select Output pin (operation mode 2).	5	5	-
	MI2SMCK6_1	I2S Master Clock Input/output pin (operation mode 2).	9	9	-
Smart Card Interface	IC1_CIN_0	Smart Card insert detection output pin	11	-	-
	IC1_CLK_0	Smart Card serial interface clock output pin	16	-	-
	IC1_DATA_0	Smart Card serial interface data input pin	12	-	-
	IC1_RST_0	Smart Card reset output pin	13	-	-
	IC1_VCC_0	Smart Card power enable output pin	15	-	-
	IC1_VPEN_0	Smart Card programming output pin	14	-	-
Real-time Clock	RTCCO_0	0.5 seconds pulse output pin of real-time clock	64	48	1
	RTCCO_1		43	31	21
	RTCCO_2		11	10	-
	SUBOUT_0	Sub clock output pin	64	48	1
	SUBOUT_1		43	31	21
	SUBOUT_2		11	10	-
HDMI-CEC/Remote Control Reception	CEC0_0	HDMI-CEC/Remote Control Reception ch.0 input/output pin	38	27	-
	CEC1_0	HDMI-CEC/Remote Control Reception ch.1 input/output pin	33	25	17

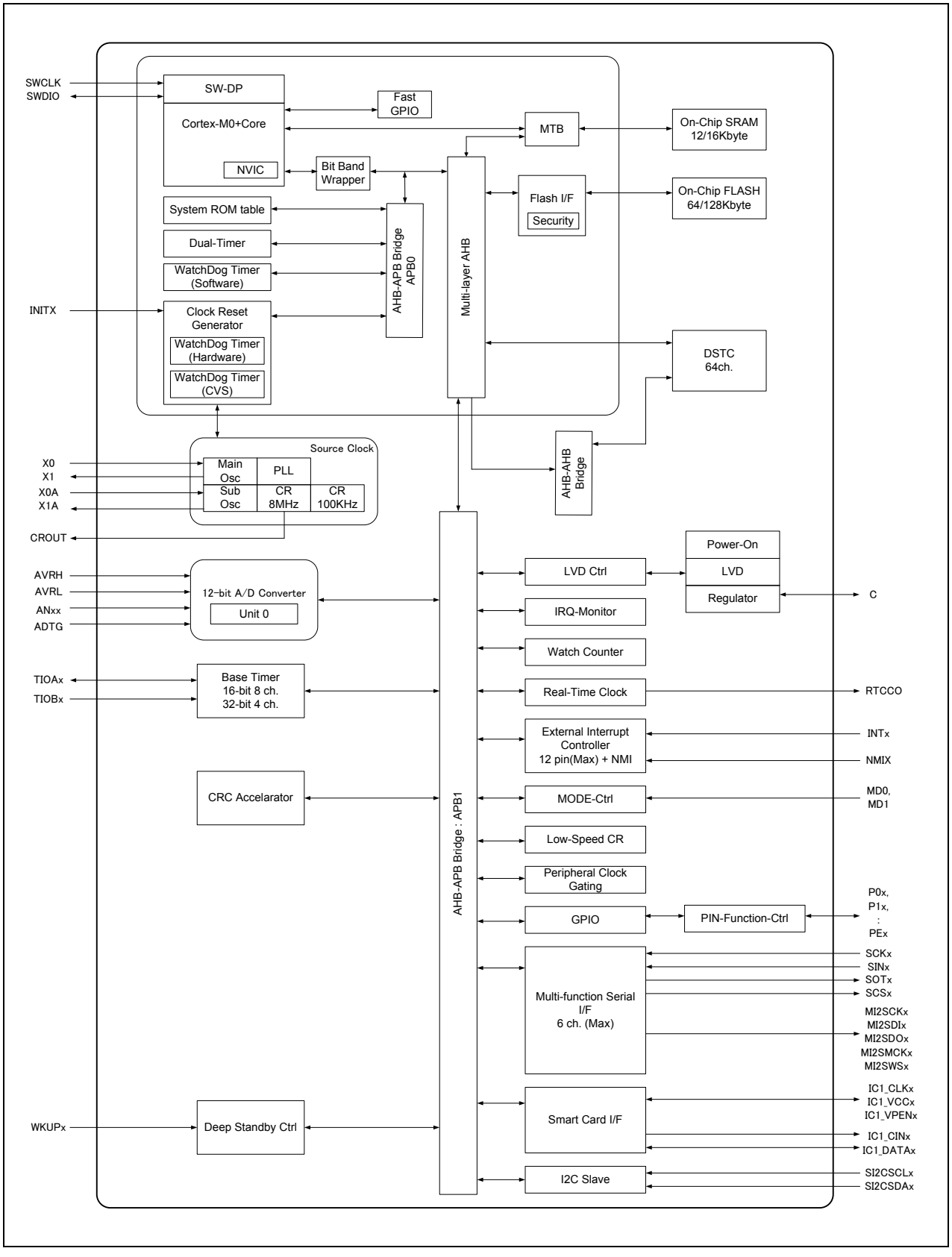
Pin function	Pin name	Function description	Pin no.		
			LQFP-64 QFN-64	LQFP-48 QFN-48	LQFP-32 QFN-32
Low Power Consumption Mode	WKUP0	Deep Standby mode return signal input pin 0	64	48	1
	WKUP1	Deep Standby mode return signal input pin 1	41	29	19
	WKUP2	Deep Standby mode return signal input pin 2	51	39	26
	WKUP3	Deep Standby mode return signal input pin 3	56	42	29
	WKUP4	Deep Standby mode return signal input pin 4	52	-	-
	WKUP5	Deep Standby mode return signal input pin 5	54	-	-
	WKUP6	Deep Standby mode return signal input pin 6	62	-	-
	WKUP7	Deep Standby mode return signal input pin 7	63	-	-
I2C Slave	SI2CSCL6_1	I2C Clock Pin	6	6	5
	SI2CSDA6_1	I2C Data Pin	7	7	6
RESET	INITX	External Reset Input pin. A reset is valid when INITX="L".	32	24	16
MODE	MD0	Mode 0 pin. During normal operation, input MD0="L". During serial programming to Flash memory, input MD0="H".	17	13	8
	MD1	Mode 1 pin. During normal operation, input is not needed. During serial programming to Flash memory, MD1 = "L" must be input.	56	42	29
CLOCK	X0	Main clock (oscillation) input pin	18	14	9
	X0A	Sub clock (oscillation) input pin	30	22	14
	X1	Main clock (oscillation) I/O pin	19	15	10
	X1A	Sub clock (oscillation) I/O pin	31	23	15
	CROUT_1	Built-in high-speed CR oscillation clock output port	64	48	1
POWER	VCC	Power supply pin	27	19	11
	VCC		48	36	24
	VCC		57	43	-
GND	VSS	GND pin	29	21	13
	VSS		60	46	32
Analog Reference	AVRH *	A/D converter analog reference voltage input pin	49	37	-
	AVRL	A/D converter analog reference voltage input pin	50	38	25
C pin	C	Power supply stabilization capacitance pin	28	20	12

*: In case of 32-pin package, AVRH pin is internally connected to VCC pin.

Type	Circuit	Remarks
C		It is possible to select the sub oscillation / GPIO function When the sub oscillation is selected. • Oscillation feedback resistor : Approximately 5MΩ • With Standby mode control When the GPIO is selected. • CMOS level output. • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 33kΩ I_{OH}= -4mA, I_{OL}= 4mA

Type	Circuit	Remarks
H		・CMOS level output ・CMOS level hysteresis input ・5V tolerant ・With pull-up resistor control ・With standby mode control ・Pull-up resistor : Approximately 33kΩ ・IOH= -4mA, IOL= 4mA ・Available to control PZR registers ・When this pin is used as an I2C pin, the digital output P-ch transistor is always off
I		・CMOS level hysteresis input
J		・CMOS level output ・CMOS level hysteresis input ・With standby mode control

8. Block Diagram



10. Pin Status in Each CPU State

The following table shows pin status in each CPU state.

Type	Selected Pin function		CPU state							
			(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)
A	Main osillation circuit selected *1	Main osillation circuit selected	OS	OS	OE	OE	OE	OS	OS	OS
	Digital I/O slected *2	Main clock external input selected	-	-	IE/IS	IE/IS	IE/IS	IS	IS	IS
		GPIO selected	-	-	PC	HC	IS	HS	IS	HS
B	Main osillation circuit selected *1	Main osillation circuit selected	OS	OS	OE	OE	OE	OS	OS	OS
	Digital I/O slected *2	GPIO selected	-	-	PC	HC	IS	GS	IS	GS
C	Sub osillation circuit selected *1	Sub osillation circuit selected	OS	OE	OE	OE	OE	OE	OE	OE
	Digital I/O slected *2	Sub clock external input selected	-	-	IE/IS	IE/IS	IE/IS	IS	IS	IS
		GPIO selected	-	-	PC	HC	IS	HS	IS	HS
D	Sub osillation circuit selected *1	Sub osillation circuit selected	OS	OE	OE	OE	OE	OE	OE	OE
	Digital I/O slected *2	GPIO selected	-	-	PC	HC	IS	HS	IS	HS
E	Digital I/O slected	INITX input	This pin is digital input pin, pull up register is on, and digital input is not shut off in all CPU state..							
F	Digital I/O slected	MD0 input	This pin is digital input pin, pull up register is none, digital input is not shut off in all CPU state..							
G	Digital I/O slected *6	GPIO selected	IS	IE	CP	HC	IS	HS	IS	HS
H	Digital I/O slected	SW selected	IS	IP *5	PC	IP	IP	IP	IP	IP
		GPIO selected	-	-	PC	HC	IS	HS	IS	HS
I	Digital I/O slected	NMI selected	-	-	IP	IP	IP	-	-	-
		WKUP0 enable and input selected	-	-	IP	IP	IP	IP	IP	IP
		GPIO selected	IS	IE	PC	HC	IS	-	-	-
J	Analog input selected *3	Analog input selected	Analog input is enalbe in all CPU state							
	Digital I/O slected *4	WKUP enable and input selected	-	-	IP	IP	IP	IP	IP	IP
		Exterrnal interrupt enable and input selected	-	-	IP	IP	IP	GS	IS	GS
		GPIO selected	-	-	PC	HC	IS	HS	IS	HS
		Resource other than above selected	-	-	PC	HC	IS	GS	IS	GS
K	Digital I/O slected	CEC pin selected	-	-	CP	CP	CP	CP	CP	CP
		WKUP enable and input selected	-	-	IP	IP	IP	IP	IP	IP
		I2CSLAVE enable selected	-	-	PC	HC	IP	GS	IS	GS
		Exterrnal interrupt enable and input selected	-	-	PC	HC	IP	GS	IS	GS
		GPIO selected	IS	IE	PC	HC	IS	HS	IS	HS
		Resource other than above selected	-	-	PC	HC	IS	GS	IS	GS

Each term in above table have the following meanings.

11.3 DC Characteristics

11.3.1 Current Rating

Symbol (Pin Name)	Conditions		HCLK Frequency*4	Value Typ*1	Value Max*2	Unit	Remarks
Icc (VCC)	Run mode, code executed from Flash	8 MHz external clock input, PLL ON*8 NOP code executed Built-in high speed CR stopped	8 MHZ	1.4	2.7	mA	*3
			20 MHZ	2.6	4.1		
			40 MHZ	3.9	5.6		
		8 MHz external clock input, PLL ON*8 Benchmark code executed Built-in high speed CR stopped	8 MHZ	1.3	2.6	mA	*3
			20 MHZ	2.3	3.8		
			40 MHZ	3.4	5.1		
		8 MHz crystal oscillation, PLL ON*8 NOP code executed Built-in high speed CR stopped	8 MHZ	1.6	3.0	mA	*3
			20 MHZ	2.8	4.4		
			40 MHZ	4.1	5.9		
	Run mode, code executed from RAM	8 MHz external clock input, PLL ON*8 NOP code executed Built-in high speed CR stopped	8 MHZ	1.0	2.1	mA	*3
			20 MHZ	1.7	2.9		
			40 MHZ	2.7	4.0		
	Run mode, code executed from Flash	8 MHz external clock input, PLL ON NOP code executed Built-in high speed CR stopped PCLK1 stopped	40 MHZ	1.6	3.1	mA	*3,*6,*7
	Run mode, code executed from Flash	Built-in high speed CR*5 NOP code executed All peripheral clock stopped by CKENx	8 MHZ	1.1	2.4	mA	*3
		32 kHz crystal oscillation NOP code executed All peripheral clock stopped by CKENx	32 kHZ	240	1264	µA	*3
		Built-in low speed CR NOP code executed All peripheral clock stopped by CKENx	100 kHZ	246	1271	µA	*3
Iccs (VCC)	Sleep operation	8 MHz external clock input, PLL ON*8 All peripheral clock stopped by CKENx	8 MHZ	0.8	1.9	mA	*3
			20 MHZ	1.3	2.4		
			40 MHZ	1.8	3.0		
		Built-in high speed CR*5 All peripheral clock stopped by CKENx	8 MHZ	0.6	1.7	mA	*3
		32 kHz crystal oscillation All peripheral clock stopped by CKENx	32 kHZ	237	1261	µA	*3
		Built-in low speed CR All peripheral clock stopped by CKENx	100 kHZ	238	1262	µA	*3

*1 : T_A=+25°C,V_{CC}=3.3 V
*2 : T_A=+105°C,V_{CC}=3.6 V
*3 : All ports are fixed
*4 : PCLK0 is set to divided rate 8
*5 : The frequency is set to 8 MHz by trimming
*6 : Flash sync down is set to FRWTR.RWT=111 and FSYNDN.SD=1111
*7 : VCC=1.65 V
*8 : When HCLK=8 MHz, PLL OFF

Parameter	Symbol (Pin Name)	Conditions		Value		Unit	Remarks
				Typ	Max		
Power supply current	I_{CCH} (VCC)	Stop mode	Ta=25°C Vcc=3.3 V	12.4	52.4	µA	*1, *2
			Ta=25°C Vcc=1.65 V	12.0	52.0	µA	*1, *2
			Ta=105°C Vcc=3.6 V	-	597	µA	*1, *2
	I_{CCT} (VCC)	Sub timer mode	Ta=25°C Vcc=3.3 V 32 kHz Crystal oscillation	15.6	55.6	µA	*1, *2
			Ta=25°C Vcc=1.65 V 32 kHz Crystal oscillation	15.0	55.0	µA	*1, *2
			Ta=105°C Vcc=3.6 V 32 kHz Crystal oscillation	-	601	µA	*1, *2
	I_{CCR} (VCC)	RTC mode	Ta=25°C Vcc=3.3 V 32 kHz Crystal oscillation	13.2	53.2	µA	*1, *2
			Ta=25°C Vcc=1.65 V 32 kHz Crystal oscillation	12.7	52.7	µA	*1, *2
			Ta=105°C Vcc=3.6 V 32 kHz Crystal oscillation	-	598	µA	*1, *2

*1: All ports are fixed. LVD off. Flash off.

*2: When CALDONE bit(CAL_CTL:CALDONE) is “1”. In case of “0”, Bipolar Vref current is added.

Peripheral Current Dissipation

(V_{CC}=1.65 V to 3.6 V, V_{SS}=0 V, T_A=- 40°C to +105°C)

Clock System	Peripheral	Conditions	Frequency (MHz)			Unit	Remarks
			8	20	40		
HCLK	GPIO	At all ports operation	0.05	0.12	0.23	mA	
	DSTC	At 2ch operation	0.02	0.06	0.10		
PCLK1	Base timer	At 4ch operation	0.02	0.05	0.10	mA	
	ADC	At 1 unit operation	0.04	0.10	0.21		
	Multi-function serial	At 1ch operation	0.01	0.03	0.06		
	MFS-I2S	At 1ch operation	0.02	0.05	0.08		
	Smart Card I/F	At 1ch operation	0.04	0.08	0.18		

11.4.4 Operating Conditions of Main PLL (In the Case of Using the Main Clock as the Input Clock of the PLL)

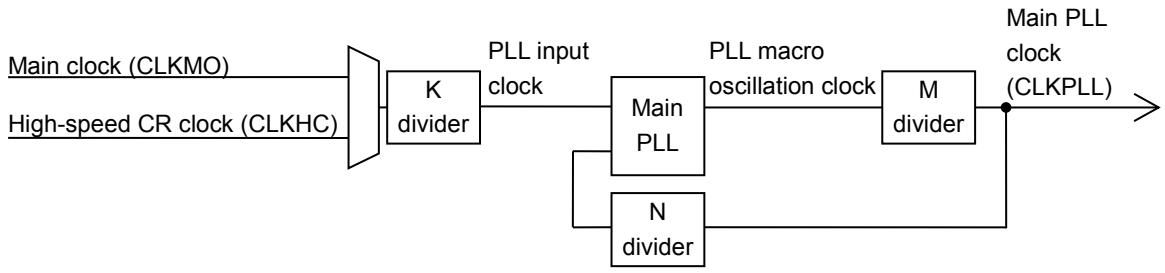
(V_{CC}= 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (LOCK UP time)	t_{LOCK}	50	-	-	µs	
PLL input clock frequency	F_{PLLI}	8	-	16	MHz	
PLL multiple rate	-	5	-	18	multiple	
PLL macro oscillation clock frequency	F_{PLLO}	75	-	150	MHz	
Main PLL clock frequency*2	F_{CLKPLL}	-	-	40	MHz	

*1: The wait time is the time it takes for PLL oscillation to stabilize.

*2: For details of the main PLL clock (CLKPLL), refer to "Chapter: Clock" in "FM0+ Family Peripheral Manual".

Main PLL connection



11.4.5 Operating Conditions of Main PLL (In the Case of Using the Built-in High-Speed CR Clock as the Input Clock of the Main PLL)

(V_{CC}= 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (LOCK UP time)	t_{LOCK}	50	-	-	µs	
PLL input clock frequency	F_{PLLI}	7.84	8	8.16	MHz	
PLL multiple rate	-	9	-	18	multiple	
PLL macro oscillation clock frequency	F_{PLLO}	75	-	150	MHz	
Main PLL clock frequency*2	F_{CLKPLL}	-	-	40.8	MHz	

*1: The wait time is the time it takes for PLL oscillation to stabilize.

*2: For details of the main PLL clock (CLKPLL), refer to "Chapter: Clock" in "FM0+ Family Peripheral Manual".

Note:

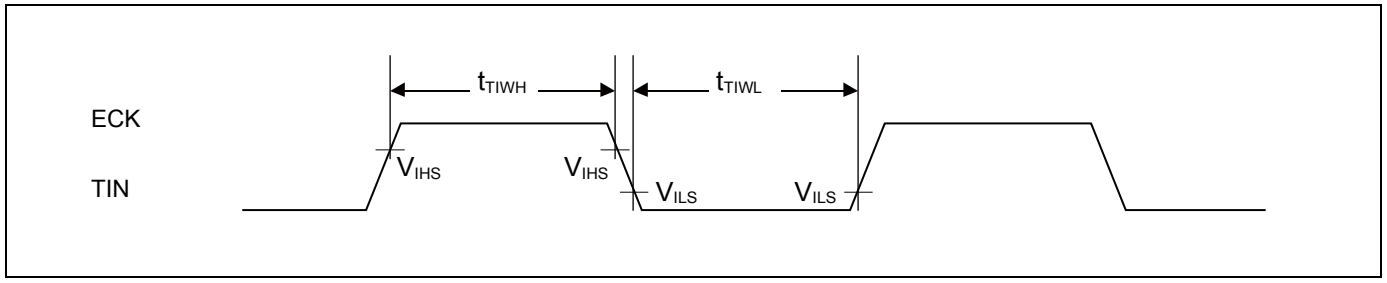
- *For the main PLL source clock, input the high-speed CR clock (CLKHC) whose frequency and temperature have been trimmed. When setting PLL multiple rate, please take the accuracy of the built-in High-speed CR clock into account and prevent the master clock from exceeding the maximum frequency.*

11.4.8 Base Timer Input Timing

Timer Input Timing

(V_{CC}= 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

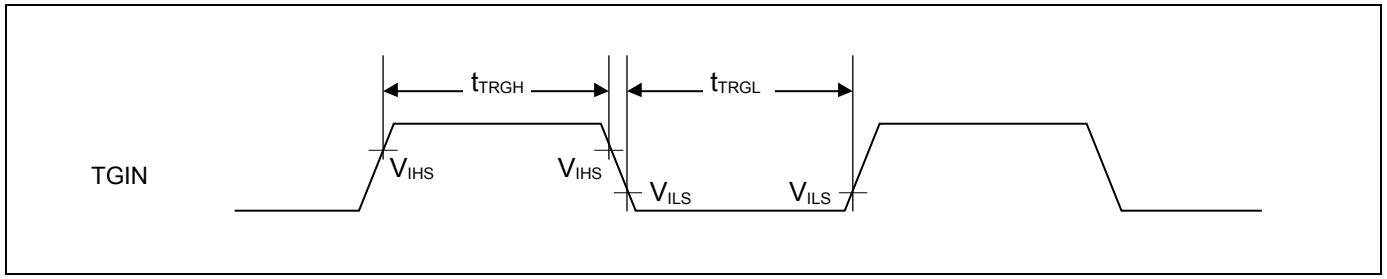
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH}, t_{TIWL}	TIOAn/TIOBn (when using as ECK, TIN)	-	2 t_{CYCP}	-	ns	



Trigger Input Timing

(V_{CC}= 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH}, t_{TRGL}	TIOAn/TIOBn (when using as TGIN)	-	2 t_{CYCP}	-	ns	



Note:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  For the number of the APB bus to which the Base Timer has been connected, see "8. Block Diagram".

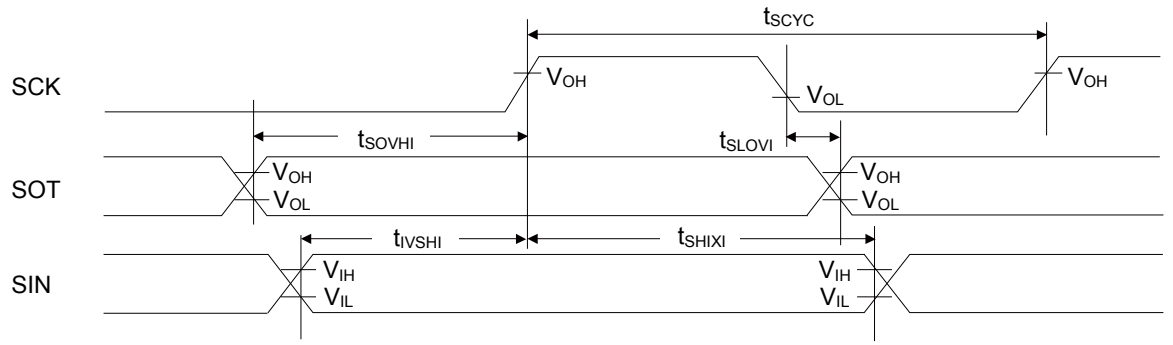
CSIO (SPI=0, SCINV=1)

(V_{CC}= 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

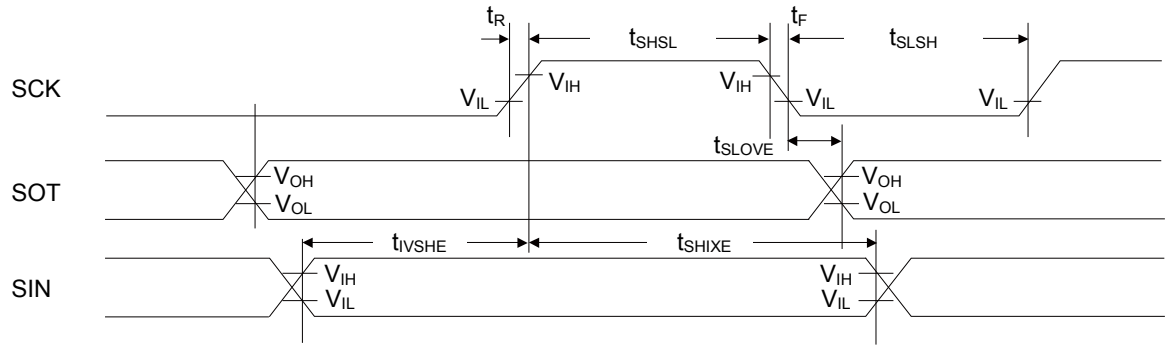
Parameter	Symbol	Pin name	Conditions	V_{CC} < 2.7V		V_{CC} ≥ 2.7V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	4 t_{CYCP}	-	4 t_{CYCP}	-	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↓ setup time	t_{IVSLI}	SCKx, SINx		50	-	36	-	ns
SCK ↓ → SIN hold time	t_{SLIXI}	SCKx, SINx		0	-	0	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	Slave mode	2 t_{CYCP} - 10	-	2 t_{CYCP} - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCKx, SOTx		-	50	-	33	ns
SIN → SCK ↓ setup time	t_{IVSLE}	SCKx, SINx		10	-	10	-	ns
SCK ↓ → SIN hold time	t_{SLIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	tF	SCKx		-	5	-	5	ns
SCK rising time	tR	SCKx		-	5	-	5	ns

Notes:

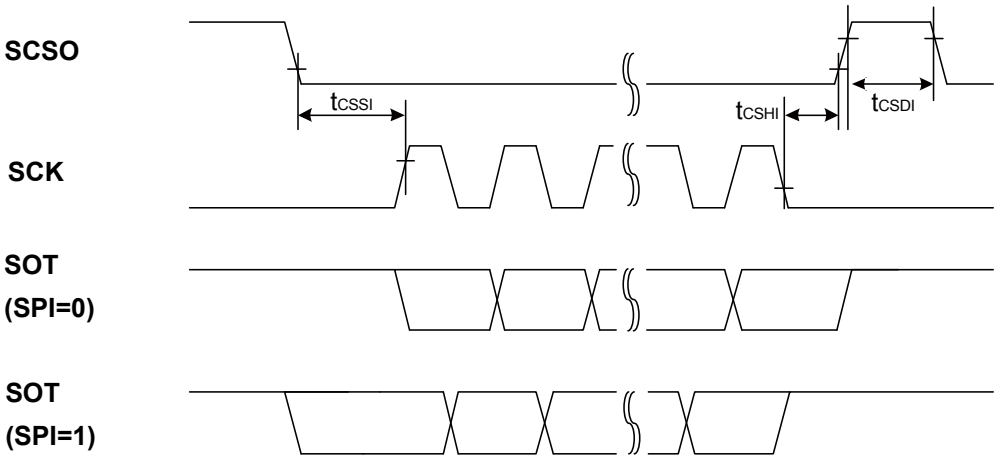
- *The above AC characteristics are for clock synchronous mode.*
- *t_{CYCP} represents the APB bus clock cycle time.*
  For the number of the APB bus to which Multi-function Serial has been connected, see "8. Block Diagram".
- *The characteristics are only applicable when the relocate port numbers are the same.*
  For instance, they are not applicable for the combination of SCKx_0 and SOTx_1.
- *External load capacitance C_L=30 pF*



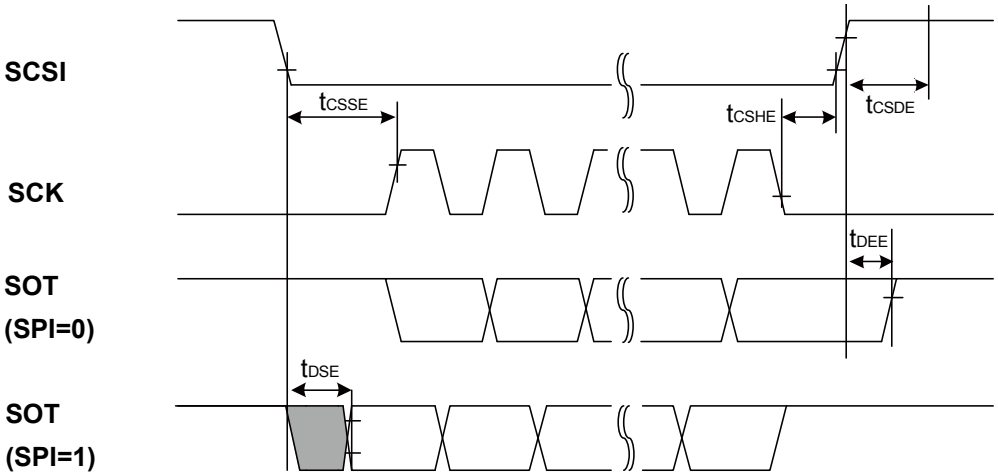
Master mode



Slave mode



Master mode



Slave mode

When Using CSIO/SPI Chip Select (SCINV=0, CSLVL=0)

(V_{CC}= 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Conditions	V_{CC} < 2.7 V		V_{CC} ≥ 2.7 V		Unit
			Min	Max	Min	Max	
SCS↑→SCK↓ setup time	t_{CSSI}	Master mode	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK↑→SCS↓ hold time	t_{CSHI}		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t_{CSDI}		(*3)-50	(*3)+50	(*3)-50	(*3)+50	ns
SCS↑→SCK↓ setup time	t_{CSSE}	Slave mode	$3t_{CYCP}$+30	-	$3t_{CYCP}$+30	-	ns
SCK↑→SCS↓ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		$3t_{CYCP}$+30	-	$3t_{CYCP}$+30	-	ns
SCS↑→SOT delay time	t_{DSE}		-	55	-	40	ns
SCS↓→SOT delay time	t_{DEE}		0	-	0	-	ns

*1: CSSU bit value × serial chip select timing operating clock cycle.

*2: CSHD bit value × serial chip select timing operating clock cycle.

*3: CSDS bit value × serial chip select timing operating clock cycle.
Irrespective of CSDS bit setting, $5t_{CYCP}$ or more are required for the period the time when the serial chip select pin becomes inactive to the time when the serial chip select pin becomes active again.

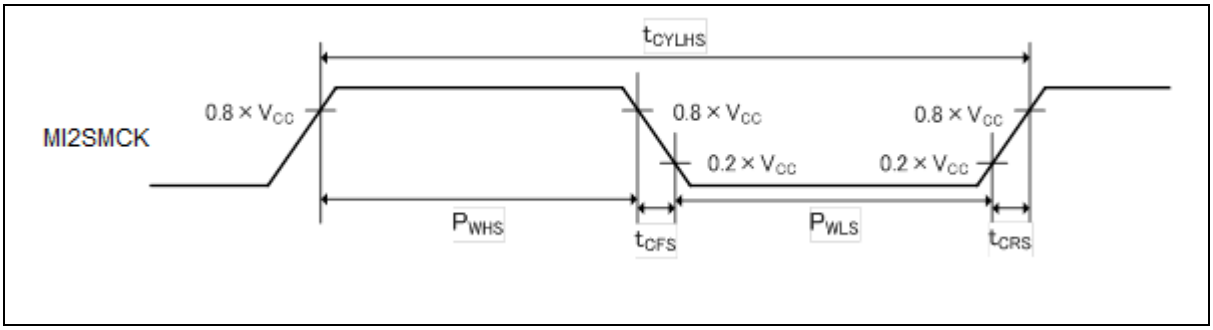
Notes:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  For information about the APB bus number which Multi-function Serial is connected to, see "8. Block Diagram".
- *For information About CSSU, CSHD, CSDS, serial chip select timing operating clock, see "FM0+ Family Peripheral Manual".*
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCKx_0 and SCSIx_1 is not guaranteed.
- *When the external load capacitance C_L=30 pF.*

MI2SMCK Input Characteristics

(V_{CC}= 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	f_{CHS}	MI2SMCK	-	-	12.288	MHz	
Input clock cycle	t_{CYLHS}	-	-	81.3	-	ns	
Input clock pulse width	-	-	P_{WHS}/t_{CYLHS} P_{WLS}/t_{CYLHS}	45	55	%	When using external clock
Input clock rise time and fall time	t_{CFS} t_{CRS}	-	-	-	5	ns	When using external clock

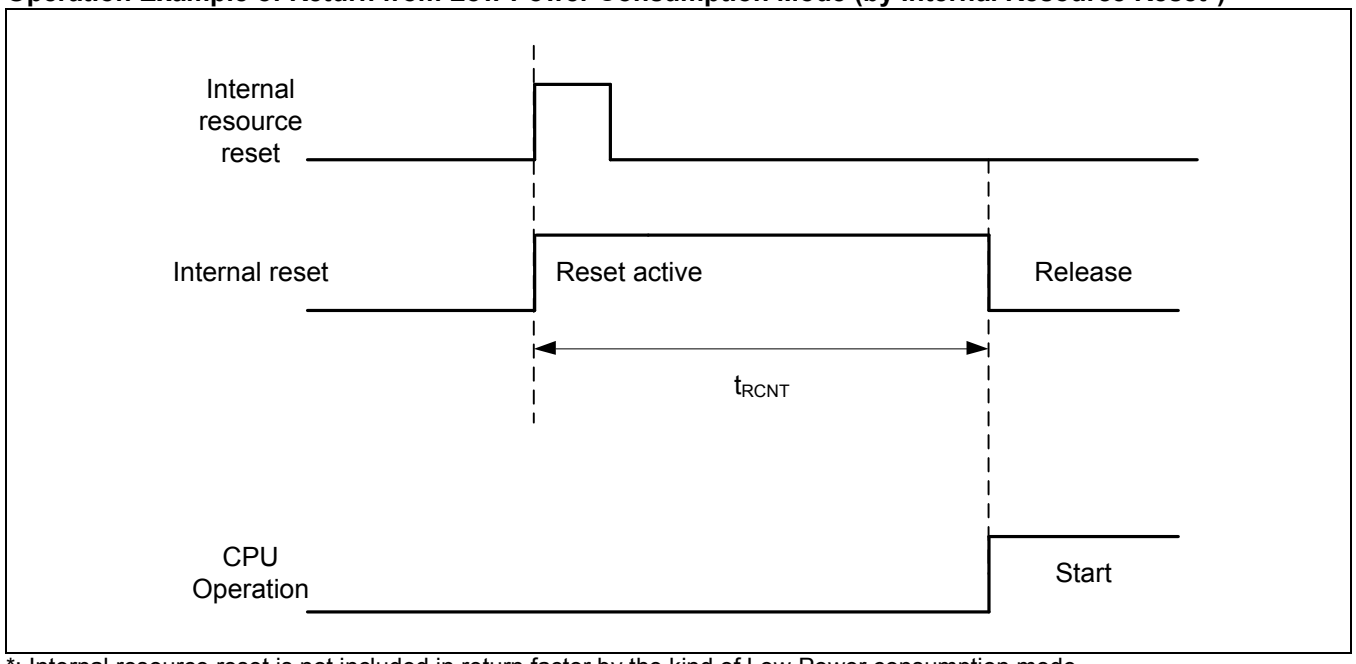


MI2SMCK Output Characteristics

(V_{CC}= 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Output frequency	f_{CHS}	MI2SMCK	-	-	25	MHz	$V_{CC} \geq 2.7$ V
				-	20	MHz	$V_{CC} < 2.7$ V

Operation Example of Return from Low Power Consumption Mode (by Internal Resource Reset*)



*: Internal resource reset is not included in return factor by the kind of Low-Power consumption mode.

Notes:

- *The return factor is different in each Low-Power consumption modes.*
  See "Chapter: Low Power Consumption Mode" and "Operations of Standby Modes" in FM0+ Family Peripheral Manual.
- *When interrupt recoveries, the operation mode that CPU recoveries depends on the state before the Low-Power consumption mode transition. See "Chapter: Low Power Consumption Mode" in "FM0+ Family Peripheral Manual".*
- *The time during the power-on reset/low-voltage detection reset is excluded. See "11.4.7 Power-on Reset Timing in 11.4 AC Characteristics in 11. Electrical Characteristics" for the detail on the time during the power-on reset/low -voltage detection reset.*
- *When in recovery from reset, CPU changes to the high-speed CR run mode. When using the main clock or the PLL clock, it is necessary to add the main clock oscillation stabilization wait time or the main PLL clock stabilization wait time.*
- *The internal resource reset means the watchdog reset and the CSV reset.*