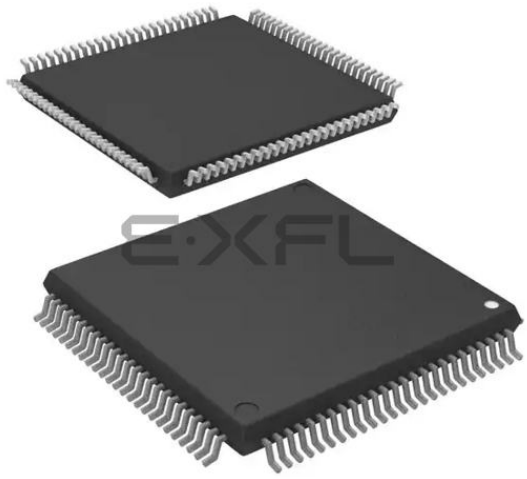
Renesas Electronics America Inc - UPD78F1848AGC-UEU-AX Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0R
Core Size	16-Bit
Speed	20MHz
Connectivity	CSI, I²C, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	80
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f1848agc-ueu-ax

(2) Non-port functions (1/3): 78K0R/KF3-C

Function Name	I/O	Function	After Reset	Alternate Function
ANI0 to ANI7	Input	A/D converter analog input	Digital input port	P20 to P27
ANI8 to ANI11	Input	A/D converter analog input	Digital input port	P150 to P153
CECIN	Input	Serial data input for CEC	Input port	P110
CECIO	I/O	Serial data I/O for CEC	Input port	P62
CECOUT	Output	Serial data output for CEC	Input port	P111
EXLVI	Input	Potential input for external low-voltage detection	Input port	P120/INTP0
INTP0	Input	External interrupt request input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified	Input port	P120/EXLVI
INTP1				P50
INTP2				P51
INTP3				P30/RTC1HZ
INTP4				P31/TI03/TO03
INTP5				P16/TI01/TO01
INTP7				P55/PCLBUZ1
INTP8				P74/KR4
KR0 to KR3	Input	Key interrupt input	Input port	P70 to P73
KR4				P74/INTP8
KR5 to KR7				P75 to P77
PCLBUZ0	Output	Clock output/buzzer output	Input port	P140
PCLBUZ1				P55/INTP7
REGC	–	Connecting regulator output (2.4 V) stabilization capacitance for internal operation. Connect to V_{SS} via a capacitor (0.47 to 1 μF).	–	–
RIN01	Input	Remote control receive data input (channels 0, 1)	Input port	P46
RIN23	Input	Remote control receive data input (channels 2, 3)	Input port	P47
ROUT	Output	Remote control receive data output	Input port	P91
RTCDIV	Output	Real-time counter clock (32 kHz divided frequency) output	Input port	P15/RTCCL
RTCCL	Output	Real-time counter clock (32 kHz original oscillation) output	Input port	P15/RTCDIV
RTC1HZ	Output	Real-time counter correction clock (1 Hz) output	Input port	P30/INTP3
$\overline{\text{RESET}}$	Input	System reset input	–	–
RxD0	Input	Serial data input to UART0	Input port	P11/SI00
RxD1	Input	Serial data input to UART1	Input port	P03/SI10/SDA10
RxD2	Input	Serial data input to UART2	Input port	P143/SI20/SDA20
$\overline{\text{SCK00}}$	I/O	Clock input/output for CSI00, CSI01, CSI10, and CSI20	Input port	P10
$\overline{\text{SCK01}}$				P43
$\overline{\text{SCK10}}$				P04/SCL10
$\overline{\text{SCK20}}$				P142/SCL20
SCL0	I/O	Clock input/output for I^2C	Input port	P60
SCL10	I/O	Clock input/output for simplified I^2C	Input port	P04/$\overline{\text{SCK10}}$
SCL20				P142/$\overline{\text{SCK20}}$

(d) SO10

This is a serial data output pin of serial interface CSI10.

(e) $\overline{\text{SCK10}}$

This is a serial clock I/O pin of serial interface CSI10.

(f) TxD1

This is a serial data output pin of serial interface UART1.

(g) RxD1

This is a serial data input pin of serial interface UART1.

(h) SDA10

This is a serial data I/O pin of serial interface for simplified I^2C.

(i) SCL10

This is a serial clock I/O pin of serial interface for simplified I^2C.

Caution To use P02/SO10/TxD1, P03/SI10/RxD1/SDA10, or P04/$\overline{\text{SCK10}}$/SCL10 as a general-purpose port, note the serial array unit 0 setting. For details, refer to the following tables.

- **Table 11-7 Relationship Between Register Settings and Pins (Channel 2 of Unit 0: CSI10, UART1 Transmission, IIC10)**
- **Table 11-8 Relationship Between Register Settings and Pins (Channel 3 of Unit 0: UART1 Reception)**

In addition, clear port output mode register 0 (POM0) to 00H.

2.2.2 P10 to P17 (port 1)

P10 to P17 function as an 8-bit I/O port. These pins also function as external interrupt request input, serial interface data I/O, clock I/O, timer I/O, and real-time counter clock output.

Input to the P10 and P11 pins can be specified through a normal input buffer or a TTL input buffer in 1-bit units, using port input mode register 1 (PIM1).

Output from the P10 and P12 pins can be specified as normal CMOS output or N-ch open-drain output (V_{DD} tolerance) in 1-bit units, using port output mode register 1 (POM1).

The following operation modes can be specified in 1-bit units.

(1) Port mode

P10 to P17 function as an 8-bit I/O port. P10 to P17 can be set to input or output port in 1-bit units using port mode register 1 (PM1). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 1 (PU1).

(2) Control mode

P10 to P12 and P15 to P17 function as external interrupt request input, serial interface data I/O, clock I/O, timer I/O, and real-time counter clock output.

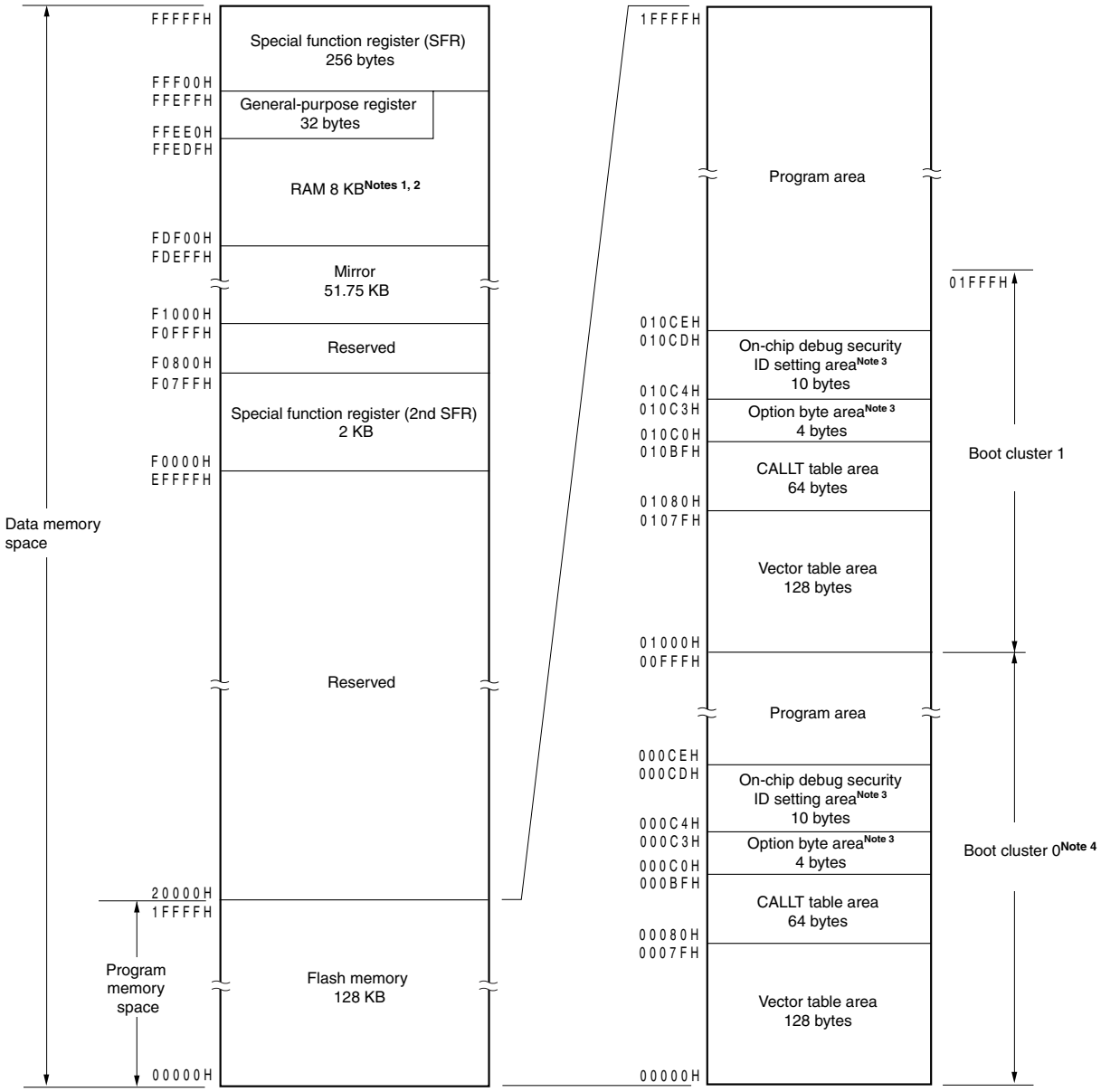
(a) SI00

This is a serial data input pin of serial interface CSI00.

(b) SO00

This is a serial data output pin of serial interface CSI00.

Figure 3-2. Memory Map (μPD78F1847A, 78F1849A)



Notes 1. While using the self-programming function, the area of FFE20H to FFEFFH and FDF00H to FE2FFH cannot be used as a stack memory.

2. Instructions can be executed from the RAM area excluding the general-purpose register area.

3. When boot swap is not used: Set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.

When boot swap is used: Set the option bytes to 000C0H to 000C3H and 010C0H to 010C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 010C4H to 010CDH.

4. Writing boot cluster 0 can be prohibited depending on the setting of security (see **25.7 Security Setting**).

Table 3-5. SFR List (3/5)

Address	Special Function Register (SFR) Name	Symbol	R/W	Manipulable Bit Range			After Reset
				1-bit	8-bit	16-bit	
FFF5EH	Remote controller receive data register 3	RMDR3	R/W	–	√	–	00H
FFF5FH	Remote controller receive counter register 3	RMSCR3	R/W	–	√	–	00H
FFF60H	Remote controller receive shift register 3	RMSR3	R/W	–	√	–	00H
FFF61H	Remote control reception error bit detection register 3	RMERBD3	R/W	–	√	–	00H
FFF62H	Remote control reception error bit detection shift register 3	RMERBSR3	R/W	–	√	–	00H
FFF63H	Remote controller receive interrupt status register 3	RMINTS3	R/W	–	√	–	00H
FFF64H	Timer data register 02	TDR02	R/W	–	–	√	0000H
FFF65H							
FFF66H	Timer data register 03	TDR03	R/W	–	–	√	0000H
FFF67H							
FFF68H	Timer data register 04	TDR04	R/W	–	–	√	0000H
FFF69H							
FFF6AH	Timer data register 05	TDR05	R/W	–	–	√	0000H
FFF6BH							
FFF6CH	Timer data register 06	TDR06	R/W	–	–	√	0000H
FFF6DH							
FFF6EH	Timer data register 07	TDR07	R/W	–	–	√	0000H
FFF6FH							
FFF70H	Timer data register 10	TDR10	R/W	–	–	√	0000H
FFF71H							
FFF72H	Timer data register 11	TDR11	R/W	–	–	√	0000H
FFF73H							
FFF74H	Timer data register 12	TDR12	R/W	–	–	√	0000H
FFF75H							
FFF78H	CEC transmission buffer register	CTXD	R/W	–	√	–	
FFF79H	CEC reception buffer register	CRXD	R	–	√	–	
FFF7AH	CEC communication error status register	CECES	R	–	√	–	
FFF7BH	CEC communication status register	CECS	R	–	√	–	
FFF7CH	CEC communication error flag clear trigger register	CECFC	R/W	√	√	–	
FFF7DH	CEC control register 0	CECCTL0	R/W	√	√	–	
FFF90H	Sub-count register	RSUBC	R	–	–	√	0000H
FFF91H							
FFF92H	Second count register	SEC	R/W	–	√	–	00H
FFF93H	Minute count register	MIN	R/W	–	√	–	00H
FFF94H	Hour count register	HOUR	R/W	–	√	–	12H[Note]
FFF95H	Week count register	WEEK	R/W	–	√	–	00H
FFF96H	Day count register	DAY	R/W	–	√	–	01H
FFF97H	Month count register	MONTH	R/W	–	√	–	01H
FFF98H	Year count register	YEAR	R/W	–	√	–	00H
FFF99H	Watch error correction register	SUBCUD	R/W	–	√	–	00H

Note The value of this register is 00H if the AMPM bit (bit 3 of the RTCC0 register) is set to 1 after reset.

(4) Port function register 6 (PF6)

This register sets whether to use pin P62 as I/O port mode or CECIO mode.

Input to the P62 pin can be specified through a normal input buffer or a CEC input buffer, using port function register 6 (PF6) and port input mode register 6 (PIM6).

Whether to connect a diode can be set by setting the PF6 register and pull-up resistor option register 6 (PU6).

Figure 4-58. Format of Port Function Register 6 (PF6)

Address: F0076H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PF6	0	0	0	0	0	PF62	0	0

PF62	P62 operation mode specification
0	Used as I/O port mode
1	Used as CECIO mode

Figure 4-59. Relationship Between PF6 Register, PIM6 Register, and PU6 Register

PF62	PIM62	Input buffer specification
0	0	Normal input buffer
0	1	
1	0	
1	1	CEC input buffer

PF62	PU62	Diode connection
0	0	Does not connect pull-up resistor to diode
0	1	
1	0	
1	1	Connects pull-up resistor to diode

Caution CECIO and CECIN/CECOUT pins must not be used at the same time.
Do not set PF110 and PF111 to 1 while PF62 = 1.
Do not set PF62 to 1 while PF110 and PF111 = 1.

4.5 Settings of PF11, PF6, Port Mode Register, and Output Latch When Using Alternate Function

To use the alternate function of a port pin, set the PF11, PF6, port mode register, and output latch as shown in Table 4-7.

Table 4-7. Settings of PF11, PF6, Port Mode Register, and Output Latch When Using Alternate Function (1/4)

Pin Name	Alternate Function		PF11	PF6	PM××	P××
	Function Name	I/O				
P00	TI00Note	Input			1	×
P01	TO00Note	Output			0	0
P02	SO10	Output			0	1
	TxD1	Output			0	1
P03	SI10	Input			1	×
	RxD1	Input			1	×
	SDA10	I/O			0	1
P04	$\overline{\text{SCK10}}$	Input			1	×
		Output			0	1
	SCL10	I/O			0	1
P05	TI05Note	Input			1	×
	TO05Note	Output			0	0
P06	TI06Note	Input			1	×
	TO06Note	Output			0	0
P10	$\overline{\text{SCK00}}$	Input			1	×
		Output			0	1
P11	SI00	Input			1	×
	RxD0	Input			1	×
P12	SO00	Output			0	1
	TxD0	Output			0	1
P15	RTCDIV	Output			0	0
	RTCCL	Output			0	0
P16	TI01	Input			1	×
	TO01	Output			0	0
	INTP5	Input			1	×
P17	TI02	Input			1	×
	TO02	Output			0	0

Remark ×: don't care
PM××: Port mode register
P××: Port output latch

Note The ports with which TI00, TO00, TI05/TO05, TI06/TO06, and TI07/TO07 pins are shared differ depending on the product.
78K0R/KF3-C: P53/TI00, P52/TO00, P05/TI05/TO05, P06/TI06/TO06, P54/TI07/TO07
78K0R/KG3-C: P00/TI00, P01/TO00, P46/INTP1/TI05/TO05/RIN01, P131/TI06/TO06, P145/TI07/TO07

Remark f_X: X1 clock oscillation frequency
f_{IH}: Internal high-speed oscillation clock frequency
f_{IH20}: 20 MHz internal high-speed oscillation clock frequency
f_{EX}: External main system clock frequency
f_{MX}: High-speed system clock frequency
f_{MAIN}: Main system clock frequency
f_{MAINC}: Main system select clock frequency
f_{XT}: XT1 clock oscillation frequency
f_{SUB}: Subsystem clock frequency
f_{CLK}: CPU/peripheral hardware clock frequency
f_{IL}: Internal low-speed oscillation clock frequency

5.3 Registers Controlling Clock Generator

The following eight registers are used to control the clock generator.

- Clock operation mode control register (CMC)
- Clock operation status control register (CSC)
- Oscillation stabilization time counter status register (OSTC)
- Oscillation stabilization time select register (OSTS)
- System clock control register (CKC)
- 20 MHz internal high-speed oscillation control register (DSCCTL)
- Peripheral enable registers 0, 1 (PER0, PER1)
- Operation speed mode control register (OSMC)

(1) Clock operation mode control register (CMC)

This register is used to set the operation mode of the X1/P121, X2/EXCLK/P122, XT1/P123, and XT2/P124 pins, and to select a gain of the oscillator.

CMC can be written only once by an 8-bit memory manipulation instruction after reset release. This register can be read by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 6-66. Operation Procedure of One-Shot Pulse Output Function (1/2)

	Software Operation	Hardware Status
TAU default setting		Power-off status (Clock supply is stopped and writing to each register is disabled.)
	Sets the TAU0EN bit, TAU0EN bit of the PER0 register to 1. →	Power-on status. Each channel stops operating. (Clock supply is started and writing to each register is enabled.)
	Sets the TPSm register. Determines clock frequencies of CKm0 and CKm1.	
Channel default setting	Sets the TMRmn and TMRmp registers of two channels to be used (determines operation mode of channels). An output delay is set to the TDRmn register of the master channel, and a pulse width is set to the TDRmp register of the slave channel.	Channel stops operating. (Clock is supplied and some power is consumed.)
	Sets slave channel. The TOMmp bit of the TOMm register is set to 1 (slave channel output mode). Sets the TOLmp bit. Sets the TOmp bit and determines default level of the TOmp output. →	The TOmn pin goes into Hi-Z output state. The TOmp default setting level is output when the port mode register is in output mode and the port register is 0.
	Sets TOEmp to 1 and enables operation of TOmp. →	TOmp does not change because channel stops operating.
	Clears the port register and port mode register to 0. →	The TOmp pin outputs the TOmp set level.

Remark m: Unit number, n: Channel number, p: Slave channel number (p = n+1),
When m = 0: n = 0, 2, 4, 6
When m = 1: n = 0

Figure 9-2. Format of Clock Output Select Register n (CKSn)

Address: FFFA5H (CKS0), FFFA6H (CKS1) After reset: 00H R/W

Symbol	<7>	6	5	4	3	2	1	0
CKSn	PCLOEn	0	0	0	CSELn	CCSn2	CCSn1	CCSn0

PCLOEn	PCLBUZn output enable/disable specification
0	Output disable (default)
1	Output enable

CSELn	CCSn2	CCSn1	CCSn0		PCLBUZn output clock selection		
					f_{MAIN} = 5 MHz	f_{MAIN} = 10 MHz	f_{MAIN} = 20 MHz
0	0	0	0	f_{MAIN}	5 MHz	10 MHz	Setting prohibited[Note]
0	0	0	1	$f_{MAIN}/2$	2.5 MHz	5 MHz	10 MHz
0	0	1	0	$f_{MAIN}/2^2$	1.25 MHz	2.5 MHz	5 MHz
0	0	1	1	$f_{MAIN}/2^3$	625 kHz	1.25 MHz	2.5 MHz
0	1	0	0	$f_{MAIN}/2^4$	312.5 kHz	625 kHz	1.25 MHz
0	1	0	1	$f_{MAIN}/2^{11}$	2.44 kHz	4.88 kHz	9.76 kHz
0	1	1	0	$f_{MAIN}/2^{12}$	1.22 kHz	2.44 kHz	4.88 kHz
0	1	1	1	$f_{MAIN}/2^{13}$	610 Hz	1.22 kHz	2.44 kHz
1	0	0	0	f_{SUB}	32.768 kHz		
1	0	0	1	$f_{SUB}/2$	16.384 kHz		
1	0	1	0	$f_{SUB}/2^2$	8.192 kHz		
1	0	1	1	$f_{SUB}/2^3$	4.096 kHz		
1	1	0	0	$f_{SUB}/2^4$	2.048 kHz		
1	1	0	1	$f_{SUB}/2^5$	1.024 kHz		
1	1	1	0	$f_{SUB}/2^6$	512 Hz		
1	1	1	1	$f_{SUB}/2^7$	256 Hz		

Note Setting an output clock exceeding 10 MHz is prohibited.

Cautions 1. Change the output clock after disabling clock output (PCLOEn = 0).

2. To shift to STOP mode when the main system clock is selected (CSELn = 0), set PCLOEn = 0 before executing the STOP instruction. When the subsystem clock is selected (CSELn = 1), PCLOEn = 1 can be set because the clock can be output in STOP mode.

Remarks 1. n = 0, 1

2. f_{MAIN}: Main system clock frequency

f_{SUB}: Subsystem clock frequency

10.4 A/D Converter Operations

10.4.1 Basic operations of A/D converter

<1> Set bit 5 (ADCEN) of peripheral enable register 0 (PER0) to 1 to start the supply of the input clock to the A/D converter.

<2> Set the A/D conversion time by using bits 5 to 1 (FR2 to FR0, LV1, and LV0) of ADM, and set the operation mode by using bit 6 (ADMD) of ADM.

<3> Set bit 0 (ADCE) of A/D converter mode register (ADM) to 1 to start the operation of the A/D voltage comparator.

<4> Set the channels for A/D conversion to analog input by using the A/D port configuration register (ADPC) and set to input mode by using port mode registers (PM2 and PM15).

<5> Select one channel for A/D conversion using the analog input channel specification register (ADS).

<6> Start the conversion operation by setting bit 7 (ADCS) of ADM to 1.
A timer trigger wait state is entered if the timer trigger mode is set in step <7>.
(<7> to <13> are operations performed by hardware.)

<7> The voltage input to the selected analog input channel is sampled by the sample & hold circuit.

<8> When sampling has been done for a certain time, the sample & hold circuit is placed in the hold state and the sampled voltage is held until the A/D conversion operation has ended.

<9> Bit 9 of the successive approximation register (SAR) is set. The series resistor string voltage tap is set to (1/2) AV_{REF} by the tap selector.

<10> The voltage difference between the series resistor string voltage tap and sampled voltage is compared by the voltage comparator. If the analog input is greater than (1/2) AV_{REF}, the MSB of SAR remains set to 1. If the analog input is smaller than (1/2) AV_{REF}, the MSB is reset to 0.

<11> Next, bit 8 of SAR is automatically set to 1, and the operation proceeds to the next comparison. The series resistor string voltage tap is selected according to the preset value of bit 9, as described below.

- Bit 9 = 1: (3/4) AV_{REF}
- Bit 9 = 0: (1/4) AV_{REF}

The voltage tap and sampled voltage are compared and bit 8 of SAR is manipulated as follows.

- Sampled voltage ≥ Voltage tap: Bit 8 = 1
- Sampled voltage < Voltage tap: Bit 8 = 0

<12> Comparison is continued in this way up to bit 0 of SAR.

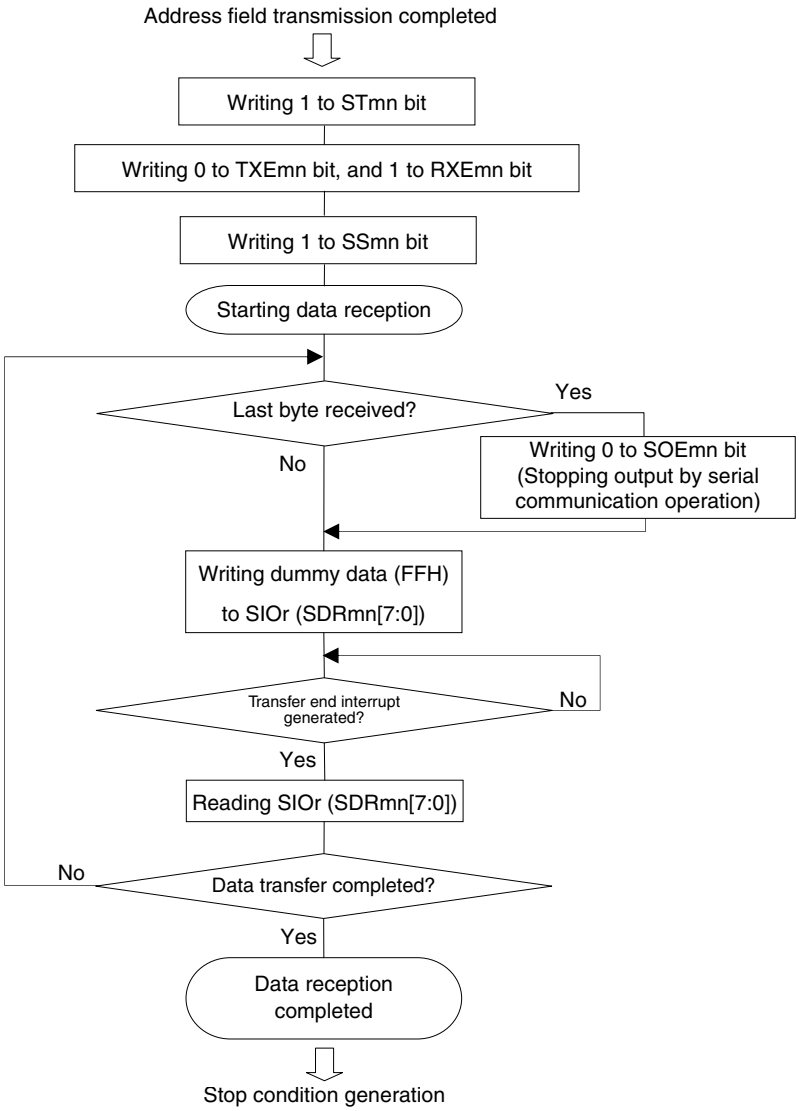
<13> Upon completion of the comparison of 10 bits, an effective digital result value remains in SAR, and the result value is transferred to the A/D conversion result register (ADCR, ADCRH) and then latched.
At the same time, the A/D conversion end interrupt request (INTAD) can also be generated.

<14> Repeat steps <7> to <13>, until ADCS is cleared to 0.
To stop the A/D converter, clear ADCS to 0.
To restart A/D conversion from the status of ADCE = 1, start from <6>. To start A/D conversion again when ADCE = 0, set ADCE to 1, wait for 1 μs or longer, and start <6>. To change a channel of A/D conversion, start from <5>.

Caution Make sure the period of <3> to <6> is 1 μs or more.

Remark Two types of A/D conversion result registers are available.
- ADCR (16 bits): Store 10-bit A/D conversion value
- ADCRH (8 bits): Store 8-bit A/D conversion value

Figure 11-96. Flowchart of Data Reception



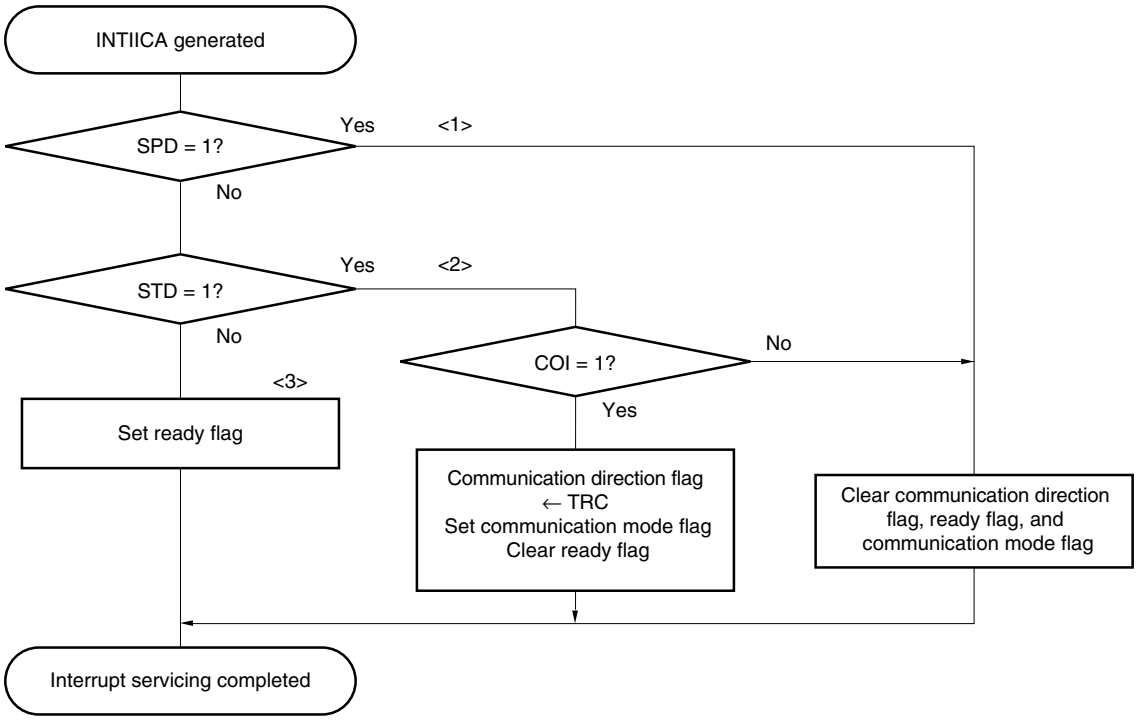
Caution ACK is not output when the last data is received (NACK). Communication is then completed by setting "1" to the STmn bit to stop operation and generating a stop condition.

An example of the processing procedure of the slave with the INTIICA interrupt is explained below (processing is performed assuming that no extension code is used). The INTIICA interrupt checks the status, and the following operations are performed.

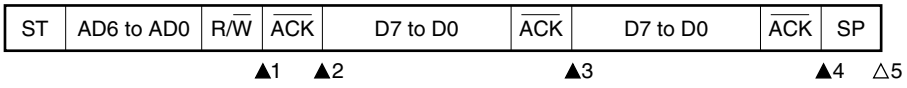
<1> Communication is stopped if the stop condition is issued.
<2> If the start condition is issued, the address is checked and communication is completed if the address does not match. If the address matches, the communication mode is set, wait is cancelled, and processing returns from the interrupt (the ready flag is cleared).
<3> For data transmit/receive, only the ready flag is set. Processing returns from the interrupt with the I^2C bus remaining in the wait state.

Remark <1> to <3> above correspond to <1> to <3> in Figure 12-31 Slave Operation Flowchart (2).

Figure 12-31. Slave Operation Flowchart (2)



(ii) When WTIM = 1



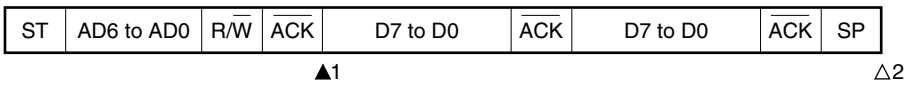
▲1: IICS = 0110×010B
▲2: IICS = 0010×110B
▲3: IICS = 0010×100B
▲4: IICS = 0010××00B
△5: IICS = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE = 1
×: Don't care

(6) Operation when arbitration loss occurs (no communication after arbitration loss)

When the device is used as a master in a multi-master system, read the MSTS bit each time interrupt request signal INTIICA has occurred to check the arbitration result.

(a) When arbitration loss occurs during transmission of slave address data (when WTIM = 1)



▲1: IICS = 01000110B
△2: IICS = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE = 1

The meanings of <1> to <7> in (1) Start condition ~ address ~ data in Figure 12-33 are explained below.

<1> The start condition trigger is set by the master device (STT = 1) and a start condition (SDA0 = 0 and SCL0 = 1) is generated once the bus data line goes low (SDA0 = 0). When the start condition is subsequently detected, the master device enters the master device communication status (MSTS = 1). The master device is ready to communicate once the bus clock line goes low (SCL0 = 0) after the hold time has elapsed.

<2> The master device writes the address + W (transmission) to the IICA shift register (IICA) and transmits the slave address.

<3> If the address received matches the address of a slave device[Note], that slave device sends an ACK by hardware to the master device. The ACK is detected by the master device (ACKD = 1) at the rising edge of the 9th clock.

<4> The master device issues an interrupt (INTIICA: end of address transmission) at the falling edge of the 9th clock, and the slave device whose address matched the transmitted slave address also issues an interrupt (INTIICA: address match). The master device and slave device also set a wait status (SCL0 = 0)[Note] when the addresses match.

<5> The timing at which the master device sets the wait status changes to the 8th clock (WTIM = 0).

<6> The slave device writes the data to transmit to the IICA register and releases the wait status that it set by the slave device.

<7> If the master device releases the wait status (WREL = 1), the slave device starts transferring data to the master device.

Note If the transmitted address does not match the address of the slave device, the slave device does not return an ACK to the master device (NACK: SDA0 = 1). The slave device also does not issue the INTIICA interrupt (address match) and does not set a wait status. The master device, however, issues the INTIICA interrupt (end of address transmission) regardless of whether it receives an ACK or NACK.

Remark <1> to <19> in Figure 12-33 represent the entire procedure for communicating data using the I^2C bus. Figure 12-33 (1) Start condition ~ address ~ data shows the processing from <1> to <7>, Figure 12-33 (2) Address ~ data ~ data shows the processing from <3> to <12>, and Figure 12-33 (3) Data ~ data ~ stop condition shows the processing from <8> to <19>.

(3) CEC transmission interrupt

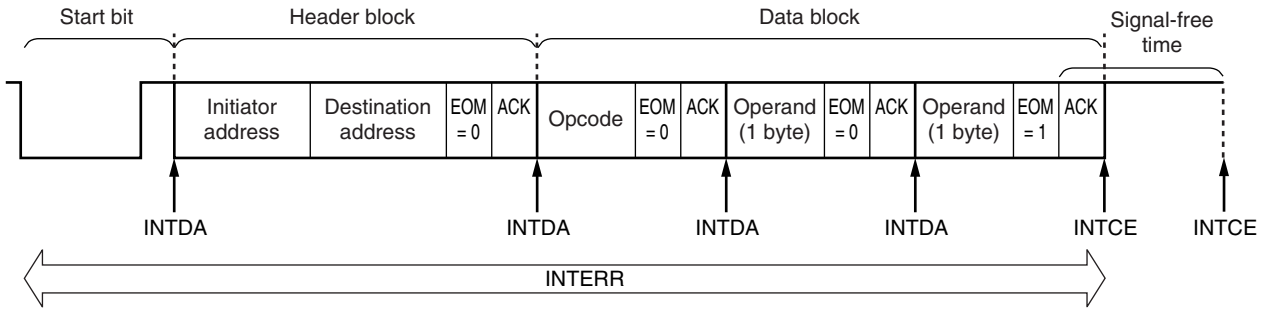
The hardware has three interrupt functions, namely a data interrupt (INTDA), a communication complete interrupt (INTCE), and an error interrupt (INTERR).

A data interrupt (INTDA) occurs at the start of each block.

A communication complete interrupt (INTCE) can be generated if ACK reception for a data block for which EOM is set to 1 ends, if the signal-free time specified using SFT1 and SFT0 elapses, or if both conditions occur, depending on the settings of CESEL1 and CESEL0.

An error interrupt (INTERR) is generated if a timing error, ACK error, underrun error, transmission error, or bus lock error is detected during any period of time during communication.

Figure 13-49. Interrupt Generation Timing



Caution If the falling edge of the CEC line is detected when receiving the ACK bit by setting EOM to 1 (before receiving the ACK bit ends), an irregular operation is performed as shown in Table 13-2 according to that timing.

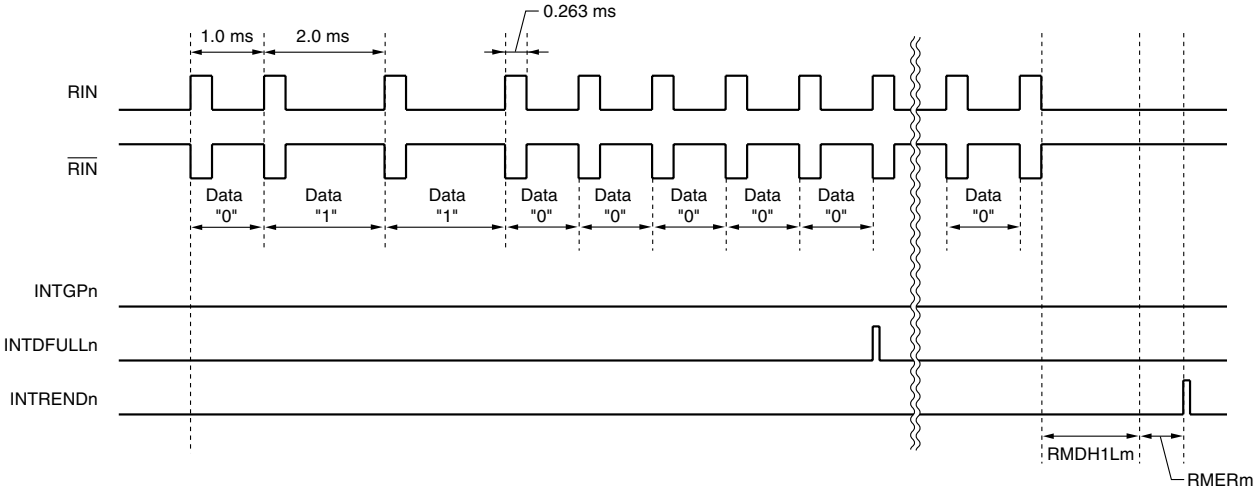
Table 13-2. Operation If Falling Edge of CEC Line Is Detected before Receiving ACK Bit Ends

CEC Line Falling Timing	Values Specified for CESEL1 and CESEL0 Bits of CECCTL1 Register	INTCE Generation	Handling of ACK Bit	Operation after CEC Line Falls
After the minimum data bit value (DATBL ≤ counter)	CESEL1 and CESEL0 are 0 and 0, or 0 and 1, respectively.	INTCE is generated once when the CEC line falls.	Handling the ACK bit is enabled because it has the correct width. (ACK or NACK is correctly determined.)	The start of the next communication is recognized and then determining whether to receive the start bit starts.
	CESEL1 and CESEL0 are 1 and 0, respectively.	INTCE is not generated.		
Before the minimum data bit value (counter < DATBL)	CESEL1 and CESEL0 are 0 and 0, or 0 and 1, respectively.	INTCE is generated once when the CEC line falls.	ACK cannot be correctly determined because it has the incorrect width. (If ACKTEN is set to 1, a timing error occurs.)	
	CESEL1 and CESEL0 are 1 and 0, respectively.	INTCE is not generated.		

14.5.5 Format of type C reception mode

Figure 14-36 shows the data format for type C.

Figure 14-36. Example of Type C Data Format



Remarks 1. m = 02, 13, n = 0 to 3

2. $\overline{\text{RIN}}$ is the internally inverted signal of RIN. Input the $\overline{\text{RIN}}$ waveform to RMIN (see **Figure 14-1**).

14.5.6 Operation flow of type C reception mode

Figure 14-37 shows the operation flow.

Cautions 1. When INTRERRn is generated, RMSRn and RMSCRn are automatically cleared immediately.

2. When data has been set to all the bits of RMSRn, the following processing is automatically performed.

- **The value of RMSRn is transferred to RMDRn.**
- **INTDFULLn is generated.**
- **RMSRn is cleared.**

RMDRn must then be read before the next data is set to all the bits of RMSRn.

3. When INTRENDn has been generated, read RMSCRn first followed by RMSRn.
When RMSRn has been read, RMSCRn and RMSRn are automatically cleared.
If INTRENDn is generated, the next data cannot be received until RMSRn is read.

4. RMSRn, RMSCRn, and RMDRn are cleared simultaneously to operation termination (RMENm = 0).

5. In type C reception mode, if the conditions for receiving a data low-/high-level width are not met before the first INTDFULLn interrupt is generated, INTRERRn will not be generated. However, RMSRn and RMSCRn will be cleared.

Remark m = 02, 13, n = 0 to 3

(2) Type B reception mode

After the guide pulse has been detected normally, the INTRERRn signal is generated under any of the following conditions.

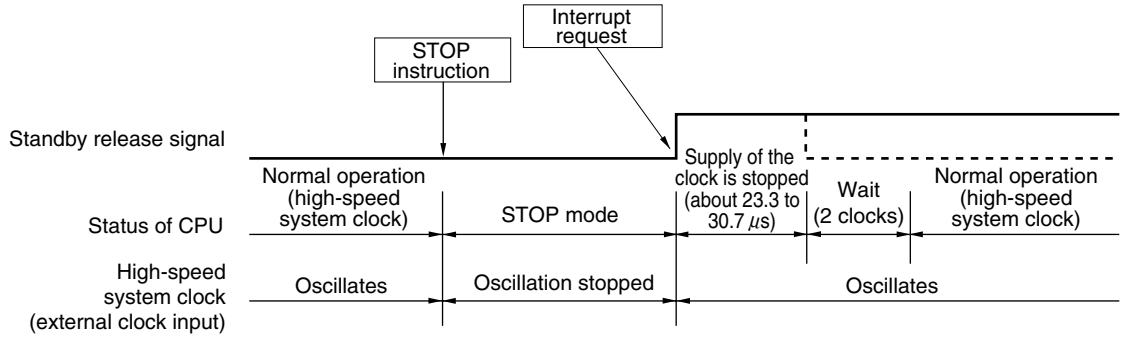
- Counter < RMDLSm at the rising edge of RMIN
- RMDLLm ≤ counter while RMIN is at low level
- Counter < RMDH0Sm at the falling edge of RMIN
- RMDH0Lm ≤ counter < RMDH1Sm at the falling edge of RMIN
- RMDH1Lm ≤ counter and counter after RMDH1Lm < RMERm at the falling edge of RMIN

The INTRERRn signal is not generated until the guide pulse is detected.
Once the INTRERRn signal has been generated, it will not be generated again until the next guide pulse is detected. The generation timing of the INTRERRn signal is shown in **Figure 14-45**.

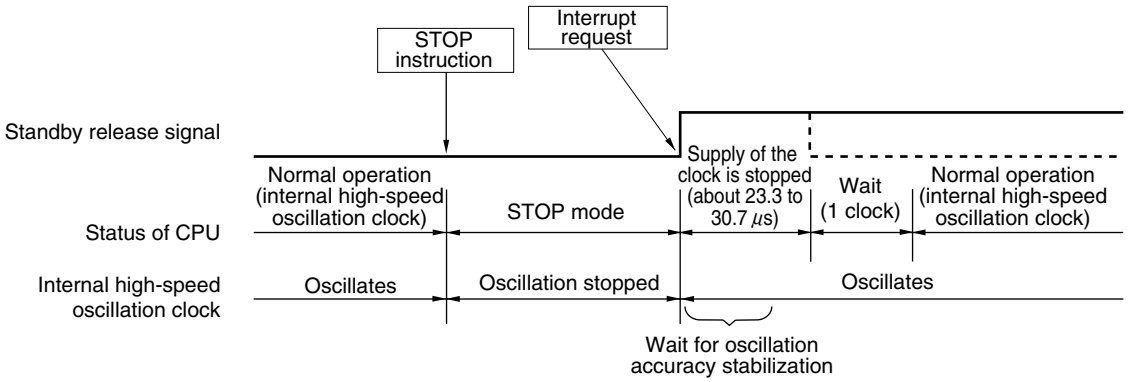
Remark m = 02, 13, n = 0 to 3

Figure 19-5. STOP Mode Release by Interrupt Request Generation (2/2)

(2) When high-speed system clock (external clock input) is used as CPU clock

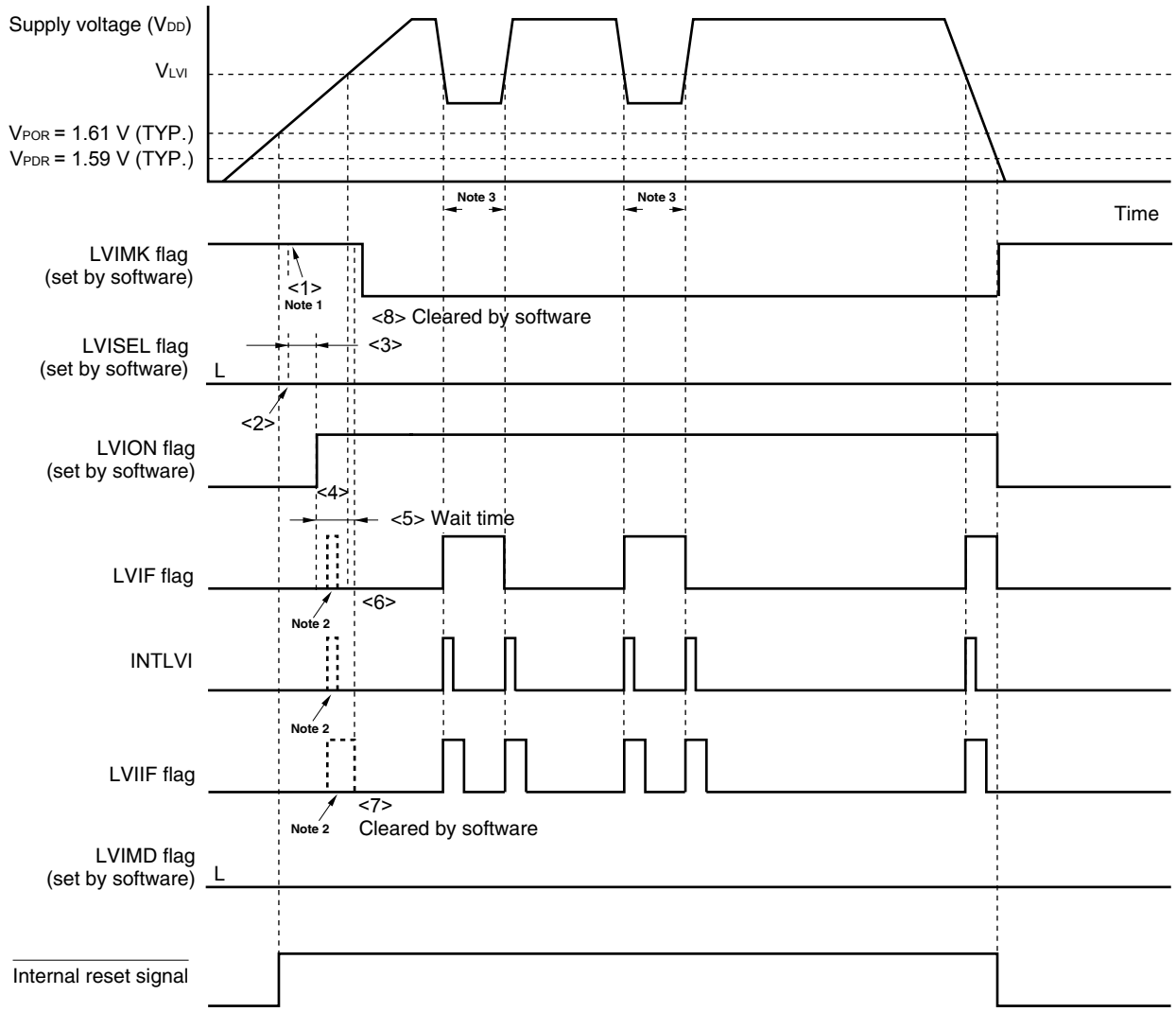


(3) When internal high-speed oscillation clock is used as CPU clock



Remark The broken lines indicate the case when the interrupt request that has released the standby mode is acknowledged.

Figure 22-8. Timing of Low-Voltage Detector Interrupt Signal Generation (Bit: LVISEL = 0, Option Byte: LVIOFF = 1)



Notes 1. The LVIMK flag is set to "1" by reset signal generation.

2. The interrupt request signal (INTLVI) is generated and the LVIF and LVIIF flags may be set (1).

3. If LVI operation is disabled when the supply voltage (V_{DD}) is less than or equal to the detection voltage (V_{LVI}), an interrupt request signal (INTLVI) is generated and LVIIF may be set to 1.

Remarks 1. <1> to <8> in Figure 22-8 above correspond to <1> to <8> in the description of "When starting operation" in **22.4.2 (1) (a) When LVI default start function stopped is set (LVIOFF = 1).**

2. V_{POR}: POC power supply rise detection voltage
V_{PDR}: POC power supply fall detection voltage

Table 25-1. Wiring Between 78K0R/Kx3-C and Dedicated Flash Memory Programmer

Pin Configuration of Dedicated Flash Memory Programmer			78K0R/KF3-C		78K0R/KG3-C	
Signal Name	I/O	Pin Function	Pin Name	Pin No.	Pin Name	Pin No.
SI/RxD[Notes 1, 2]	Input	Receive signal	TOOL0/P40	9	TOOL0/P40	12
SO/TxD[Note 2]	Output	Transmit signal				
SCK	Output	Transfer clock	–	–	–	–
CLK	Output	Clock output	–	–	–	–
/RESET	Output	Reset signal	$\overline{\text{RESET}}$	10	$\overline{\text{RESET}}$	13
FLMD0	Output	Mode signal	FLMD0	13	FLMD0	16
V_{DD}	I/O	V_{DD} voltage generation/ power monitoring	V_{DD}	19	V_{DD}	22
			EV_{DD}	20	EV_{DD0}	23
					EV_{DD1}	53
			AV_{REF}	59	AV_{REF}	73
GND	–	Ground	V_{SS}	17	V_{SS}	20
			EV_{SS}	18	EV_{SS0}	21
					EV_{SS1}	43
			AV_{SS}	60	AV_{SS}	74

Notes 1. This pin is not required to be connected when using PG-FP5 or FL-PR5.

2. Connect SI/RxD or SO/TxD when using QB-MINI2.