NXP USA Inc. - MC9S08PA4AVSC Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	20MHz
Connectivity	LINbus, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	4
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	8-SOIC (0.154", 3.90mm Width)
Supplier Device Package	8-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s08pa4avsc

Table of Contents

1 Ordering parts

1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to nxp.com and perform a part number search for the following device numbers: PA4.

2 Part identification

2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

2.2 Format

Part numbers for this device have the following format:

MC 9 S08 PA AA (V) B CC

2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
MC	Qualification status	• MC = fully qualified, general market flow
9	Memory	• 9 = flash based
S08	Core	• S08 = 8-bit CPU
PA	Device family	• PA
AA	Approximate flash size in KB	• 4 = 4 KB
(V)	Mask set version	• (blank) = Any version[1] • A = Rev. 2 or later version, this is recommended for new design[1]

Table continues on the next page...

Field	Description	Values
B	Operating temperature range (°C)	• M = –40 to 125 • V = –40 to 105
CC	Package designator	• WJ = 20-SOIC • TJ = 20-TSSOP • TG = 16-TSSOP • DC = 8-DFN • SC = 8-SOIC

1. From June 1, 2017, (blank) and A share the same mask set version.

2.4 Example

This is an example part number:

MC9S08PA4AVWJ

3 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 1. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

5 General

5.1 Nonswitching electrical specifications

5.1.1 DC characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 2. DC characteristics

Symbol	C	Descriptions			Min	Typical[1]	Max	Unit
—	—	Operating voltage		—	2.7	—	5.5	V
V_{OH}	C	Output high voltage	All I/O pins, standard-drive strength	5 V, I_{load} = -5 mA	V_{DD} - 0.8	—	—	V
	C			3 V, I_{load} = -2.5 mA	V_{DD} - 0.8	—	—	V
	C		High current drive pins, high-drive strength[2]	5 V, I_{load} = -20 mA	V_{DD} - 0.8	—	—	V
	C			3 V, I_{load} = -10 mA	V_{DD} - 0.8	—	—	V
I_{OHT}	D	Output high current	Max total I_{OH} for all ports	5 V	—	—	-100	mA
				3 V	—	—	-50	
V_{OL}	C	Output low voltage	All I/O pins, standard-drive strength	5 V, I_{load} = 5 mA	—	—	0.8	V
	C			3 V, I_{load} = 2.5 mA	—	—	0.8	V
	C		High current drive pins, high-drive strength[2]	5 V, I_{load} =20 mA	—	—	0.8	V
	C			3 V, I_{load} = 10 mA	—	—	0.8	V
I_{OLT}	D	Output low current	Max total I_{OL} for all ports	5 V	—	—	100	mA
				3 V	—	—	50	
V_{IH}	P	Input high voltage	All digital inputs	V_{DD}>4.5V	0.70 × V_{DD}	—	—	V
	C			V_{DD}>2.7V	0.75 × V_{DD}	—	—	
V_{IL}	P	Input low voltage	All digital inputs	V_{DD}>4.5V	—	—	0.30 × V_{DD}	V
	C			V_{DD}>2.7V	—	—	0.35 × V_{DD}	
V_{hys}	C	Input hysteresis	All digital inputs	—	0.06 × V_{DD}	—	—	mV
$\|I_{In}\|$	P	Input leakage current	All input only pins (per pin)	V_{IN} = V_{DD} or V_{SS}	—	0.1	1	µA

Table continues on the next page...

Table 3. LVD and POR Specification (continued)

Symbol	C	Description		Min	Typ	Max	Unit
V_{LVDL}	C	Falling low-voltage detect threshold - low range (LVDV = 0)		2.56	2.61	2.66	V
V_{LVDW1L}	C	Falling low-voltage warning threshold - low range	Level 1 falling (LVWV = 00)	2.62	2.7	2.78	V
V_{LVDW2L}	C		Level 2 falling (LVWV = 01)	2.72	2.8	2.88	V
V_{LVDW3L}	C		Level 3 falling (LVWV = 10)	2.82	2.9	2.98	V
V_{LVDW4L}	C		Level 4 falling (LVWV = 11)	2.92	3.0	3.08	V
V_{HYSDL}	C	Low range low-voltage detect hysteresis		—	40	—	mV
V_{HYSWL}	C	Low range low-voltage warning hysteresis		—	80	—	mV
V_{BG}	P	Buffered bandgap output [4]		1.14	1.16	1.18	V

1. Maximum is highest voltage that POR is guaranteed.
2. POR ramp time must be longer than 20us/V to get a stable startup.
3. Rising thresholds are falling threshold + hysteresis.
4. Voltage factory trimmed at V_{DD} = 5.0 V, Temp = 25 °C

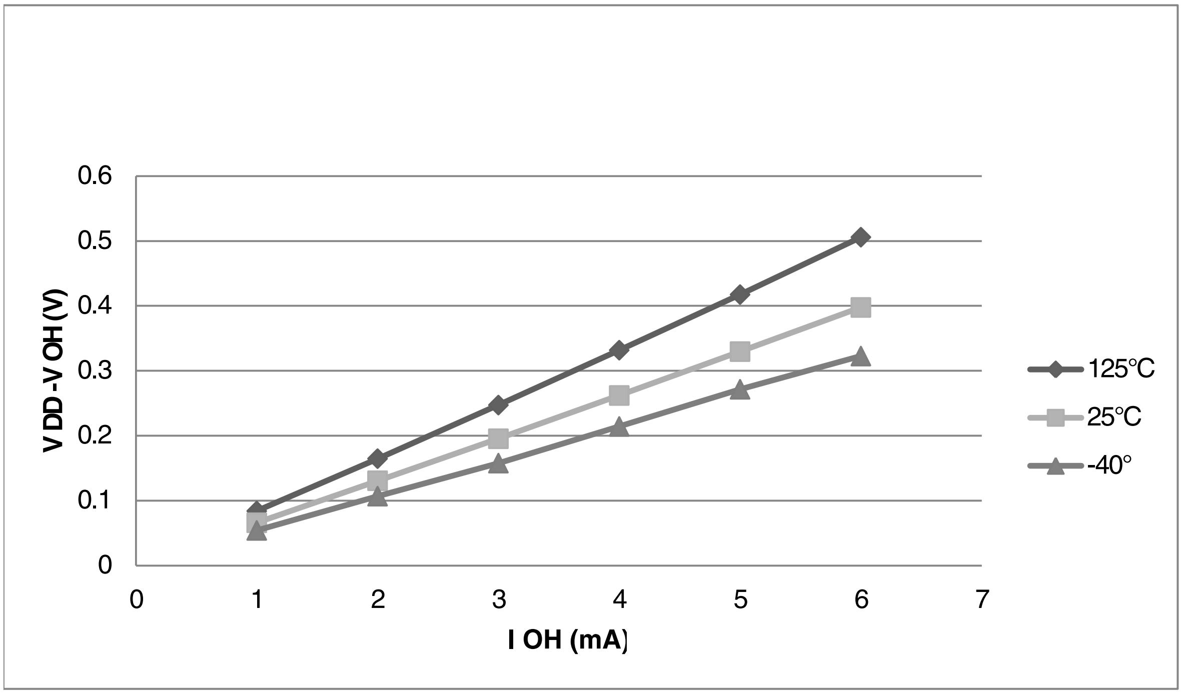


Figure 1. Typical I_{OH} Vs. V_{DD}-V_{OH} (standard drive strength) (V_{DD} = 5 V)

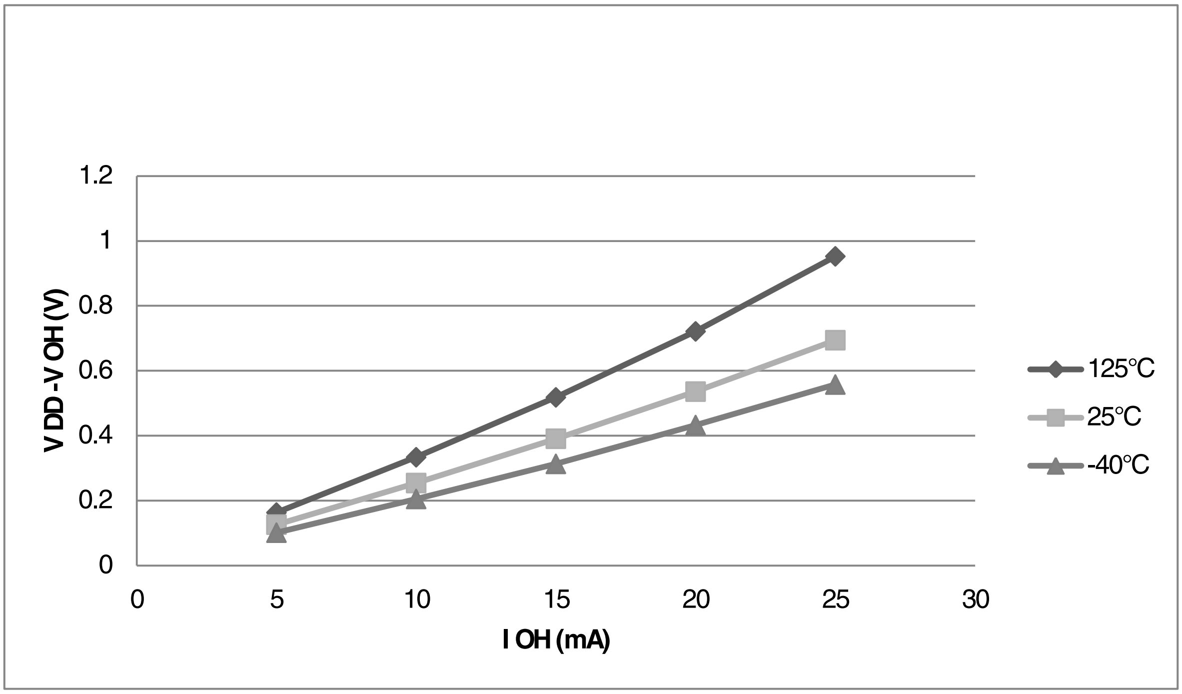


Figure 4. Typical I_{OH} Vs. V_{DD}-V_{OH} (high drive strength) (V_{DD} = 3 V)

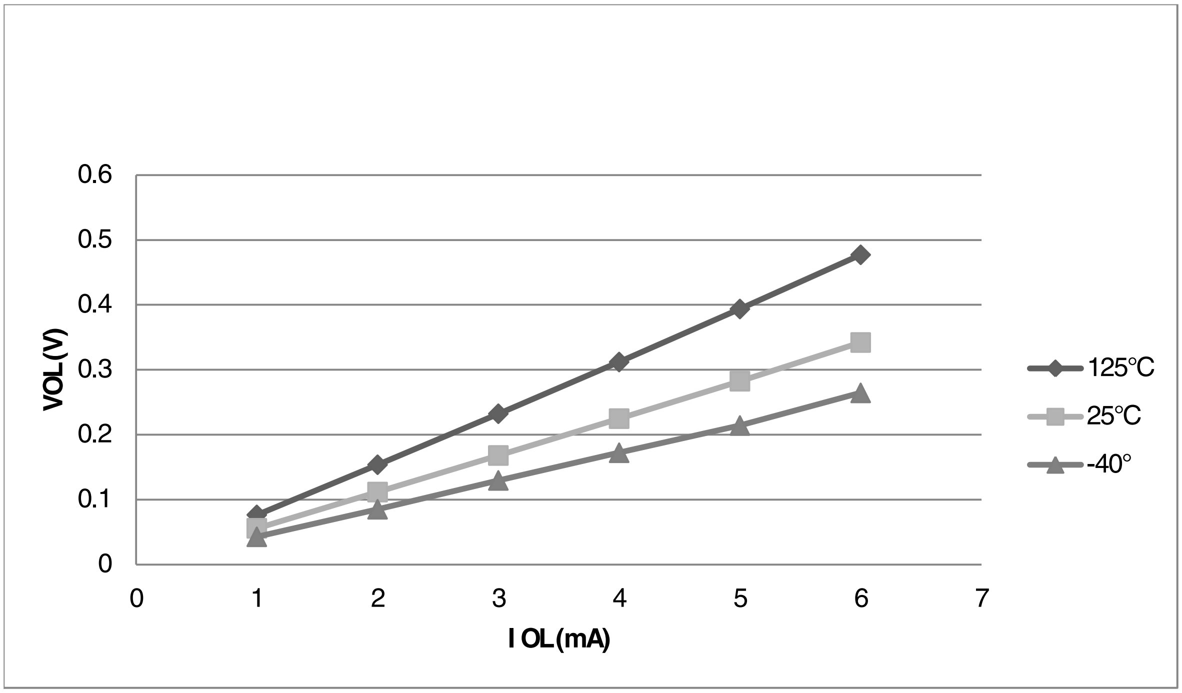


Figure 5. Typical I_{OL} Vs. V_{OL} (standard drive strength) (V_{DD} = 5 V)

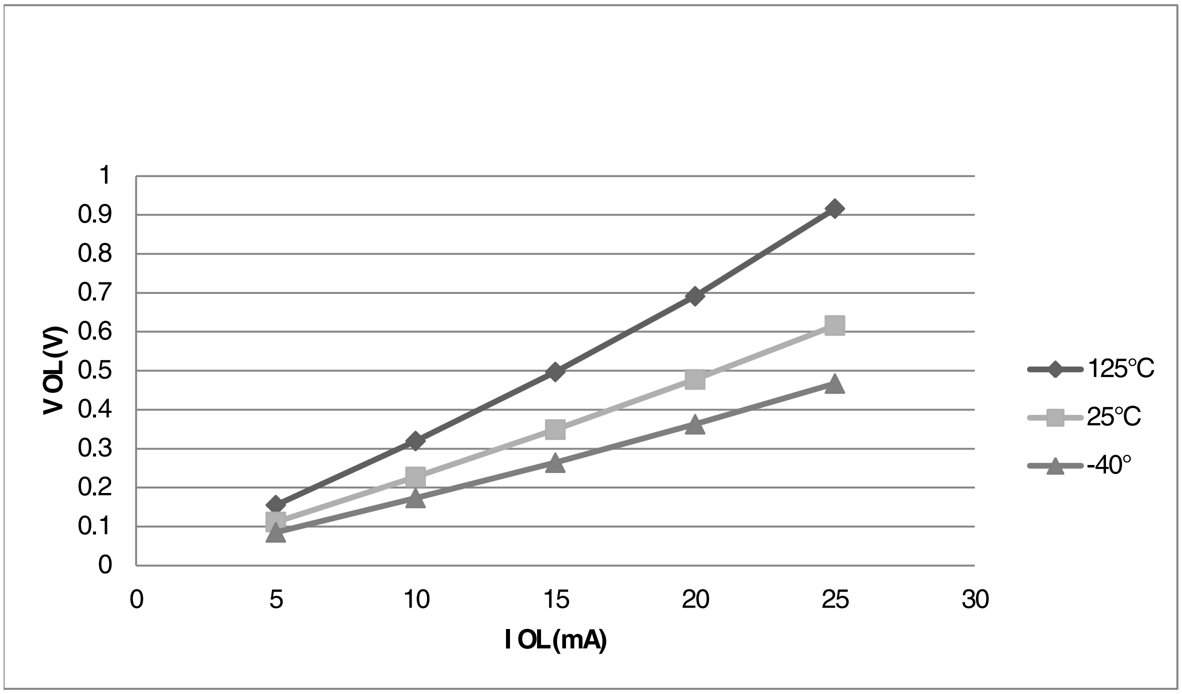


Figure 8. Typical I_{OL} Vs. V_{OL} (high drive strength) (V_{DD} = 3 V)

5.1.2 Supply current characteristics

This section includes information about power supply current in various operating modes.

Table 4. Supply current characteristics in operating temperature range

Num	C	Parameter	Symbol	Bus Freq	V_{DD} (V)	Typical[1]	Max	Unit
1	C	Run supply current FEI mode, all modules on; run from flash	RI_{DD}	20 MHz	5	5.43	—	mA
	C			10 MHz		3.46	—	
				1 MHz		1.71	—	
	C			20 MHz	3	5.35	—	
	C			10 MHz		3.45	—	
				1 MHz		1.69	—	
2	C	Run supply current FEI mode, all modules off and gated; run from flash	RI_{DD}	20 MHz	5	4.51	—	mA
	C			10 MHz		3.01	—	
				1 MHz		1.68	—	
	C			20 MHz	3	4.47	—	
	C			10 MHz		2.99	—	
				1 MHz		1.65	—	
3	P	Run supply current FBE mode, all modules on; run from RAM	RI_{DD}	20 MHz	5	5.31	7.41	mA
	C			10 MHz		3.17	—	
				1 MHz		1.25	—	
	C			20 MHz	3	5.29	—	

Table continues on the next page...

Table 4. Supply current characteristics in operating temperature range (continued)

Num	C	Parameter	Symbol	Bus Freq	V_{DD} (V)	Typical[1]	Max	Unit
	C			10 MHz		3.17	—	
				1 MHz		1.24	—	
4	P	Run supply current FBE mode, all modules off and gated; run from RAM	RI_{DD}	20 MHz	5	4.39	6.59	mA
	C			10 MHz		2.71	—	
				1 MHz		1.21	—	
	C			20 MHz	3	4.39	—	
	C			10 MHz		2.71	—	
				1 MHz		1.20	—	
5	C	Wait mode current FEI mode, all modules on	WI_{DD}	20 MHz	5	3.62	—	mA
	C			10 MHz		2.27	—	
				1 MHz		1.11	—	
	C			20 MHz	3	3.61	—	
				10 MHz		2.31	—	
				1 MHz		1.10	—	
6	C	Stop3 mode supply current no clocks active (except 1 kHz LPO clock)[2, 3]	$S3I_{DD}$	—	5	5.4	—	μA
	C			—	3	1.40	—	
7	C	ADC adder to stop3 ADLPC = 1 ADLSMP = 1 ADCO = 1 MODE = 10B ADICLK = 11B	—	—	5	96.0	—	μA
	C		—	—	3	88.3	—	
8	C	LVD adder to stop3[4]	—	—	5	129	—	μA
	C				3	126	—	

1. Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.
2. RTC adder cause <1 μA I_{DD} increase typically, RTC clock source is 1 kHz LPO clock.
3. ACMP adder cause <10 μA I_{DD} increase typically.
4. LVD is periodically woken up from stop3 by 5% duty cycle. The period is equal to or less than 2 ms.

5.1.3 EMC performance

Electromagnetic compatibility (EMC) performance is highly dependent on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult NXP applications notes such as AN2321, AN1050, AN1263, AN2764, and AN1259 for advice and guidance specifically targeted at optimizing EMC performance.

Table 6. Control timing (continued)

Num	C	Rating		Symbol	Min	Typical[1]	Max	Unit
	C	Port rise and fall time - high drive strength (load = 50 pF)[5]	—	t_{Rise}	—	5.4	—	ns
	C			t_{Fall}	—	4.6	—	ns

1. Typical values are based on characterization data at V_{DD} = 5.0 V, 25 °C unless otherwise stated.
2. This is the shortest pulse that is guaranteed to be recognized as a reset pin request.
3. To enter BDM mode following a POR, BKGD/MS must be held low during the powerup and for a hold time of t_{MSH} after V_{DD} rises above V_{LVD}.
4. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized.
5. Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels in operating temperature range.

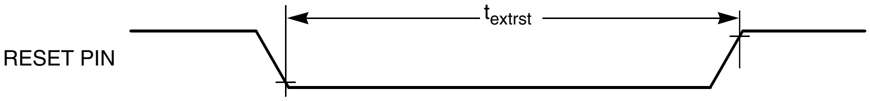


Figure 9. Reset timing

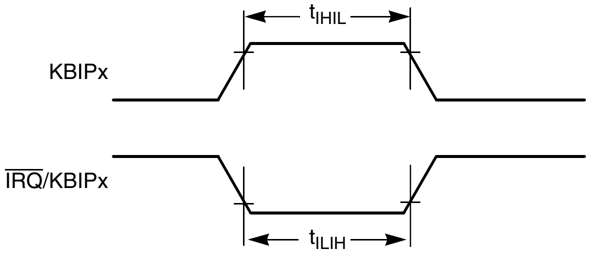


Figure 10. IRQ/KBIPx timing

5.2.2 Debug trace timing specifications

Table 7. Debug trace operating behaviors

Symbol	Description	Min.	Max.	Unit
t_{cyc}	Clock period	Frequency dependent		MHz
t_{wl}	Low pulse width	2	—	ns
t_{wh}	High pulse width	2	—	ns
t_r	Clock and data rise time	—	3	ns
t_f	Clock and data fall time	—	3	ns
t_s	Data setup	3	—	ns
t_h	Data hold	2	—	ns

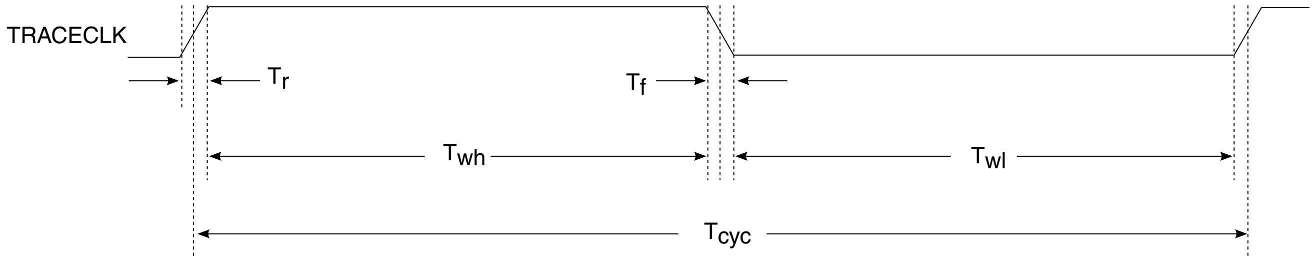


Figure 11. TRACE_CLKOUT specifications

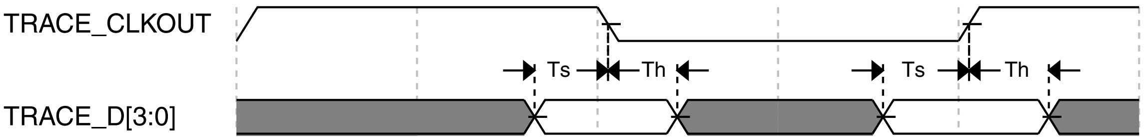


Figure 12. Trace data specifications

5.2.3 FTM module timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 8. FTM input timing

No.	C	Function	Symbol	Min	Max	Unit
1	D	External clock frequency	f_{TCLK}	0	$f_{Bus}/4$	Hz
2	D	External clock period	t_{TCLK}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

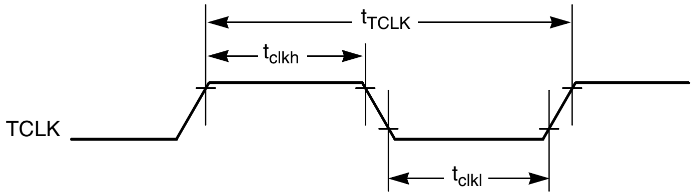


Figure 13. Timer external clock

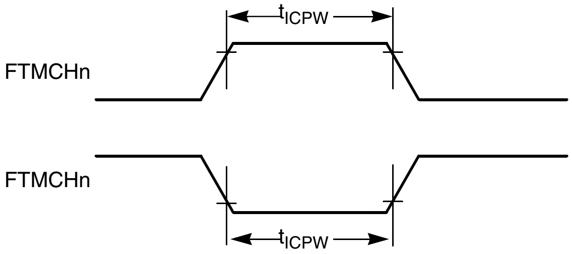


Figure 14. Timer input capture pulse

5.3 Thermal specifications

5.3.1 Thermal characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 9. Thermal characteristics

Rating	Symbol	Value	Unit
Operating temperature range (packaged)	T_A[1]	T_L to T_H • -40 to 125 for MC9S08PA4Mxx parts • -40 to 105 for MC9S08PA4Vxx parts	°C
Junction temperature range	T_J	-40 to 150	°C
Thermal resistance single-layer board			
20-pin SOIC	$R_{\theta JA}$	82	°C/W
20-pin TSSOP	$R_{\theta JA}$	115	°C/W
16-pin TSSOP	$R_{\theta JA}$	130	°C/W
8-pin DFN	$R_{\theta JA}$	170	°C/W
8-pin SOIC	$R_{\theta JA}$	150	°C/W
Thermal resistance four-layer board			
20-pin SOIC	$R_{\theta JA}$	54	°C/W
20-pin TSSOP	$R_{\theta JA}$	76	°C/W
16-pin TSSOP	$R_{\theta JA}$	87	°C/W
8-pin DFN	$R_{\theta JA}$	43	°C/W
8-pin SOIC	$R_{\theta JA}$	87	°C/W

1. Maximum T_A can be exceeded only if the user ensures that T_J does not exceed the maximum. The simplest method to determine T_J is: $T_J = T_A + R_{\theta JA}$ x chip power dissipation.

6 Peripheral operating requirements and behaviors

6.1 External oscillator (XOSC) and ICS characteristics

Table 10. XOSC and ICS specifications in operating temperature range

Num	C	Characteristic		Symbol	Min	Typical[1]	Max	Unit
1	C	Oscillator crystal or resonator	Low range (RANGE = 0)	f_{lo}	31.25	32.768	39.0625	kHz
	C		High range (RANGE = 1) FEE or FBE mode[2]	f_{hi}	4	—	20	MHz
	C		High range (RANGE = 1), high gain (HGO = 1), FBELP mode	f_{hi}	4	—	20	MHz
	C		High range (RANGE = 1), low power (HGO = 0), FBELP mode	f_{hi}	4	—	20	MHz
2	D	Load capacitors		C1, C2	See Note[3]			
3	D	Feedback resistor	Low Frequency, Low-Power Mode[4]	R_F	—	—	—	MΩ
			Low Frequency, High-Gain Mode		—	10	—	MΩ
			High Frequency, Low-Power Mode		—	1	—	MΩ
			High Frequency, High-Gain Mode		—	1	—	MΩ
4	D	Series resistor - Low Frequency	Low-Power Mode [4]	R_S	—	—	—	kΩ
			High-Gain Mode		—	200	—	kΩ
5	D	Series resistor - High Frequency	Low-Power Mode[4]	R_S	—	—	—	kΩ
	D	Series resistor - High Frequency, High-Gain Mode	4 MHz		—	0	—	kΩ
	D		8 MHz		—	0	—	kΩ
	D		16 MHz		—	0	—	kΩ
6	C	Crystal start-up time Low range = 32.768 kHz crystal; High range = 20 MHz crystal[5], [6]	Low range, low power	t_{CSTL}	—	1000	—	ms
	C		Low range, high power		—	800	—	ms
	C		High range, low power	t_{CSTH}	—	3	—	ms
	C		High range, high power		—	1.5	—	ms
7	T	Internal reference start-up time		t_{IRST}	—	20	50	μs
8	D	Square wave input clock frequency	FEE or FBE mode[2]	f_{extal}	0.03125	—	5	MHz
	D		FBELP mode		0	—	20	MHz

Table continues on the next page...

Table 10. XOSC and ICS specifications in operating temperature range (continued)

Num	C	Characteristic		Symbol	Min	Typical[1]	Max	Unit
9	P	Average internal reference frequency - trimmed		f_{int_t}	—	31.25	—	kHz
10	P	DCO output frequency range - trimmed		f_{dco_t}	16	—	20	MHz
11	P	Total deviation of DCO output from trimmed frequency[5]	Over full voltage and temperature range	Δf_{dco_t}	—	—	±2.0	%f_{dco}
	C		Over fixed voltage and temperature range of 0 to 70 °C				±1.0	
12	C	FLL acquisition time[5], [7]		$t_{Acquire}$	—	—	2	ms
13	C	Long term jitter of DCO output clock (averaged over 2 ms interval)[8]		C_{Jitter}	—	0.02	0.2	%f_{dco}

1. Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.
2. When ICS is configured for FEE or FBE mode, input clock source must be divisible using RDIV to within the range of 31.25 kHz to 39.0625 kHz.
3. See crystal or resonator manufacturer's recommendation.
4. Load capacitors (C_1,C_2), feedback resistor (R_F) and series resistor (R_S) are incorporated internally when RANGE = HGO = 0.
5. This parameter is characterized and not tested on each device.
6. Proper PC board layout procedures must be followed to achieve specifications.
7. This specification applies to any time the FLL reference source or reference divider is changed, trim value changed, or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
8. Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{Bus}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

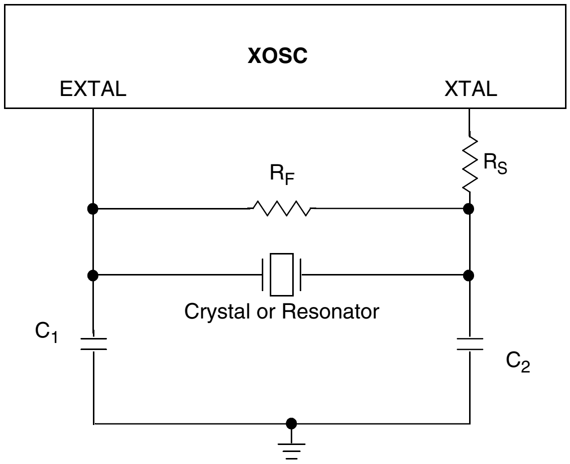


Figure 15. Typical crystal or resonator circuit

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Memory section.

6.3 Analog

6.3.1 ADC characteristics

Table 12. 5 V 12-bit ADC operating conditions

Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
Supply voltage	Absolute	V_{DDA}	2.7	—	5.5	V	—
	Delta to V_{DD} (V_{DD}-V_{DDAD})	ΔV_{DDA}	-100	0	+100	mV	
Ground voltage	Delta to V_{SS} (V_{SS}-V_{SSA})[2]	ΔV_{SSA}	-100	0	+100	mV	
Input voltage		V_{ADIN}	V_{REFL}	—	V_{REFH}	V	
Input capacitance		C_{ADIN}	—	4.5	5.5	pF	
Input resistance		R_{ADIN}	—	3	5	kΩ	—
Analog source resistance	12-bit mode • f_{ADCK} > 4 MHz • f_{ADCK} < 4 MHz	R_{AS}	— —	— —	2 5	kΩ	External to MCU
	10-bit mode • f_{ADCK} > 4 MHz • f_{ADCK} < 4 MHz		— —	— —	5 10		
	8-bit mode (all valid f_{ADCK})		—	—	10		
ADC conversion clock frequency	High speed (ADLPC=0)	f_{ADCK}	0.4	—	8.0	MHz	—
	Low power (ADLPC=1)		0.4	—	4.0		

1. Typical values assume V_{DDA} = 5.0 V, Temp = 25°C, f_{ADCK}=1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. DC potential difference.

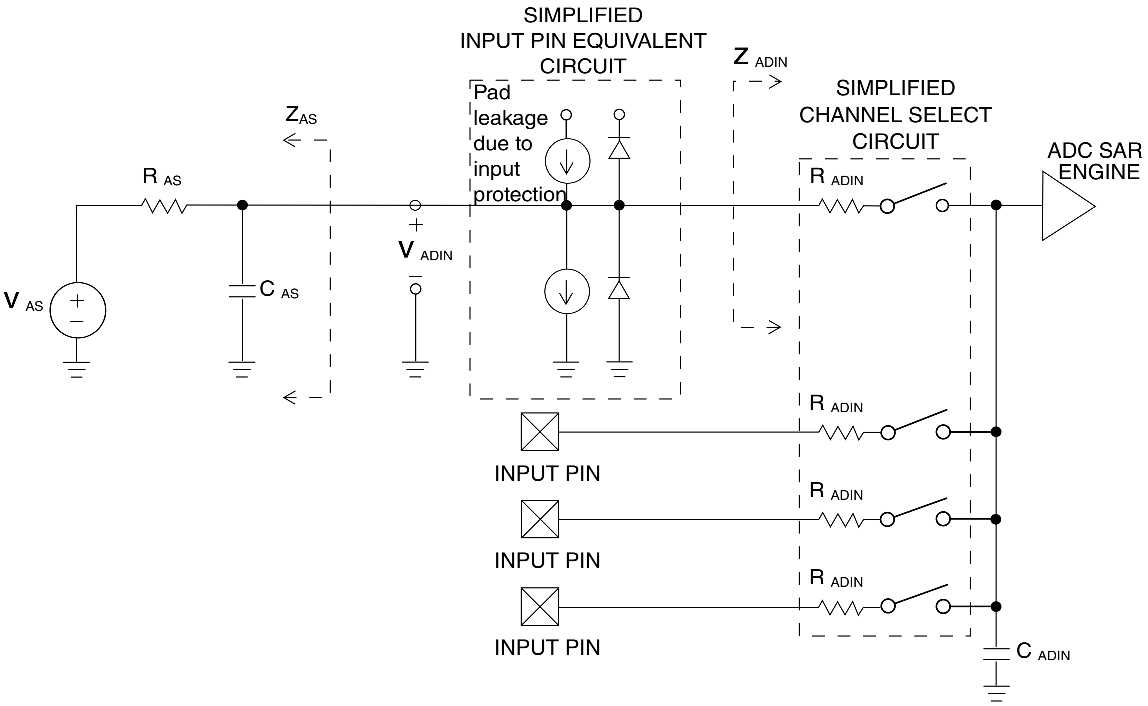


Figure 16. ADC input impedance equivalency diagram

Table 13. 12-bit ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

Characteristic	Conditions	C	Symb	Min	Typ[1]	Max	Unit
Supply current ADLPC = 1 ADLSMP = 1 ADCO = 1		T	I_{DDA}	—	133	—	µA
Supply current ADLPC = 1 ADLSMP = 0 ADCO = 1		T	I_{DDA}	—	218	—	µA
Supply current ADLPC = 0 ADLSMP = 1 ADCO = 1		T	I_{DDA}	—	327	—	µA
Supply current ADLPC = 0 ADLSMP = 0 ADCO = 1		T	I_{DDAD}	—	582	990	µA
Supply current	Stop, reset, module off	T	I_{DDA}	—	0.011	1	µA
ADC asynchronous clock source	High speed (ADLPC = 0)	P	f_{ADACK}	2	3.3	5	MHz

Table continues on the next page...

Table 13. 12-bit ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Characteristic	Conditions	C	Symb	Min	Typ[1]	Max	Unit
	Low power (ADLPC = 1)			1.25	2	3.3	
Conversion time (including sample time)	Short sample (ADLSMP = 0)	T	t_{ADC}	—	20	—	ADCK cycles
	Long sample (ADLSMP = 1)			—	40	—	
Sample time	Short sample (ADLSMP = 0)	T	t_{ADS}	—	3.5	—	ADCK cycles
	Long sample (ADLSMP = 1)			—	23.5	—	
Total unadjusted Error[2]	12-bit mode	T	E_{TUE}	—	±5.0	—	LSB[3]
	10-bit mode	P		—	±1.5	±2.0	
	8-bit mode	P		—	±0.7	±1.0	
Differential Non-Linearity	12-bit mode	T	DNL	—	±1.0	—	LSB[3]
	10-bit mode[4]	P		—	±0.25	±0.5	
	8-bit mode[4]	P		—	±0.15	±0.25	
Integral Non-Linearity	12-bit mode	T	INL	—	±1.0	—	LSB[3]
	10-bit mode	T		—	±0.3	±0.5	
	8-bit mode	T		—	±0.15	±0.25	
Zero-scale error[5]	12-bit mode	C	E_{ZS}	—	±2.0	—	LSB[3]
	10-bit mode	P		—	±0.25	±1.0	
	8-bit mode	P		—	±0.65	±1.0	
Full-scale error[6]	12-bit mode	T	E_{FS}	—	±2.5	—	LSB[3]
	10-bit mode	T		—	±0.5	±1.0	
	8-bit mode	T		—	±0.5	±1.0	
Quantization error	≤12 bit modes	D	E_Q	—	—	±0.5	LSB[3]
Input leakage error[7]	all modes	D	E_{IL}	$I_{In} * R_{AS}$			mV
Temp sensor slope	-40°C– 25°C	D	m	—	3.266	—	mV/°C
	25°C– 125°C			—	3.638	—	
Temp sensor voltage	25°C	D	V_{TEMP25}	—	1.396	—	V

1. Typical values assume V_{DDA} = 5.0 V, Temp = 25°C, f_{ADCK}=1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. Includes quantization.
3. 1 LSB = $(V_{REFH} - V_{REFL})/2^N$
4. Monotonicity and no-missing-codes guaranteed in 10-bit and 8-bit modes
5. $V_{ADIN} = V_{SSA}$
6. $V_{ADIN} = V_{DDA}$
7. I_{In} = leakage current (refer to DC characteristics)

6.3.2 Analog comparator (ACMP) electricals

Table 14. Comparator electrical specifications

C	Characteristic	Symbol	Min	Typical	Max	Unit
D	Supply voltage	V_{DDA}	2.7	—	5.5	V
T	Supply current (Operation mode)	I_{DDA}	—	10	20	μA
D	Analog input voltage	V_{AIN}	V_{SS} - 0.3	—	V_{DDA}	V
P	Analog input offset voltage	V_{AIO}	—	—	40	mV
C	Analog comparator hysteresis (HYST=0)	V_H	—	15	20	mV
C	Analog comparator hysteresis (HYST=1)	V_H	—	20	30	mV
T	Supply current (Off mode)	I_{DDAOFF}	—	60	—	nA
C	Propagation Delay	t_D	—	0.4	1	μs

7 Dimensions

7.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to nxp.com and perform a keyword search for the drawing’s document number:

If you want the drawing for this package	Then use this document number
8-pin DFN	98ASA00448D
8-pin SOIC	98ASB42564B
16-pin TSSOP	98ASH70247A
20-pin SOIC	98ASB42343B

8 Pinout

8.1 Signal multiplexing and pin assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

Table 15. Pin availability by package pin-count

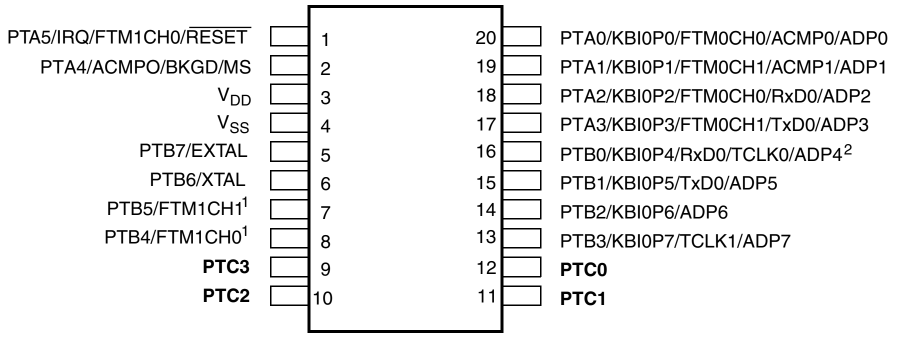
Pin Number			Lowest Priority <-- --> Highest				
20-SOIC/ TSSOP	16-TSSOP	8-DFN/SOIC	Port Pin	Alt 1	Alt 2	Alt 3	Alt 4
1	1	1	PTA5	IRQ	FTM1CH0	—	RESET
2	2	2	PTA4	—	ACMPO	BKGD	MS
3	3	3	—	—	—	—	V_{DD}
4	4	4	—	—	—	—	V_{SS}
5	5	—	PTB7	—	—	—	EXTAL
6	6	—	PTB6	—	—	—	XTAL
7	7	—	PTB5[1]	—	FTM1CH1	—	—
8	8	—	PTB4[1]	—	FTM1CH0	—	—
9	—	—	PTC3	—	—	—	—
10	—	—	PTC2	—	—	—	—
11	—	—	PTC1	—	—	—	—
12	—	—	PTC0	—	—	—	—
13	9	—	PTB3	KBI0P7	—	TCLK1	ADP7
14	10	—	PTB2	KBI0P6	—	—	ADP6
15	11	—	PTB1	KBI0P5	TxD0	—	ADP5
16	12	—	PTB0[2]	KBI0P4	RxD0	TCLK0	ADP4
17	13	5	PTA3	KBI0P3	FTM0CH1	TxD0	ADP3
18	14	6	PTA2	KBI0P2	FTM0CH0	RxD0	ADP2
19	15	7	PTA1	KBI0P1	FTM0CH1	ACMP1	ADP1
20	16	8	PTA0	KBI0P0	FTM0CH0	ACMP0	ADP0

1. This is a high current drive pin when operated as output.
2. This is a true open-drain pin when operated as output.

Note

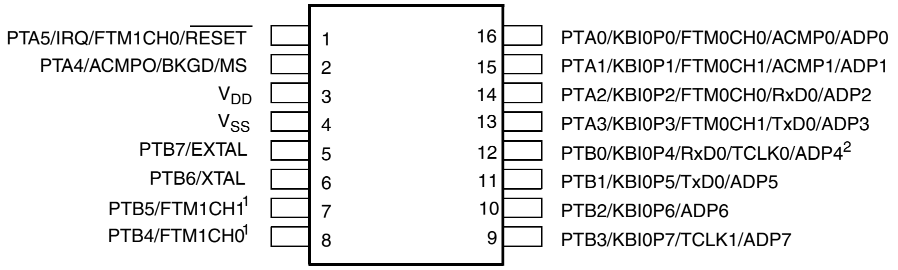
When an alternative function is first enabled, it is possible to get a spurious edge to the module. User software must clear any associated flags before interrupts are enabled. The table above illustrates the priority if multiple modules are enabled. The highest priority module will have control over the pin. Selecting a higher priority pin function with a lower priority function already enabled can cause spurious edges to the lower priority module. Disable all modules that share a pin before enabling another module.

8.2 Device pin assignment



Pins in **bold** are not available on less pin-count packages.
1. High source/sink current pins
2. True open drain pins

Figure 17. MC9S08PA4 20-pin SOIC/TSSOP packages



Pins in **bold** are not available on less pin-count packages.
1. High source/sink current pins
2. True open drain pins

Figure 18. 16-pin TSSOP package

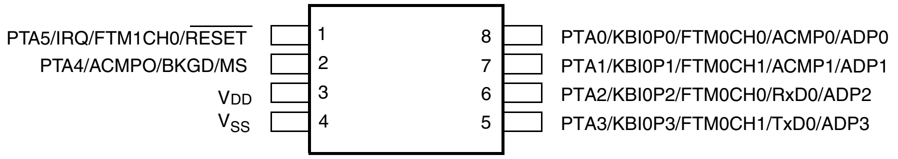


Figure 19. 8-pin DFN/SOIC packages

9 Revision history

The following table provides a revision history for this document.

Table 16. Revision history

Rev. No.	Date	Substantial Changes
2	12/2012	Initial public release
3	5/2014	• Renamed the low drive strength to standard drive strength. • Updated V_{DIO}. • Added footnote on the S3I_{DD}

Table continues on the next page...

Table 16. Revision history (continued)

Rev. No.	Date	Substantial Changes
		• Updated EMC test conditions to be f_{OSC} = 10 MHz and f_{SYS} = 20 MHz • Updated f_{int_t} • Updated Flash characteristics • Updated the rating descriptions for t_{Rise} and t_{Fall} • Updated footnote on $t_{Acquire}$ • Added new part of MC9S08PA4MTG with operating tempature range from -40 to 125 °C • Updated I_{LAT}
3.1	09/2014	• Updated the part number format to add new field for new part numbers in Fields.
4	06/2015	• Corrected the Min. of the t_{extrst} in Control timing • Updated Thermal characteristics to add footnote to the T_A and removed redundant information..
5	01/2017	• Updated to add FTM2 module.
6	08/2017	• Updated to add new package of 8-pin DFN.
7	12/2017	• Updated to add new packages of 20-pin TSSOP and 8-pin SOIC.
8	08/2018	• Add a note in Fields.