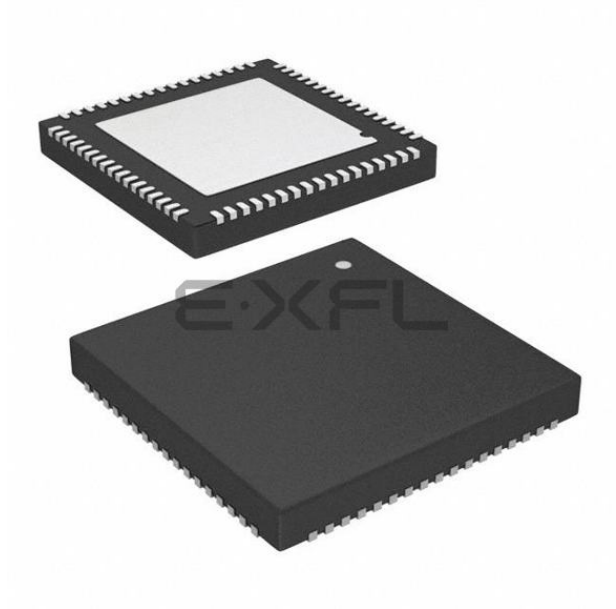

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SPI, UART/USART, USB
Peripherals	POR, PWM, WDT
Number of I/O	56
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	A/D 48x14b; D/A 2x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	68-VFQFN Exposed Pad
Supplier Device Package	68-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c24094-24ltxit

6. Getting Started

For in-depth information, along with detailed programming information, see the Technical Reference Manual for this PSoC device.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device datasheets on the web at http://www.cypress.com.

6.1 Application Notes

Cypress application notes are an excellent introduction to the wide variety of possible PSoC designs.

6.2 Development Kits

PSoC Development Kits are available online from and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

6.3 Training

Free PSoC technical training (on demand, webinars, and workshops), which is available online via www.cypress.com, covers a wide variety of topics and skill levels to assist you in your designs.

6.4 CYPros Consultants

Certified PSoC consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC consultant go to the CYPros Consultants web site.

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Visit our growing library of solution-focused designs. Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

6.6 Technical Support

Technical support – including a searchable Knowledge Base articles and technical forums – is also available online. If you cannot find an answer to your question, call our Technical Support hotline at 1-800-541-4736.

7. Development Tools

PSoC Designer™ is the revolutionary Integrated Design Environment (IDE) that you can use to customize PSoC to meet your specific application requirements. PSoC Designer software accelerates system design and time to market. Develop your applications using a library of precharacterized analog and digital peripherals (called user modules) in a drag-and-drop design environment. Then, customize your design by leveraging the dynamically generated application programming interface (API) libraries of code. Finally, debug and test your designs with the integrated debug environment, including in-circuit emulation and standard software debug features. PSoC Designer includes:

- Application editor graphical user interface (GUI) for device and user module configuration and dynamic reconfiguration
- Extensive user module catalog
- Integrated source-code editor (C and assembly)
- Free C compiler with no size restrictions or time limits
- Built-in debugger
- In-circuit emulation
- Built-in support for communication interfaces:
  - Hardware and software I^2C slaves and masters
  - Full speed USB 2.0
  - Up to four full-duplex universal asynchronous receiver/transmitters (UARTs), SPI master and slave, and wireless

PSoC Designer supports the entire library of PSoC 1 devices and runs on Windows XP, Windows Vista, and Windows 7.

7.1 PSoC Designer Software Subsystems

7.1.1 Design Entry

In the chip-level view, choose a base device to work with. Then select different onboard analog and digital components that use the PSoC blocks, which are called user modules. Examples of user modules are analog-to-digital converters (ADCs), digital-to-analog converters (DACs), amplifiers, and filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration makes it possible to change configurations at run time. In essence, this allows you to use more than 100 percent of PSoC's resources for an application.

7.1.2 Code Generation Tools

The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. You can develop your design in C, assembly, or a combination of the two.

Assemblers. The assemblers allow you to merge assembly code seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and are linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all of the features of C, tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

7.1.3 Debugger

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow you to read and program and

9.3 68-Pin Part Pinout

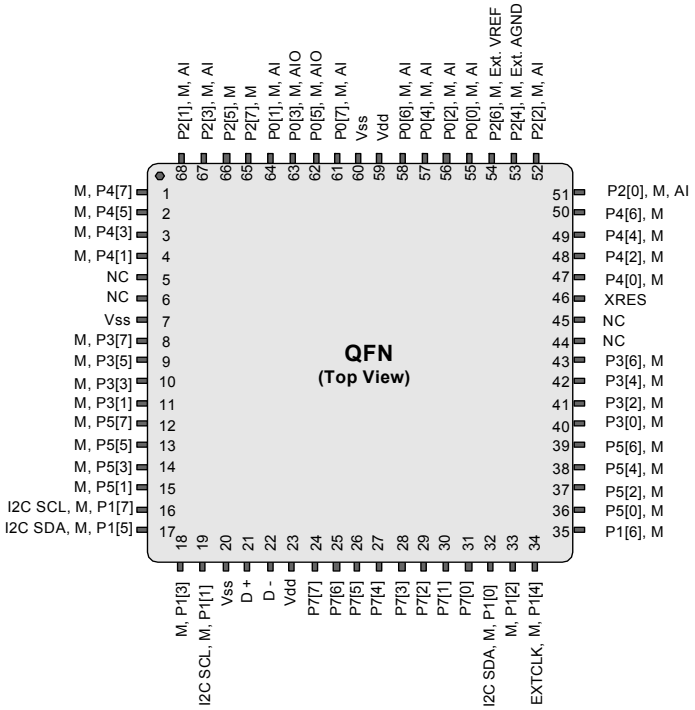
The following 68-pin QFN part table and drawing is for the CY8C24994 PSoC device.

Table 4. 68-Pin Part Pinout (QFN[9])

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	M	P4[7]	
2	I/O	M	P4[5]	
3	I/O	M	P4[3]	
4	I/O	M	P4[1]	
5			NC	No connection. Pin must be left floating
6			NC	No connection. Pin must be left floating
7	Power		V_{SS}	Ground connection [10]
8	I/O	M	P3[7]	
9	I/O	M	P3[5]	
10	I/O	M	P3[3]	
11	I/O	M	P3[1]	
12	I/O	M	P5[7]	
13	I/O	M	P5[5]	
14	I/O	M	P5[3]	
15	I/O	M	P5[1]	
16	I/O	M	P1[7]	I^2C SCL
17	I/O	M	P1[5]	I^2C SDA
18	I/O	M	P1[3]	
19	I/O	M	P1[1]	I2C SCL ISSP SCLK[11]
20	Power		V_{SS}	Ground connection [10]
21	USB		D+	
22	USB		D–	
23	Power		V_{DD}	Supply voltage
24	I/O		P7[7]	
25	I/O		P7[6]	
26	I/O		P7[5]	
27	I/O		P7[4]	
28	I/O		P7[3]	
29	I/O		P7[2]	
30	I/O		P7[1]	
31	I/O		P7[0]	
32	I/O	M	P1[0]	I^2C SDA, ISSP SDATA[11]
33	I/O	M	P1[2]	
34	I/O	M	P1[4]	Optional EXTCLK
35	I/O	M	P1[6]	
36	I/O	M	P5[0]	
37	I/O	M	P5[2]	
38	I/O	M	P5[4]	
39	I/O	M	P5[6]	
40	I/O	M	P3[0]	
41	I/O	M	P3[2]	
42	I/O	M	P3[4]	
43	I/O	M	P3[6]	
44			NC	No connection. Pin must be left floating.
45			NC	No connection. Pin must be left floating.
46	Input		XRES	Active high pin reset with internal pull-down.
47	I/O	M	P4[0]	
48	I/O	M	P4[2]	
49	I/O	M	P4[4]	
50	I/O	M	P4[6]	
51	I/O	I, M	P2[0]	Direct switched capacitor block input
52	I/O	I, M	P2[2]	Direct switched capacitor block input
53	I/O	M	P2[4]	External AGND input
54	I/O	M	P2[6]	External VREF input
55	I/O	I, M	P0[0]	Analog column mux input
56	I/O	I, M	P0[2]	Analog column mux input and column output
57	I/O	I, M	P0[4]	Analog column mux input and column output
58	I/O	I, M	P0[6]	Analog column mux input
59	Power		V_{DD}	Supply voltage
60	Power		V_{SS}	Ground connection [10]
61	I/O	I, M	P0[7]	Analog column mux input, integration input #1
62	I/O	I/O, M	P0[5]	Analog column mux input and column output, integration input #2
63	I/O	I/O, M	P0[3]	Analog column mux input and column output
64	I/O	I, M	P0[1]	Analog column mux input
65	I/O	M	P2[7]	
66	I/O	M	P2[5]	
67	I/O	I, M	P2[3]	Direct switched capacitor block input
68	I/O	I, M	P2[1]	Direct switched capacitor block input

LEGEND A = Analog, I = Input, O = Output, NC = No connection. Pin must be left floating, M = Analog Mux Input.

Figure 6. CY8C24994 68-Pin PSoC Device



Notes

9. The center pad on the QFN package should be connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it should be electrically floated and not connected to any other signal.
10. All V_{SS} pins should be brought out to one common GND plane.
11. These are the ISSP pins, which are not High Z at POR. See the PSoC Technical Reference Manual for details.

9.4 68-Pin Part Pinout (On-Chip Debug)

The following 68-pin QFN part table and drawing is for the CY8C24094 OCD PSoC device.

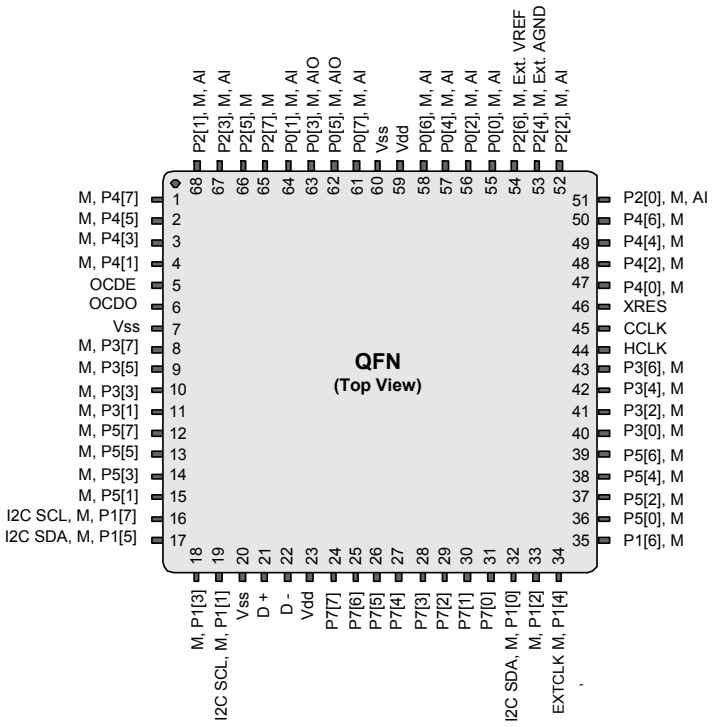
Note This part is only used for in-circuit debugging. It is NOT available for production.

Table 5. 68-Pin Part Pinout (QFN[12])

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	M	P4[7]	
2	I/O	M	P4[5]	
3	I/O	M	P4[3]	
4	I/O	M	P4[1]	
5			OCDE	OCD even data I/O
6			OCDO	OCD odd data output
7	Power		V_{SS}	Ground connection [13]
8	I/O	M	P3[7]	
9	I/O	M	P3[5]	
10	I/O	M	P3[3]	
11	I/O	M	P3[1]	
12	I/O	M	P5[7]	
13	I/O	M	P5[5]	
14	I/O	M	P5[3]	
15	I/O	M	P5[1]	
16	I/O	M	P1[7]	I^2C SCL
17	I/O	M	P1[5]	I^2C SDA
18	I/O	M	P1[3]	
19	I/O	M	P1[1]	I^2C SCL, ISSP SCLK [14]
20	Power		V_{SS}	Ground connection [13]
21	USB		D+	
22	USB		D–	
23	Power		V_{DD}	Supply voltage
24	I/O		P7[7]	
25	I/O		P7[6]	
26	I/O		P7[5]	
27	I/O		P7[4]	
28	I/O		P7[3]	
29	I/O		P7[2]	
30	I/O		P7[1]	
31	I/O		P7[0]	
32	I/O	M	P1[0]	I^2C SDA, ISSP SDATA[14]
33	I/O	M	P1[2]	
34	I/O	M	P1[4]	Optional EXTCLK
35	I/O	M	P1[6]	
36	I/O	M	P5[0]	
37	I/O	M	P5[2]	
38	I/O	M	P5[4]	
39	I/O	M	P5[6]	
40	I/O	M	P3[0]	
41	I/O	M	P3[2]	
42	I/O	M	P3[4]	
43	I/O	M	P3[6]	
44			HCLK	OCD high speed clock output
45			CCLK	OCD CPU clock output
46	Input		XRES	Active high pin reset with internal pull-down
47	I/O	M	P4[0]	
48	I/O	M	P4[2]	
49	I/O	M	P4[4]	
50	I/O	M	P4[6]	
51	I/O	I, M	P2[0]	Direct switched capacitor block input
52	I/O	I, M	P2[2]	Direct switched capacitor block input
53	I/O	M	P2[4]	External AGND input
54	I/O	M	P2[6]	External VREF input
55	I/O	I, M	P0[0]	Analog column mux input
56	I/O	I, M	P0[2]	Analog column mux input and column output
57	I/O	I, M	P0[4]	Analog column mux input and column output
58	I/O	I, M	P0[6]	Analog column mux input
59	Power		V_{DD}	Supply voltage
60	Power		V_{SS}	Ground connection [13]
61	I/O	I, M	P0[7]	Analog column mux input, integration input #1
62	I/O	I/O, M	P0[5]	Analog column mux input and column output, integration input #2
63	I/O	I/O, M	P0[3]	Analog column mux input and column output
64	I/O	I, M	P0[1]	Analog column mux input
65	I/O	M	P2[7]	
66	I/O	M	P2[5]	
67	I/O	I, M	P2[3]	Direct switched capacitor block input
68	I/O	I, M	P2[1]	Direct switched capacitor block input

LEGEND A = Analog, I = Input, O = Output, M = Analog Mux Input, OCD = On-Chip Debugger.

Figure 7. CY8C24094 68-Pin OCD PSoC Device



Notes

12. The center pad on the QFN package should be connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it should be electrically floated and not connected to any other signal.
13. All V_{SS} pins should be brought out to one common GND plane.
14. These are the ISSP pins, which are not High Z at POR. See the PSoC Technical Reference Manual for details.

10. Register Reference

This section lists the registers of the CY8C24x94 PSoC device family. For detailed register information, see the *PSoC Technical Reference Manual*.

10.1 Register Conventions

The register conventions specific to this section are listed in the following table.

Convention	Description
R	Read register or bit(s)
W	Write register or bit(s)
L	Logical register or bit(s)
C	Clearable register or bit(s)
#	Access is bit specific

10.2 Register Mapping Tables

The PSoC device has a total register address space of 512 bytes. The register space is referred to as I/O space and is divided into two banks, Bank 0 and Bank 1. The XOI bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XOI bit is set to 1, the user is in Bank 1.

Note In the following register mapping tables, blank fields are Reserved and should not be accessed.

10.3 Register Map Bank 0 Table: User Space

Name	Addr (0, Hex)	Access	Name	Addr (0, Hex)	Access	Name	Addr (0, Hex)	Access	Name	Addr (0, Hex)	Access
PRT0DR	00	RW	PMA0_DR	40	RW	ASC10CR0	80	RW		C0	
PRT0IE	01	RW	PMA1_DR	41	RW	ASC10CR1	81	RW		C1	
PRT0GS	02	RW	PMA2_DR	42	RW	ASC10CR2	82	RW		C2	
PRT0DM2	03	RW	PMA3_DR	43	RW	ASC10CR3	83	RW		C3	
PRT1DR	04	RW	PMA4_DR	44	RW	ASD11CR0	84	RW		C4	
PRT1IE	05	RW	PMA5_DR	45	RW	ASD11CR1	85	RW		C5	
PRT1GS	06	RW	PMA6_DR	46	RW	ASD11CR2	86	RW		C6	
PRT1DM2	07	RW	PMA7_DR	47	RW	ASD11CR3	87	RW		C7	
PRT2DR	08	RW	USB_SOF0	48	R		88			C8	
PRT2IE	09	RW	USB_SOF1	49	R		89			C9	
PRT2GS	0A	RW	USB_CR0	4A	RW		8A			CA	
PRT2DM2	0B	RW	USBI/O_CR0	4B	#		8B			CB	
PRT3DR	0C	RW	USBI/O_CR1	4C	RW		8C			CC	
PRT3IE	0D	RW		4D			8D			CD	
PRT3GS	0E	RW	EP1_CNT1	4E	#		8E			CE	
PRT3DM2	0F	RW	EP1_CNT	4F	RW		8F			CF	
PRT4DR	10	RW	EP2_CNT1	50	#	ASD20CR0	90	RW	CUR_PP	D0	RW
PRT4IE	11	RW	EP2_CNT	51	RW	ASD20CR1	91	RW	STK_PP	D1	RW
PRT4GS	12	RW	EP3_CNT1	52	#	ASD20CR2	92	RW		D2	
PRT4DM2	13	RW	EP3_CNT	53	RW	ASD20CR3	93	RW	IDX_PP	D3	RW
PRT5DR	14	RW	EP4_CNT1	54	#	ASC21CR0	94	RW	MVR_PP	D4	RW
PRT5IE	15	RW	EP4_CNT	55	RW	ASC21CR1	95	RW	MVW_PP	D5	RW
PRT5GS	16	RW	EP0_CR	56	#	ASC21CR2	96	RW	I2C_CFG	D6	RW
PRT5DM2	17	RW	EP0_CNT	57	#	ASC21CR3	97	RW	I2C_SCR	D7	#
	18		EP0_DR0	58	RW		98		I2C_DR	D8	RW
	19		EP0_DR1	59	RW		99		I2C_MSCR	D9	#
	1A		EP0_DR2	5A	RW		9A		INT_CLR0	DA	RW
	1B		EP0_DR3	5B	RW		9B		INT_CLR1	DB	RW
PRT7DR	1C	RW	EP0_DR4	5C	RW		9C		INT_CLR2	DC	RW
PRT7IE	1D	RW	EP0_DR5	5D	RW		9D		INT_CLR3	DD	RW
PRT7GS	1E	RW	EP0_DR6	5E	RW		9E		INT_MSK3	DE	RW
PRT7DM2	1F	RW	EP0_DR7	5F	RW		9F		INT_MSK2	DF	RW
DBB00DR0	20	#	AMX_IN	60	RW		A0		INT_MSK0	E0	RW
DBB00DR1	21	W	AMUXCFG	61	RW		A1		INT_MSK1	E1	RW
DBB00DR2	22	RW		62			A2		INT_VC	E2	RC
DBB00CR0	23	#	ARF_CR	63	RW		A3		RES_WDT	E3	W
DBB01DR0	24	#	CMP_CR0	64	#		A4		DEC_DH	E4	RC
DBB01DR1	25	W	ASY_CR	65	#		A5		DEC_DL	E5	RC
DBB01DR2	26	RW	CMP_CR1	66	RW		A6		DEC_CR0	E6	RW
DBB01CR0	27	#		67			A7		DEC_CR1	E7	RW
DCB02DR0	28	#		68		MUL1_X	A8	W	MUL0_X	E8	W
DCB02DR1	29	W		69		MUL1_Y	A9	W	MUL0_Y	E9	W
DCB02DR2	2A	RW		6A		MUL1_DH	AA	R	MUL0_DH	EA	R
DCB02CR0	2B	#		6B		MUL1_DL	AB	R	MUL0_DL	EB	R
DCB03DR0	2C	#	TMP_DR0	6C	RW	ACC1_DR1	AC	RW	ACC0_DR1	EC	RW
DCB03DR1	2D	W	TMP_DR1	6D	RW	ACC1_DR0	AD	RW	ACC0_DR0	ED	RW
DCB03DR2	2E	RW	TMP_DR2	6E	RW	ACC1_DR3	AE	RW	ACC0_DR3	EE	RW
DCB03CR0	2F	#	TMP_DR3	6F	RW	ACC1_DR2	AF	RW	ACC0_DR2	EF	RW
	30		ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
	31		ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
	32		ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
	34		ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
	35		ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
	36		ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
	37		ACB01CR2	77	RW		B7		CPU_F	F7	RL
	38			78			B8			F8	
	39			79			B9			F9	
	3A			7A			BA			FA	
	3B			7B			BB			FB	
	3C			7C			BC			FC	
	3D			7D			BD		DAC_D	FD	RW
	3E			7E			BE		CPU_SCR1	FE	#
	3F			7F			BF		CPU_SCR0	FF	#

Blank fields are reserved and should not be accessed. # Access is bit specific.

Table 20. 3.3-V DC Analog Reference Specifications

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b000	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.200	$V_{DD}/2$ + 1.290	$V_{DD}/2$ + 1.365	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.030	$V_{DD}/2$	$V_{DD}/2$ + 0.034	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.346	$V_{DD}/2$ – 1.292	$V_{DD}/2$ – 1.208	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.196	$V_{DD}/2$ + 1.292	$V_{DD}/2$ + 1.374	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.029	$V_{DD}/2$	$V_{DD}/2$ + 0.031	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.349	$V_{DD}/2$ – 1.295	$V_{DD}/2$ – 1.227	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.204	$V_{DD}/2$ + 1.293	$V_{DD}/2$ + 1.369	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.030	$V_{DD}/2$	$V_{DD}/2$ + 0.030	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.351	$V_{DD}/2$ – 1.297	$V_{DD}/2$ – 1.229	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.189	$V_{DD}/2$ + 1.294	$V_{DD}/2$ + 1.384	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.032	$V_{DD}/2$	$V_{DD}/2$ + 0.029	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.353	$V_{DD}/2$ – 1.297	$V_{DD}/2$ – 1.230	V
0b001	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.105	P2[4] + P2[6] – 0.008	P2[4] + P2[6] + 0.095	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.035	P2[4] – P2[6] + 0.006	P2[4] – P2[6] + 0.053	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.094	P2[4] + P2[6] – 0.005	P2[4] + P2[6] + 0.073	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.033	P2[4] – P2[6] + 0.002	P2[4] – P2[6] + 0.042	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.094	P2[4] + P2[6] – 0.003	P2[4] + P2[6] + 0.075	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.035	P2[4] – P2[6]	P2[4] – P2[6] + 0.038	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.095	P2[4] + P2[6] – 0.003	P2[4] + P2[6] + 0.080	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.038	P2[4] – P2[6]	P2[4] – P2[6] + 0.038	V

Note The bits PORLEV and VM in the following table refer to bits in the VLT_CR register. See the *PSoC Technical Reference Manual* for more information on the VLT_CR register.

Table 22. DC POR and LVD Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
	V_{DD} value for PPOR trip (positive ramp)					
V_{PPOR0R}	PORLEV[1:0] = 00b		2.91		V	
V_{PPOR1R}	PORLEV[1:0] = 01b	–	4.39	–	V	
V_{PPOR2R}	PORLEV[1:0] = 10b		4.55		V	
	V_{DD} value for PPOR trip (negative ramp)					
V_{PPOR0} [23]	PORLEV[1:0] = 00b		2.82		V	
V_{PPOR1} [23]	PORLEV[1:0] = 01b	–	4.39	–	V	
V_{PPOR2} [23]	PORLEV[1:0] = 10b		4.55		V	
	PPOR hysteresis					
V_{PH0}	PORLEV[1:0] = 00b	–	92	–	mV	
V_{PH1}	PORLEV[1:0] = 01b	–	0	–	mV	
V_{PH2}	PORLEV[1:0] = 10b	–	0	–	mV	
	V_{DD} value for LVD trip					
V_{LVD0}	VM[2:0] = 000b	2.86	2.92	2.98[24]	V	
V_{LVD1}	VM[2:0] = 001b	2.96	3.02	3.08	V	
V_{LVD2}	VM[2:0] = 010b	3.07	3.13	3.20	V	
V_{LVD3}	VM[2:0] = 011b	3.92	4.00	4.08	V	
V_{LVD4}	VM[2:0] = 100b	4.39	4.48	4.57	V	
V_{LVD5}	VM[2:0] = 101b	4.55	4.64	4.74[25]	V	
V_{LVD6}	VM[2:0] = 110b	4.63	4.73	4.82	V	
V_{LVD7}	VM[2:0] = 111b	4.72	4.81	4.91	V	

Notes
23. Errata: When V_{DD} of the device is pulled below ground just before power on, the first read from each 8K Flash page may be corrupted. This issue does not affect Flash page 0 because it is the selected page upon reset. More details in "Errata" on page 66.
24. Always greater than 50 mV above PPOR (PORLEV = 00) for falling supply.
25. Always greater than 50 mV above PPOR (PORLEV = 10) for falling supply.

11.3.10 DC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 23. DC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DDP}	V_{DD} for programming and erase	4.5	5	5.5	V	This specification applies to the functional requirements of external programmer tools
V_{DDLV}	Low V_{DD} for verify	3	3.1	3.2	V	This specification applies to the functional requirements of external programmer tools
V_{DDHV}	High V_{DD} for verify	5.1	5.2	5.3	V	This specification applies to the functional requirements of external programmer tools
$V_{DDIWRITE}$	Supply voltage for flash write operation	3		5.25	V	This specification applies to this device when it is executing internal flash writes
I_{DDP}	Supply current during programming or verify	–	15	30	mA	
V_{ILP}	Input low voltage during programming or verify	–	–	0.8	V	
V_{IHP}	Input high voltage during programming or verify	2.1	–	–	V	
I_{ILP}	Input current when applying V_{ILP} to P1[0] or P1[1] during programming or verify	–	–	0.2	mA	Driving internal pull-down resistor.
I_{IHP}	Input current when applying V_{IHP} to P1[0] or P1[1] during programming or verify	–	–	1.5	mA	Driving internal pull-down resistor.
V_{OLV}	Output low voltage during programming or verify	–	–	V_{SS} + 0.75	V	
V_{OHV}	Output high voltage during programming or verify	V_{DD} – 1.0	–	V_{DD}	V	
$Flash_{ENPB}$	Flash endurance (per block)[26]	50,000	–	–	–	Erase/write cycles per block.
$Flash_{ENT}$	Flash endurance (total)[27]	1,800,000	–	–	–	Erase/write cycles.
$Flash_{DR}$	Flash data retention	10	–	–	Years	

11.3.11 DC I²C Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 24. DC I²C Specifications[28]

Symbol	Description	Min	Typ	Max	Units	Notes
V_{ILI2C}	Input low level	–	–	0.3 × V_{DD}	V	3.0 V ≤ V_{DD} ≤ 3.6 V
		–	–	0.25 × V_{DD}	V	4.75 V ≤ V_{DD} ≤ 5.25 V
V_{IHI2C}	Input high level	0.7 × V_{DD}	–	–	V	3.0 V ≤ V_{DD} ≤ 5.25 V

Table 25. AC Chip Level Specifications *(continued)*

Symbol	Description	Min	Typ	Max	Units	Notes
$t_{POWERUP}$	Time from end of POR to CPU executing code	–	16	100	ms	Power-up from 0 V. See the System Resets section of the PSoC Technical Reference Manual.
t_{jit_IMO}[32]	24 MHz IMO cycle-to-cycle jitter (RMS)	–	200	1200	ps	
	24 MHz IMO long term N cycle-to-cycle jitter (RMS)	–	900	6000	ps	N=32
	24 MHz IMO period jitter (RMS)	–	200	900	ps	

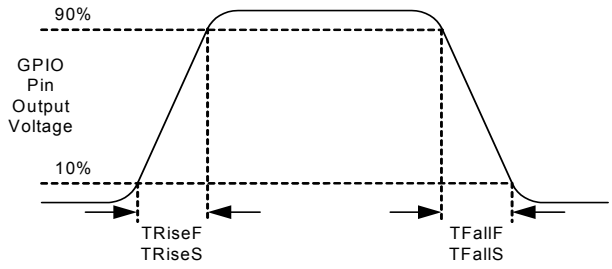
11.4.2 AC GPIO Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 26. AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO operating frequency	0	–	12	MHz	Normal strong mode
t_{RiseF}	Rise time, normal strong mode, Cload = 50 pF	3	–	18	ns	V_{DD} = 4.5 to 5.25 V, 10% to 90%
t_{FallF}	Fall time, normal strong mode, Cload = 50 pF	2	–	18	ns	V_{DD} = 4.5 to 5.25 V, 10% to 90%
t_{RiseS}	Rise time, slow strong mode, Cload = 50 pF	10	27	–	ns	V_{DD} = 3 to 5.25 V, 10% to 90%
t_{FallS}	Fall time, slow strong mode, Cload = 50 pF	10	22	–	ns	V_{DD} = 3 to 5.25 V, 10% to 90%

Figure 12. GPIO Timing Diagram



Notes
29. 4.75 V < V_{DD} < 5.25 V.
30. 3.0 V < V_{DD} < 3.6 V. See application note Adjusting PSoC® Trims for 3.3 V and 2.7 V Operation – AN2012 for information on trimming for operation at 3.3 V.
31. See the individual user module datasheets for information on maximum frequencies for user modules.
32. Refer to Cypress Jitter Specifications application note, Understanding Datasheet Jitter Specifications for Cypress Timing Products – AN5054 for more information.

11.5 Thermal Impedance

Table 37. Thermal Impedances per Package

Package	Typical θ_{JA} [36]
56-Pin QFN[37]	12.93 °C/W
68-Pin QFN[37]	13.05 °C/W
100-Ball VFBGA	65 °C/W
100-Pin TQFP	51 °C/W

11.6 Solder Reflow Peak Specifications

Table 38 shows the solder reflow temperature limits that must not be exceeded.

Table 38. Solder Reflow Specifications

Package	Maximum Peak Temperature (T_C)	Maximum Time above T_C – 5 °C
56-Pin QFN	260 °C	30 seconds
68-Pin QFN	260 °C	30 seconds
100-Ball VFBGA	260 °C	30 seconds
100-Pin TQFP	260 °C	30 seconds

Notes
36. $T_J = T_A + POWER \times \theta_{JA}$.
37. To achieve the thermal impedance specified for the QFN package, see the *Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages* available at http://www.amkor.com.

12. Development Tool Selection

12.1 Software

12.1.1 PSoC Designer

At the core of the PSoC development software suite is PSoC Designer, used to generate PSoC firmware applications. PSoC Designer is available free of charge at http://www.cypress.com and includes a free C compiler.

12.1.2 PSoC Programmer

Flexible enough to be used on the bench in development, yet suitable for factory programming, PSoC Programmer works either as a standalone programming application or it can operate directly from PSoC Designer. PSoC Programmer software is compatible with both PSoC ICE-Cube in-circuit emulator and PSoC MiniProg. PSoC programmer is available free of charge at http://www.cypress.com.

12.2 Development Kits

All development kits can be purchased from the Cypress Online Store.

12.2.1 CY3215-DK Basic Development Kit

The CY3215-DK is for prototyping and development with PSoC Designer. This kit supports in-circuit emulation, and the software interface enables you to run, halt, and single step the processor, and view the content of specific memory locations. Advance emulation features are also supported through PSoC Designer. The kit includes:

- PSoC Designer software CD
- ICE-Cube in-circuit Emulator
- ICE Flex-Pod for CY8C29x66 family
- Cat-5 adapter
- MiniEval programming board
- 110 ~ 240 V power supply, Euro-Plug adapter
- iMAGEcraft C compiler (registration required)
- ISSP cable
- USB 2.0 cable and Blue Cat-5 cable
- Two CY8C29466-24PXI 28-PDIP chip samples

12.3 Evaluation Tools

All evaluation tools can be purchased from the Cypress Online Store.

12.3.1 CY3210-MiniProg1

The CY3210-MiniProg1 kit enables you to program PSoC devices via the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC via a provided USB 2.0 cable. The kit includes:

- MiniProg programming unit
- MiniEval socket programming and evaluation board
- 28-Pin CY8C29466-24PXI PDIP PSoC device sample
- 28-Pin CY8C27443-24PXI PDIP PSoC device sample
- PSoC Designer software CD
- Getting Started guide
- USB 2.0 cable

12.3.2 CY3210-PSoCEval1

The CY3210-PSoCEval1 kit features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, and plenty of bread-boarding space to meet all of your evaluation needs. The kit includes:

- Evaluation board with LCD module
- MiniProg programming unit
- 28-Pin CY8C29466-24PXI PDIP PSoC device sample (2)
- PSoC Designer software CD
- Getting Started guide
- USB 2.0 cable

12.3.3 CY3214-PSoCEvalUSB

The CY3214-PSoCEvalUSB evaluation kit features a development board for the CY8C24794-24LTXI PSoC device. The board supports both USB and capacitive sensing development and debugging support. This evaluation board also includes an LCD module, potentiometer, LEDs, an enunciator and plenty of breadboarding space to meet all of your evaluation needs. The kit includes:

- PSoCEvalUSB board
- LCD module
- MIniProg programming unit
- Mini USB cable
- PSoC Designer and Example Projects CD
- Getting Started guide
- Wire pack

12.4 Device Programmers

All device programmers can be purchased from the Cypress Online Store.

12.4.1 CY3216 Modular Programmer

The CY3216 Modular Programmer kit features a modular programmer and the MiniProg1 programming unit. The modular programmer includes three programming module cards and supports multiple Cypress products. The kit includes:

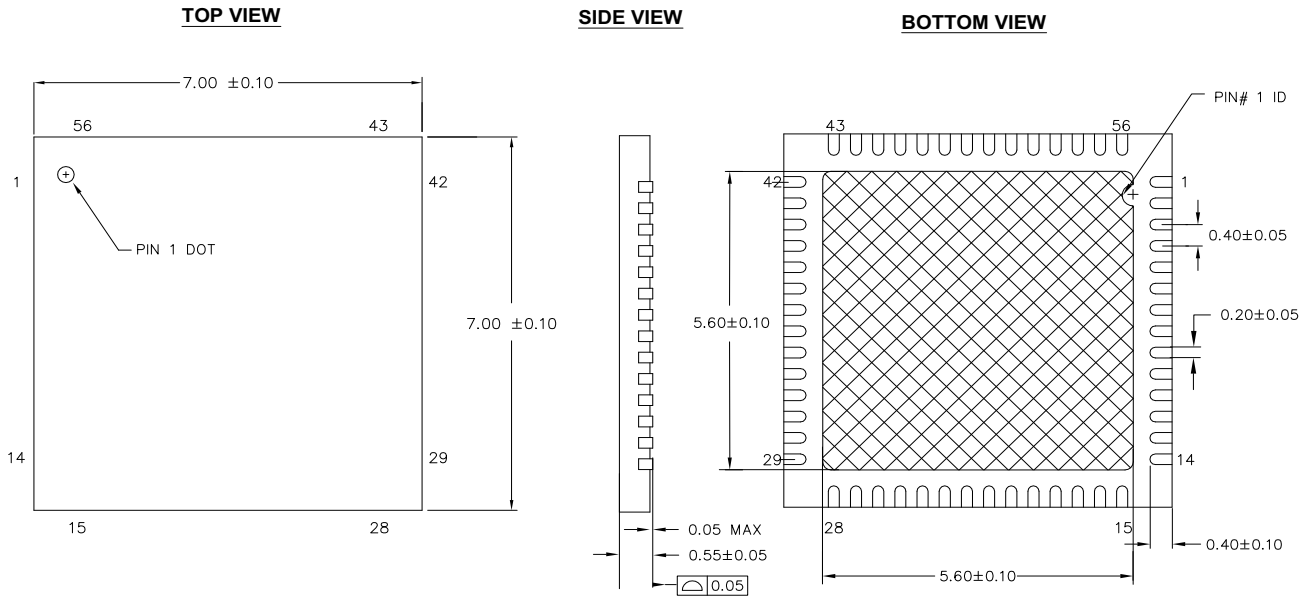
- Modular programmer base
- Three programming module cards
- MiniProg programming unit
- PSoC Designer software CD

14. Packaging Dimensions

This section illustrates the package specification for the CY8C24x94 PSoC devices, along with the thermal impedance for the package and solder reflow peak temperatures.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the emulator pod dimension drawings at http://www.cypress.com/design/MR10161.

Figure 16. 56-pin QFN (7 × 7 × 0.6 mm) LR56A/LQ56A 5.6 × 5.6 E-Pad (Sawn) Package Outline, 001-58740

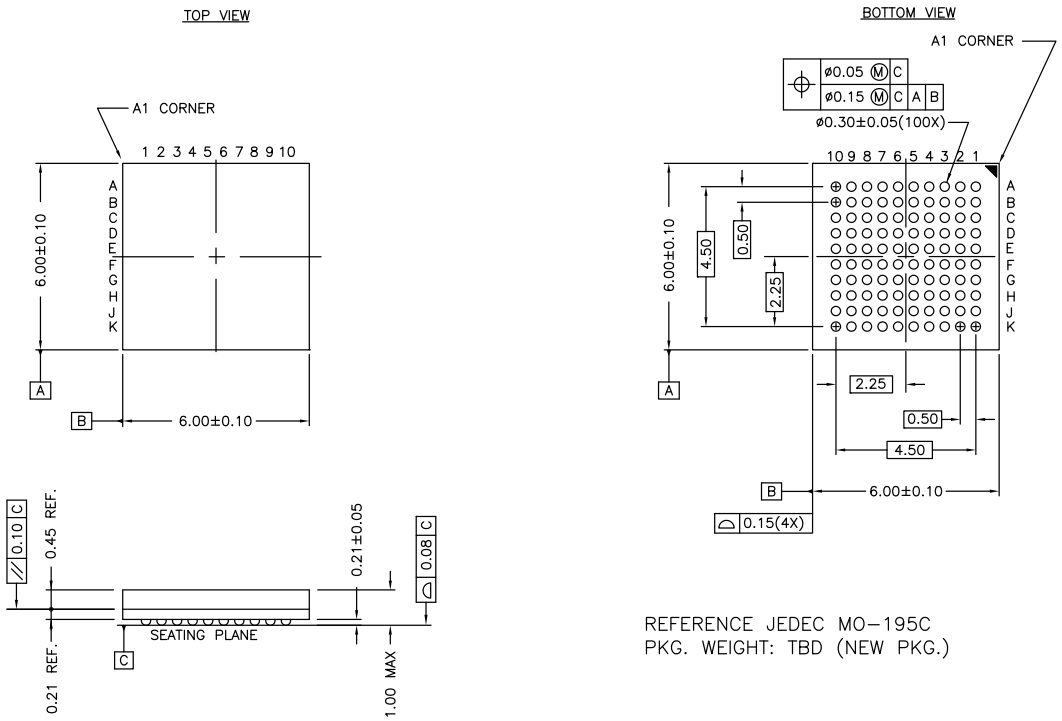


NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. BASED ON REF JEDEC # MO-248
3. ALL DIMENSIONS ARE IN MILLIMETERS

001-58740 *C

Figure 20. 100-ball VFBGA (6 × 6 × 1.0 mm) BZ100 Package Outline, 51-85209



15. Acronyms

15.1 Acronyms Used

The following table lists the acronyms that are used in this document.

Acronym	Description	Acronym	Description
AC	alternating current	MIPS	million instructions per second
ADC	analog-to-digital converter	OCD	on-chip debug
API	application programming interface	PCB	printed circuit board
CMOS	complementary metal oxide semiconductor	PDIP	plastic dual-in-line package
CPU	central processing unit	PGA	programmable gain amplifier
CRC	cyclic redundancy check	POR	power-on reset
CT	continuous time	PPOR	precision power-on reset
DAC	digital-to-analog converter	PRS	pseudo-random sequence
DC	direct current	PSoC®	Programmable System-on-Chip™
DTMF	dual-tone multi-frequency	PWM	pulse-width modulator
EEPROM	electrically erasable programmable read-only memory	QFN	quad flat no leads
GPIO	general purpose I/O	SAR	successive approximation register
ICE	in-circuit emulator	SC	switched capacitor
IDE	integrated development environment	SLIMO	slow IMO
ILO	internal low-speed oscillator	SOIC	small-outline integrated circuit
IMO	internal main oscillator	SPI™	serial peripheral interface
I/O	input/output	SRAM	static random-access memory
IrDA	infrared data association	SROM	supervisory read-only memory
ISSP	In-System Serial Programming	TQFP	thin quad flat pack
LCD	liquid crystal display	UART	universal asynchronous receiver / transmitter
LED	light-emitting diode	USB	universal serial bus
LPC	low power comparator	VFBGA	very fine-pitch ball grid array
LVD	low-voltage detect	WDT	watchdog timer
MAC	multiply-accumulate	XRES	external reset
MCU	microcontroller unit		

16. Document Conventions

16.1 Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
°C	degree Celsius	mV	millivolt
dB	decibels	nA	nanoampere
fF	femtofarad	ns	nanosecond
kHz	kilohertz	nV	nanovolt
kΩ	kilohms	Ω	ohms
MHz	megahertz	pA	picoampere
µA	microampere	pF	picofarad
µs	microsecond	ps	picosecond
µV	microvolt	%	percent
mA	milliampere	rt-Hz	root hertz
mm	millimeter	V	volt
ms	millisecond	W	watt

16.2 Numeric Conventions

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexadecimal numbers may also be represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (for example, ‘01010100b’ or ‘01000011b’). Numbers not indicated by an ‘h’ or ‘b’ are decimal.

17. Glossary

active high	6. A logic signal having its asserted state as the logic 1 state. 7. A logic signal having the logic 1 state as the higher voltage of the two states.
analog blocks	The basic programmable opamp circuits. These are SC (switched capacitor) and CT (continuous time) blocks. These blocks can be interconnected to provide ADCs, DACs, multi-pole filters, gain stages, and much more.
analog-to-digital (ADC)	A device that changes an analog signal to a digital signal of corresponding magnitude. Typically, an ADC converts a voltage to a digital number. The digital-to-analog (DAC) converter performs the reverse operation.
API (Application Programming Interface)	A series of software routines that comprise an interface between a computer application and lower level services and functions (for example, user modules and libraries). APIs serve as building blocks for programmers that create software applications.
asynchronous	A signal whose data is acknowledged or acted upon immediately, irrespective of any clock signal.
Bandgap reference	A stable voltage reference design that matches the positive temperature coefficient of VT with the negative temperature coefficient of VBE, to produce a zero temperature coefficient (ideally) reference.
bandwidth	1. The frequency range of a message or information processing system measured in hertz. 2. The width of the spectral region over which an amplifier (or absorber) has substantial gain (or loss); it is sometimes represented more specifically as, for example, full width at half maximum.
bias	1. A systematic deviation of a value from a reference value. 2. The amount by which the average of a set of values departs from a reference value. 3. The electrical, mechanical, magnetic, or other force (field) applied to a device to establish a reference level to operate the device.

17. Glossary *(continued)*

SRAM	An acronym for static random access memory. A memory device allowing users to store and retrieve data at a high rate of speed. The term static is used because, after a value has been loaded into an SRAM cell, it remains unchanged until it is explicitly altered or until power is removed from the device.
SROM	An acronym for supervisory read only memory. The SROM holds code that is used to boot the device, calibrate circuitry, and perform Flash operations. The functions of the SROM may be accessed in normal user code, operating from Flash.
stop bit	A signal following a character or block that prepares the receiving device to receive the next character or block.
synchronous	1. A signal whose data is not acknowledged or acted upon until the next active edge of a clock signal. 2. A system whose operation is synchronized by a clock signal.
tristate	A function whose output can adopt three states: 0, 1, and Z (high-impedance). The function does not drive any value in the Z state and, in many respects, may be considered to be disconnected from the rest of the circuit, allowing another output to drive the same net.
UART	A UART or universal asynchronous receiver-transmitter translates between parallel bits of data and serial bits.
user modules	Pre-build, pre-tested hardware/firmware peripheral functions that take care of managing and configuring the lower level Analog and Digital PSoC Blocks. User Modules also provide high level ***API (Application Programming Interface)*** for the peripheral function.
user space	The bank 0 space of the register map. The registers in this bank are more likely to be modified during normal program execution and not just during initialization. Registers in bank 1 are most likely to be modified only during the initialization phase of the program.
V_{DD}	A name for a power net meaning "voltage drain." The most positive power supply signal. Usually 5 V or 3.3 V.
V_{SS}	A name for a power net meaning "voltage source." The most negative power supply signal.
watchdog timer	A timer that must be serviced periodically. If it is not serviced, the CPU resets after a specified period of time.

When Vdd is pulled below ground before power on, an internal Flash reference may deviate from its nominal voltage. The reference deviation tends to result in the first Flash read from that page returning 0xFF. During the first read from each page, the reference is reset resulting in all future reads returning the correct value. A short delay of 5 µs before the first real read provides time for the reference voltage to stabilize.

■ **WORKAROUND**

To prevent an invalid Flash read, a dummy read from each Flash page must occur before use of the pages. A delay of 5 µs must occur after the dummy read and before a real read. The dummy reads occurs as soon as possible and must be located in Flash page 0 before a read from any other Flash page. An example for reading a byte of memory from each Flash page is listed below. Placed it in boot.tpl and boot.asm immediately after the ‘start:’ label.

```
// dummy read from each 8K Flash page
// page 1
mov  A, 0x20        // MSB
mov  X, 0x00        // LSB
romx
// wait at least 5 µs
mov  X, 14
loop1:
dec  X
jnz  loop1
```

19. Document History Page

Document Title: CY8C24094/CY8C24794/CY8C24894/CY8C24994, PSoC® Programmable System-on-Chip™ Document Number: 38-12018				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	133189	NWJ	01/27/2004	New silicon and new document – Advance datasheet.
*A	251672	SFV	See ECN	First Preliminary datasheet. Changed title to encompass only the CY8C24794 because the CY8C24494 and CY8C24694 are not being offered by Cypress.
*B	289742	HMT	See ECN	Add standard DS items from SFV memo. Add Analog Input Mux on pinouts. 2 MACs. Change 512 bytes of SRAM to 1 K. Add dimension key to package. Remove HAPI. Update diagrams, registers and specs.
*C	335236	HMT	See ECN	Add CY logo. Update CY copyright. Update new CY.com URLs. Re-add ISSP programming pinout notation. Add Reflow Temp. table. Update features (MAC, Oscillator, and voltage range), registers (INT_CLR2/MSK2, second MAC), and specs. (Rext, IMO, analog output buffer...).
*D	344318	HMT	See ECN	Add new color and logo. Expand analog arch. diagram. Fix I/O #. Update Electrical Specifications.
*E	346774	HMT	See ECN	Add USB temperature specifications. Make datasheet Final.
*F	349566	HMT	See ECN	Remove USB logo. Add URL to preferred dimensions for mounting MLF packages.
*G	393164	HMT	See ECN	Add new device, CY8C24894 56-pin MLF with XRES pin. Add Fimousb3v char. to specs. Upgrade to CY Perform logo and update corporate address and copyright.
*H	469243	HMT	See ECN	Add ISSP note to pinout tables. Update typical and recommended Storage Temperature per industrial specs. Update Low Output Level maximum I/OL budget. Add FLS_PR1 to Register Map Bank 1 for users to specify which Flash bank should be used for SROM operations. Add two new devices for a 68-pin QFN and 100-ball VFBGA under RPNs: CY8C24094 and CY8C24994. Add two packages for 68-pin QFN. Add OCD non-production pinouts and package diagrams. Update CY branding and QFN convention. Add new Dev. Tool section. Update copyright and trademarks.
*I	561158	HMT	See ECN	Add Low Power Comparator (LPC) AC/DC electrical spec. tables. Add CY8C20x34 to PSoC Device Characteristics table. Add detailed dimensions to 56-pin QFN package diagram and update revision. Secure one package diagram/manufacturing per QFN. Update emulation pod/feet kit part numbers. Fix pinout type-o per TestTrack.
*J	728238	HMT	See ECN	Add CapSense SNR requirement reference. Update figure standards. Update Technical Training paragraphs. Add QFN package clarifications and dimensions. Update ECN-ed Amkor dimensioned QFN package diagram revisions. Reword SNR reference. Add new 56-pin QFN spec.
*K	2552459	AZIE / PYRS	08/14/08	Add footnote on AGND descriptions to avoid using P2[4] for digital signaling as it may add noise to AGND. Remove reference to CMP_GO_EN1 in Map Bank 1 Table on Address 65; this register has no functionality on 24xxx. Add footnote on die sales. Add description 'Optional External Clock Input' on P1[4] to match description of P1[4].
*L	2616550	OGNE / PYRS	12/05/08	Updated Programmable Pin Configuration detail. Changed title from PSoC® Mixed-Signal Array to PSoC® Programmable System-on-Chip™
*M	2657956	DPT / PYRS	02/11/09	Added package diagram 001-09618 and updated Ordering Information table

19. Document History Page *(continued)*

Document Title: CY8C24094/CY8C24794/CY8C24894/CY8C24994, PSoC® Programmable System-on-Chip™ Document Number: 38-12018				
AD	3503402	PMAD	01/20/2012	Updated V_{OH} and V_{OL} section in Table 12.
AE	3545509	PSAI	03/08/2012	Updated link to 'Technical reference Manual'.
AF	3862667	CSAI	01/09/2013	Updated Ordering Information (Updated part numbers). Updated Packaging Dimensions: spec 001-53450 – Changed revision from *B to *C. spec 001-09618 – Changed revision from *D to *E. spec 51-85048 – Changed revision from *E to *G.
AG	3979302	CSAI	04/23/2013	Updated Packaging Dimensions: spec 001-58740 – Changed revision from ** to *A. Added Errata.
AH	4074544	CSAI	07/23/2013	Added Errata Footnotes (Note 21, 23) Updated Electrical Specifications: Updated DC Electrical Characteristics: Updated DC Chip-Level Specifications: Added Note 21 and referred the same note in “Sleep Mode” in description of I_{SB} parameter in Table 11. Updated DC POR and LVD Specifications: Added Note 23 and referred the same note in V_{PPOR0}, V_{PPOR1}, V_{PPOR2} parameters in Table 22. Updated to new template.
AI	4596835	DIMA	12/15/2014	Updated Pin Information: Updated 56-Pin Part Pinout: Updated Table 2: Added Note 5 and referred the same note in description of pin 19 and pin 50. Updated 56-Pin Part Pinout (with XRES): Updated Table 3: Added Note 8 and referred the same note in description of pin 19 and pin 50. Updated 68-Pin Part Pinout: Updated Table 4: Added Note 10 and referred the same note in description of pin 7, pin 20 and pin 60. Updated 68-Pin Part Pinout (On-Chip Debug): Updated Table 5: Added Note 13 and referred the same note in description of pin 7, pin 20 and pin 60. Updated 100-Ball VFBGA Part Pinout: Updated Table 6: Added Note 15 and referred the same note in caption of Table 6. Updated 100-Ball VFBGA Part Pinout (On-Chip Debug): Updated Table 7: Added Note 17 and referred the same note in caption of Table 7. Updated 100-Pin Part Pinout (On-Chip Debug): Updated Table 8: Added Note 19 and referred the same note in caption of Table 8. Updated Packaging Dimensions: spec 001-12921 – Changed revision from *B to *C. spec 001-53450 – Changed revision from *C to *D. spec 51-85209 – Changed revision from *D to *E. spec 51-85048 – Changed revision from *G to *I. Completing Sunset Review.
AJ	4622083	SLAN	01/13/2015	Added More Information section.
AK	4684565	PSI	03/12/2015	Updated Packaging Dimensions: spec 001-58740 – Changed revision from *A to *B. Updated Errata.
AL	5699855	AESATP12	04/20/2017	Updated logo and copyright.