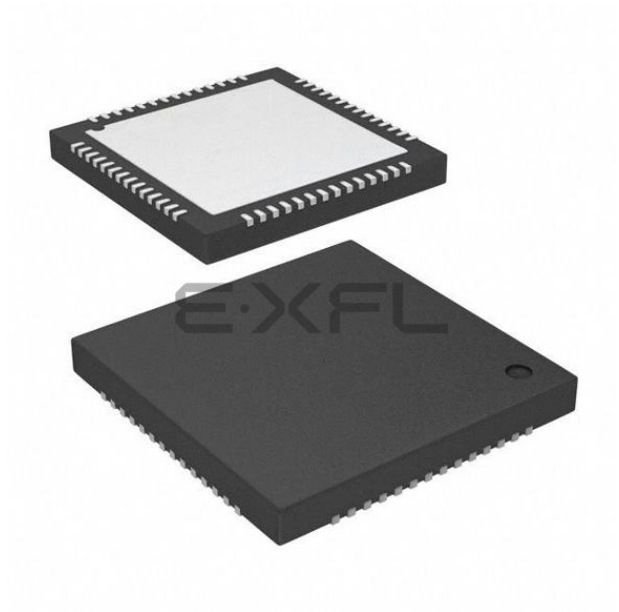

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SPI, UART/USART, USB
Peripherals	POR, PWM, WDT
Number of I/O	50
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	A/D 48x14b; D/A 2x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	56-UFQFN Exposed Pad
Supplier Device Package	56-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c24794-24lqxit

read and write data memory, and read and write I/O registers. You can read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows you to create a trace buffer of registers and memory locations of interest.

7.1.4 Online Help System

The online help system displays online, context-sensitive help. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an online support forum to aid the designer.

7.1.5 In-Circuit Emulator

A low-cost, high-functionality In-Circuit Emulator (ICE) is available for development support. This hardware can program single devices.

The emulator consists of a base unit that connects to the PC using a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full speed (24-MHz) operation.

8. Designing with PSoC Designer

The development process for the PSoC® device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PSoC Blocks, have the ability to implement a wide variety of user-selectable functions. The PSoC development process is summarized in four steps:

1. Select User Modules
2. Configure User Modules
3. Organize and Connect
4. Generate, Verify, and Debug

8.1 Select User Modules

PSoC Designer provides a library of prebuilt, pretested hardware peripheral components called “user modules.” User modules make selecting and implementing peripheral devices, both analog and digital, simple.

8.2 Configure User Modules

Each user module that you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a PWM User Module configures one or more digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit you to establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These user module datasheets explain the internal operation of the user module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information you may need to successfully implement your design.

8.3 Organize and Connect

You build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. You perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

8.4 Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, you perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides application programming interfaces (APIs) with high-level functions to control and respond to hardware events at run time and interrupt service routines that you can adapt as needed.

A complete code development environment allows you to develop and customize your applications in either C, assembly language, or both.

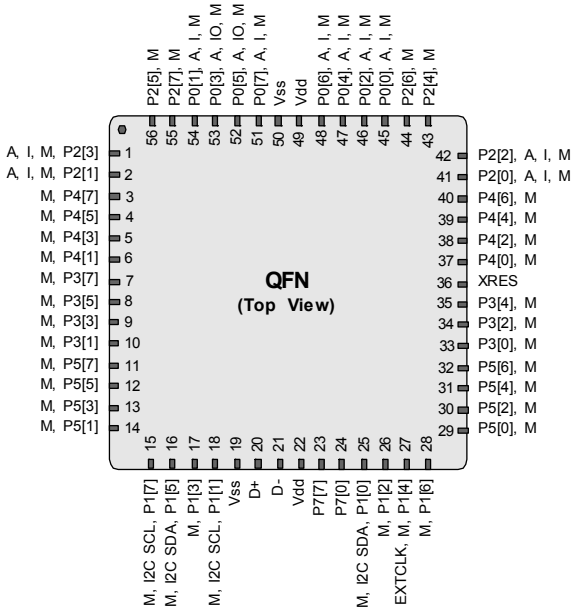
The last step in the development process takes place inside PSoC Designer’s debugger (access by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint, and watch-variable features, the debug interface provides a large trace buffer and allows you to define complex breakpoint events. These include monitoring address and data bus values, memory locations and external signals.

9.2 56-Pin Part Pinout (with XRES)

Table 3. 56-Pin Part Pinout (QFN[6])

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I, M	P2[3]	Direct switched capacitor block input
2	I/O	I, M	P2[1]	Direct switched capacitor block input
3	I/O	M	P4[7]	
4	I/O	M	P4[5]	
5	I/O	M	P4[3]	
6	I/O	M	P4[1]	
7	I/O	M	P3[7]	
8	I/O	M	P3[5]	
9	I/O	M	P3[3]	
10	I/O	M	P3[1]	
11	I/O	M	P5[7]	
12	I/O	M	P5[5]	
13	I/O	M	P5[3]	
14	I/O	M	P5[1]	
15	I/O	M	P1[7]	I^2C SCL
16	I/O	M	P1[5]	I^2C SDA
17	I/O	M	P1[3]	
18	I/O	M	P1[1]	I^2C SCL, ISSP SCLK [7]
19	Power		V_{SS}	Ground connection [8]
20	USB		D+	
21	USB		D–	
22	Power		V_{DD}	Supply voltage
23	I/O		P7[7]	
24	I/O		P7[0]	
25	I/O	M	P1[0]	I^2C SDA, ISSP SDATA[7]
26	I/O	M	P1[2]	
27	I/O	M	P1[4]	Optional EXTCLK
28	I/O	M	P1[6]	
29	I/O	M	P5[0]	
30	I/O	M	P5[2]	
31	I/O	M	P5[4]	
32	I/O	M	P5[6]	
33	I/O	M	P3[0]	
34	I/O	M	P3[2]	
35	I/O	M	P3[4]	
36	Input		XRES	Active high external reset with internal pull-down
37	I/O	M	P4[0]	
38	I/O	M	P4[2]	
39	I/O	M	P4[4]	
40	I/O	M	P4[6]	
41	I/O	I, M	P2[0]	Direct switched capacitor block input
42	I/O	I, M	P2[2]	Direct switched capacitor block input
43	I/O	M	P2[4]	External AGND input
44	I/O	M	P2[6]	External VREF input
45	I/O	I, M	P0[0]	Analog column mux input
46	I/O	I, M	P0[2]	Analog column mux input
47	I/O	I, M	P0[4]	Analog column mux input VREF
48	I/O	I, M	P0[6]	Analog column mux input
49	Power		V_{DD}	Supply voltage
50	Power		V_{SS}	Ground connection [8]
51	I/O	I, M	P0[7]	Analog column mux input
52	I/O	I/O, M	P0[5]	Analog column mux input and column output
53	I/O	I/O, M	P0[3]	Analog column mux input and column output
54	I/O	I, M	P0[1]	Analog column mux input
55	I/O	M	P2[7]	
56	I/O	M	P2[5]	

Figure 5. CY8C24894 56-Pin PSoC Device



LEGEND A = Analog, I = Input, O = Output, and M = Analog Mux Input.

Notes
6. The center pad on the QFN package should be connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it should be electrically floated and not connected to any other signal.
7. These are the ISSP pins, which are not High Z at POR. See the PSoC Technical Reference Manual for details.
8. All V_{SS} pins should be brought out to one common GND plane.

9.6 100-Ball VFBGA Part Pinout (On-Chip Debug)

The following 100-pin VFBGA part table and drawing is for the CY8C24094 OCD PSoC device.

Note This part is only used for in-circuit debugging. It is NOT available for production.

Table 7. 100-Ball Part Pinout (VFBGA[17])

Pin No.	Digital	Analog	Name	Description	Pin No.	Digital	Analog	Name	Description
A1	Power		V_{SS}	Ground connection	F1			OCDE	OCD even data I/O
A2	Power		V_{SS}	Ground connection	F2	I/O	M	P5[7]	
A3			NC	No connection. Pin must be left floating	F3	I/O	M	P3[5]	
A4			NC	No connection. Pin must be left floating	F4	I/O	M	P5[1]	
A5			NC	No connection. Pin must be left floating.	F5	Power		V_{SS}	Ground connection
A6	Power		V_{DD}	Supply voltage.	F6	Power		V_{SS}	Ground connection
A7			NC	No connection. Pin must be left floating.	F7	I/O	M	P5[0]	
A8			NC	No connection. Pin must be left floating.	F8	I/O	M	P3[0]	
A9	Power		V_{SS}	Ground connection	F9			XRES	Active high pin reset with internal pull-down
A10	Power		V_{SS}	Ground connection	F10	I/O		P7[1]	
B1	Power		V_{SS}	Ground connection	G1			OCDO	OCD odd data output
B2	Power		V_{SS}	Ground connection	G2	I/O	M	P5[5]	
B3	I/O	I, M	P2[1]	Direct switched capacitor block input	G3	I/O	M	P3[3]	
B4	I/O	I, M	P0[1]	Analog column mux input	G4	I/O	M	P1[7]	I^2C SCL
B5	I/O	I, M	P0[7]	Analog column mux input	G5	I/O	M	P1[1]	I^2C SCL, ISSP SCLK[18]
B6	Power		V_{DD}	Supply voltage	G6	I/O	M	P1[0]	I^2C SDA, ISSP SDATA[18]
B7	I/O	I, M	P0[2]	Analog column mux input	G7	I/O	M	P1[6]	
B8	I/O	I, M	P2[2]	Direct switched capacitor block input	G8	I/O	M	P3[4]	
B9	Power		V_{SS}	Ground connection	G9	I/O	M	P5[6]	
B10	Power		V_{SS}	Ground connection	G10	I/O		P7[2]	
C1			NC	No connection. Pin must be left floating	H1			NC	No connection. Pin must be left floating
C2	I/O	M	P4[1]		H2	I/O	M	P5[3]	
C3	I/O	M	P4[7]		H3	I/O	M	P3[1]	
C4	I/O	M	P2[7]		H4	I/O	M	P1[5]	I^2C SDA
C5	I/O	I/O,M	P0[5]	Analog column mux input and column output	H5	I/O	M	P1[3]	
C6	I/O	I, M	P0[6]	Analog column mux input	H6	I/O	M	P1[2]	
C7	I/O	I, M	P0[0]	Analog column mux input	H7	I/O	M	P1[4]	Optional EXTCLK
C8	I/O	I, M	P2[0]	Direct switched capacitor block input	H8	I/O	M	P3[2]	
C9	I/O	M	P4[2]		H9	I/O	M	P5[4]	
C10			NC	No connection. Pin must be left floating	H10	I/O		P7[3]	
D1			NC	No connection. Pin must be left floating	J1	Power		V_{SS}	Ground connection
D2	I/O	M	P3[7]		J2	Power		V_{SS}	Ground connection
D3	I/O	M	P4[5]		J3	USB		D+	
D4	I/O	M	P2[5]		J4	USB		D-	
D5	I/O	I/O, M	P0[3]	Analog column mux input and column output	J5	Power		V_{DD}	Supply voltage
D6	I/O	I, M	P0[4]	Analog column mux input	J6	I/O		P7[7]	
D7	I/O	M	P2[6]	External VREF input	J7	I/O		P7[0]	
D8	I/O	M	P4[6]		J8	I/O	M	P5[2]	
D9	I/O	M	P4[0]		J9	Power		V_{SS}	Ground connection
D10			CCLK	OCD CPU clock output	J10	Power		V_{SS}	Ground connection
E1			NC	No connection. Pin must be left floating	K1	Power		V_{SS}	Ground connection
E2			NC	No connection. Pin must be left floating	K2	Power		V_{SS}	Ground connection
E3	I/O	M	P4[3]		K3			NC	No connection. Pin must be left floating
E4	I/O	I, M	P2[3]	Direct switched capacitor block input	K4			NC	No connection. Pin must be left floating
E5	Power		V_{SS}	Ground connection	K5	Power		V_{DD}	Supply voltage
E6	Power		V_{SS}	Ground connection	K6	I/O		P7[6]	
E7	I/O	M	P2[4]	External AGND input	K7	I/O		P7[5]	
E8	I/O	M	P4[4]		K8	I/O		P7[4]	
E9	I/O	M	P3[6]		K9	Power		V_{SS}	Ground connection
E10			HCLK	OCD high speed clock output	K10	Power		V_{SS}	Ground connection

LEGEND A = Analog, I = Input, O = Output, M = Analog Mux Input, NC = No connection. Pin must be left floating, OCD = On-Chip Debugger.

Notes

17. All V_{SS} pins should be brought out to one common GND plane.
18. These are the ISSP pins, which are not High Z at POR. See the PSoC Technical Reference Manual for details.

11.3.3 DC Full Speed USB Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –10 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –10 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 13. DC Full Speed (12 Mbps) USB Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
USB Interface						
V_{DI}	Differential input sensitivity	0.2	–	–	V	| (D+) – (D–) |
V_{CM}	Differential input common mode range	0.8	–	2.5	V	
V_{SE}	Single ended receiver threshold	0.8	–	2.0	V	
C_{IN}	Transceiver capacitance	–	–	20	pF	
$I_{I/O}$	High Z state data line leakage	–10	–	10	µA	0 V < V_{IN} < 3.3 V.
R_{EXT}	External USB series resistor	23	–	25	Ω	In series with each USB pin.
V_{UOH}	Static output high, driven	2.8	–	3.6	V	15 kΩ ± 5% to ground. Internal pull-up enabled.
V_{UOHI}	Static output high, idle	2.7	–	3.6	V	15 kΩ ± 5% to ground. Internal pull-up enabled.
V_{UOL}	Static output low	–	–	0.3	V	15 kΩ ± 5% to ground. Internal pull-up enabled.
Z_O	USB driver output impedance	28	–	44	Ω	Including R_{EXT} resistor.
V_{CRS}	D+/D– crossover voltage	1.3	–	2.0	V	

11.3.4 DC Operational Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V and 3.3 V at 25 °C and are for design guidance only.

The operational amplifier is a component of both the analog continuous time PSoC blocks and the analog switched capacitor PSoC blocks. The guaranteed specifications are measured in the analog continuous time PSoC block.

Table 14. 5-V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input offset voltage (absolute value) Power = low, Opamp bias = high Power = medium, Opamp bias = high Power = high, Opamp bias = high	 – – –	 1.6 1.3 1.2	 10 8 7.5	 mV mV mV	
TCV_{OSOA}	Average input offset voltage drift	–	7.0	35.0	µV/°C	
I_{EBOA}	Input leakage current (Port 0 analog pins)	–	20	–	pA	Gross tested to 1 µA.
C_{INOA}	Input capacitance (Port 0 analog pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25 °C.
V_{CMOA}	Common mode voltage range Common mode voltage range (high power or high Opamp bias)	0.0 0.5	– –	V_{DD} V_{DD} – 0.5	V V	The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
G_{OLOA}	Open loop gain Power = low, Opamp bias = high Power = medium, Opamp bias = high Power = high, Opamp bias = high	 60 60 80	 – – –	 – – –	 dB dB dB	
$V_{OHIGHOA}$	High output voltage swing (internal signals) Power = low, Opamp bias = high Power = medium, Opamp bias = high Power = high, Opamp bias = high	 V_{DD} – 0.2 V_{DD} – 0.2 V_{DD} – 0.5	 – – –	 – – –	 V V V	
V_{OLOWOA}	Low output voltage swing (internal signals) Power = low, Opamp bias = high Power = medium, Opamp bias = high Power = high, Opamp bias = high	 – – –	 – – –	 0.2 0.2 0.5	 V V V	
I_{SOA}	Supply current (including associated AGND buffer) Power = low, Opamp bias = low Power = low, Opamp bias = high Power = medium, Opamp bias = low Power = medium, Opamp bias = high Power = high, Opamp bias = low Power = high, Opamp bias = high	 – – – – – –	 400 500 800 1200 2400 4600	 800 900 1000 1600 3200 6400	 µA µA µA µA µA µA	
$PSRR_{OA}$	Supply voltage rejection ratio	65	80	–	dB	$V_{SS} \le V_{IN} \le (V_{DD} – 2.25)$ or $(V_{DD} – 1.25\ V) \le V_{IN} \le V_{DD}$.

11.3.6 DC Analog Output Buffer Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 17. 5-V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
C_L	Load Capacitance	–	–	200	pF	This specification applies to the external circuit that is being driven by the analog output buffer.
V_{OSOB}	Input offset voltage (absolute value)	–	3	12	mV	
TCV_{OSOB}	Average input offset voltage drift	–	+6	–	µV/°C	
V_{CMOB}	Common mode input voltage range	0.5	–	V_{DD} – 1.0	V	
R_{OUTOB}	Output resistance Power = low Power = high	 – –	 0.6 0.6	 – –	 Ω Ω	
$V_{OHIGHOB}$	High output voltage swing (Load = 32 ohms to V_{DD}/2) Power = low Power = high	 0.5 × V_{DD} + 1.1 0.5 × V_{DD} + 1.1	 – –	 – –	 V V	
V_{OLOWOB}	Low output voltage swing (Load = 32 ohms to V_{DD}/2) Power = low Power = high	 – –	 – –	 0.5 × V_{DD} – 1.3 0.5 × V_{DD} – 1.3	 V V	
I_{SOB}	Supply current including opamp bias cell (No Load) Power = low Power = high	 – –	 1.1 2.6	 5.1 8.8	 mA mA	
$PSRR_{OB}$	Supply voltage rejection ratio	53	64	–	dB	(0.5 × V_{DD} – 1.3) ≤ V_{OUT} ≤ (V_{DD} – 2.3).

Table 19. 5-V DC Analog Reference Specifications *(continued)*

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b001	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.092	P2[4] + P2[6] – 0.011	P2[4] + P2[6] + 0.064	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.031	P2[4] – P2[6] + 0.007	P2[4] – P2[6] + 0.056	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.078	P2[4] + P2[6] – 0.008	P2[4] + P2[6] + 0.063	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.031	P2[4] – P2[6] + 0.004	P2[4] – P2[6] + 0.043	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.073	P2[4] + P2[6] – 0.006	P2[4] + P2[6] + 0.062	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.032	P2[4] – P2[6] + 0.003	P2[4] – P2[6] + 0.038	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.073	P2[4] + P2[6] – 0.006	P2[4] + P2[6] + 0.062	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.034	P2[4] – P2[6] + 0.002	P2[4] – P2[6] + 0.037	V
0b010	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.037	V_{DD} – 0.007	V_{DD}	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.036	V_{DD}/2 – 0.001	V_{DD}/2 + 0.036	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.005	V_{SS} + 0.029	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.034	V_{DD} – 0.006	V_{DD}	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.036	V_{DD}/2 – 0.001	V_{DD}/2 + 0.035	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.004	V_{SS} + 0.024	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.032	V_{DD} – 0.005	V_{DD}	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.036	V_{DD}/2 – 0.001	V_{DD}/2 + 0.035	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.003	V_{SS} + 0.022	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.031	V_{DD} – 0.005	V_{DD}	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.037	V_{DD}/2 – 0.001	V_{DD}/2 + 0.035	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.003	V_{SS} + 0.020	V

Table 19. 5-V DC Analog Reference Specifications *(continued)*

Refer-ence ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b111	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	3.2 × Bandgap	4.028	4.144	4.242	V
		V_{AGND}	AGND	1.6 × Bandgap	2.028	2.076	2.125	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.008	V_{SS} + 0.034	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	3.2 × Bandgap	4.032	4.142	4.245	V
		V_{AGND}	AGND	1.6 × Bandgap	2.029	2.076	2.126	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.005	V_{SS} + 0.025	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	3.2 × Bandgap	4.034	4.143	4.247	V
		V_{AGND}	AGND	1.6 × Bandgap	2.029	2.076	2.126	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.004	V_{SS} + 0.021	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	3.2 × Bandgap	4.036	4.144	4.249	V
		V_{AGND}	AGND	1.6 × Bandgap	2.029	2.076	2.126	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.003	V_{SS} + 0.019	V

Note The bits PORLEV and VM in the following table refer to bits in the VLT_CR register. See the *PSoC Technical Reference Manual* for more information on the VLT_CR register.

Table 22. DC POR and LVD Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
	V_{DD} value for PPOR trip (positive ramp)					
V_{PPOR0R}	PORLEV[1:0] = 00b		2.91		V	
V_{PPOR1R}	PORLEV[1:0] = 01b	–	4.39	–	V	
V_{PPOR2R}	PORLEV[1:0] = 10b		4.55		V	
	V_{DD} value for PPOR trip (negative ramp)					
V_{PPOR0} [23]	PORLEV[1:0] = 00b		2.82		V	
V_{PPOR1} [23]	PORLEV[1:0] = 01b	–	4.39	–	V	
V_{PPOR2} [23]	PORLEV[1:0] = 10b		4.55		V	
	PPOR hysteresis					
V_{PH0}	PORLEV[1:0] = 00b	–	92	–	mV	
V_{PH1}	PORLEV[1:0] = 01b	–	0	–	mV	
V_{PH2}	PORLEV[1:0] = 10b	–	0	–	mV	
	V_{DD} value for LVD trip					
V_{LVD0}	VM[2:0] = 000b	2.86	2.92	2.98[24]	V	
V_{LVD1}	VM[2:0] = 001b	2.96	3.02	3.08	V	
V_{LVD2}	VM[2:0] = 010b	3.07	3.13	3.20	V	
V_{LVD3}	VM[2:0] = 011b	3.92	4.00	4.08	V	
V_{LVD4}	VM[2:0] = 100b	4.39	4.48	4.57	V	
V_{LVD5}	VM[2:0] = 101b	4.55	4.64	4.74[25]	V	
V_{LVD6}	VM[2:0] = 110b	4.63	4.73	4.82	V	
V_{LVD7}	VM[2:0] = 111b	4.72	4.81	4.91	V	

Notes
23. Errata: When V_{DD} of the device is pulled below ground just before power on, the first read from each 8K Flash page may be corrupted. This issue does not affect Flash page 0 because it is the selected page upon reset. More details in "Errata" on page 66.
24. Always greater than 50 mV above PPOR (PORLEV = 00) for falling supply.
25. Always greater than 50 mV above PPOR (PORLEV = 10) for falling supply.

11.4 AC Electrical Characteristics

11.4.1 AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 25. AC Chip Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
$F_{IMO245V}$	Internal main oscillator frequency for 24 MHz (5 V)	23.04	24	24.96[29]	MHz	Trimmed for 5 V operation using factory trim values.
$F_{IMO243V}$	Internal main oscillator frequency for 24 MHz (3.3 V)	22.08	24	25.92[30]	MHz	Trimmed for 3.3 V operation using factory trim values.
$F_{IMOUSB5V}$	Internal main oscillator frequency with USB (5 V) Frequency locking enabled and USB traffic present.	23.94	24	24.06	MHz	–10 °C ≤ T_A ≤ 85 °C 4.35 ≤ V_{DD} ≤ 5.15
$F_{IMOUSB3V}$	Internal main oscillator frequency with USB (3.3 V) Frequency locking enabled and USB traffic present.	23.94	24	24.06	MHz	–0 °C ≤ T_A ≤ 70 °C 3.15 ≤ V_{DD} ≤ 3.45
F_{CPU1}	CPU frequency (5 V nominal)	0.093	24	24.96[29]	MHz	SLIMO Mode = 0.
F_{CPU2}	CPU frequency (3.3 V nominal)	0.086	12	12.96[30]	MHz	SLIMO Mode = 0.
F_{BLK5}	Digital PSoC block frequency (5 V nominal)	0	48	49.92[29,31]	MHz	Refer to the AC digital block Specifications.
F_{BLK3}	Digital PSoC block frequency (3.3 V nominal)	0	24	25.92[31]	MHz	
F_{32K1}	Internal low speed oscillator frequency	15	32	64	kHz	
F_{32K_U}	Internal low speed oscillator untrimmed frequency	5	–	100	kHz	After a reset and before the M8C starts to run, the ILO is not trimmed. See the System Resets section of the PSoC Technical Reference Manual for details on this timing
t_{XRST}	External reset pulse width	10	–	–	µs	
DC24M	24 MHz duty cycle	40	50	60	%	
DC_{ILO}	Internal low speed oscillator duty cycle	20	50	80	%	
Step24M	24 MHz trim step size	–	50	–	kHz	
Fout48M	48 MHz output frequency	46.08	48.0	49.92[29,30]	MHz	Trimmed. Utilizing factory trim values.
F_{MAX}	Maximum frequency of signal on row input or row output.	–	–	12.96	MHz	
SR_{POWER_UP}	Power supply slew rate	–	–	250	V/ms	V_{DD} slew rate during power-up.

Notes

26. The 50,000 cycle flash endurance per block is only guaranteed if the flash is operating within one voltage range. Voltage ranges are 3.0 V to 3.6 V and 4.75 V to 5.25 V.
27. A maximum of 36 × 50,000 block endurance cycles is allowed. This may be balanced between operations on 36 × 1 blocks of 50,000 maximum cycles each, 36 × 2 blocks of 25,000 maximum cycles each, or 36 × 4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36 × 50,000 and ensure that no single block ever sees more than 50,000 cycles).
For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. See the Flash APIs application note Design Aids – Reading and Writing PSoC® Flash – AN2015 for more information.
28. All GPIOs meet the DC GPIO V_{IL} and V_{IH} specifications found in the DC GPIO Specifications sections. The I^2C GPIO pins also meet the mentioned specifications.

11.4.5 AC Low Power Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V at 25 °C and are for design guidance only.

Table 30. AC Low Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{RLPC}	LPC response time	–	–	50	µs	≥ 50 mV overdrive comparator reference set within V_{REFLPC}.

11.4.6 AC Digital Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 31. AC Digital Block Specifications

Function	Description	Min	Typ	Max	Unit	Notes
All functions	Block input clock frequency					
	V_{DD} ≥ 4.75 V	–	–	49.92	MHz	
	V_{DD} < 4.75 V	–	–	25.92	MHz	
Timer	Input clock frequency					
	No capture, V_{DD} ≥ 4.75 V	–	–	49.92	MHz	
	No capture, V_{DD} < 4.75 V	–	–	25.92	MHz	
	With capture	–	–	25.92	MHz	
	Capture pulse width	50[33]	–	–	ns	
Counter	Input clock frequency					
	No enable input, V_{DD} ≥ 4.75 V	–	–	49.92	MHz	
	No enable input, V_{DD} < 4.75 V	–	–	25.92	MHz	
	With enable input	–	–	25.92	MHz	
	Enable input pulse width	50[33]	–	–	ns	
	Kill pulse width					
	Asynchronous restart mode	20	–	–	ns	
	Synchronous restart mode	50[33]	–	–	ns	
	Disable mode	50[33]	–	–	ns	
	Input clock frequency					
	V_{DD} ≥ 4.75 V	–	–	49.92	MHz	
	V_{DD} < 4.75 V	–	–	25.92	MHz	

Note
33. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).

Table 31. AC Digital Block Specifications *(continued)*

Function	Description	Min	Typ	Max	Unit	Notes
CRCPRS (PRS Mode)	Input clock frequency					
	$V_{DD} \geq 4.75$ V	–	–	49.92	MHz	
	$V_{DD} < 4.75$ V	–	–	25.92	MHz	
CRCPRS (CRC Mode)	Input clock frequency	–	–	24.6	MHz	
SPIM	Input clock frequency	–	–	8.2	MHz	The SPI serial clock (SCLK) frequency is equal to the input clock frequency divided by 2.
SPIS	Input clock (SCLK) frequency	–	–	4.1	MHz	The input clock is the SPI SCLK in SPIS mode.
	Width of SS_negated between transmissions	50[33]	–	–	ns	
Transmitter	Input clock frequency					The baud rate is equal to the input clock frequency divided by 8.
	$V_{DD} \geq 4.75$ V, 2 stop bits	–	–	49.92	MHz	
	$V_{DD} \geq 4.75$ V, 1 stop bit	–	–	24.6	MHz	
	$V_{DD} < 4.75$ V	–	–	24.6	MHz	
Receiver	Input clock frequency					The baud rate is equal to the input clock frequency divided by 8.
	$V_{DD} \geq 4.75$ V, 2 stop bits	–	–	49.92	MHz	
	$V_{DD} \geq 4.75$ V, 1 stop bit	–	–	24.6	MHz	
	$V_{DD} < 4.75$ V	–	–	24.6	MHz	

11.4.7 AC External Clock Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 32. AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency for USB applications	23.94	24	24.06	MHz	
–	Duty cycle	47	50	53	%	
–	Power-up to IMO switch	150	–	–	µs	

11.5 Thermal Impedance

Table 37. Thermal Impedances per Package

Package	Typical θ_{JA} [36]
56-Pin QFN[37]	12.93 °C/W
68-Pin QFN[37]	13.05 °C/W
100-Ball VFBGA	65 °C/W
100-Pin TQFP	51 °C/W

11.6 Solder Reflow Peak Specifications

Table 38 shows the solder reflow temperature limits that must not be exceeded.

Table 38. Solder Reflow Specifications

Package	Maximum Peak Temperature (T_C)	Maximum Time above T_C – 5 °C
56-Pin QFN	260 °C	30 seconds
68-Pin QFN	260 °C	30 seconds
100-Ball VFBGA	260 °C	30 seconds
100-Pin TQFP	260 °C	30 seconds

Notes
36. $T_J = T_A + POWER \times \theta_{JA}$.
37. To achieve the thermal impedance specified for the QFN package, see the *Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages* available at http://www.amkor.com.

- Getting Started guide
- USB 2.0 cable

12.4.2 CY3207ISSP In-System Serial Programmer (ISSP)

The CY3207ISSP is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production-programming environment.

Note: CY3207ISSP needs special software and is not compatible with PSoC Programmer. The kit includes:

- CY3207 programmer unit
- PSoC ISSP software CD
- 110 ~ 240 V power supply, Euro-Plug adapter
- USB 2.0 cable

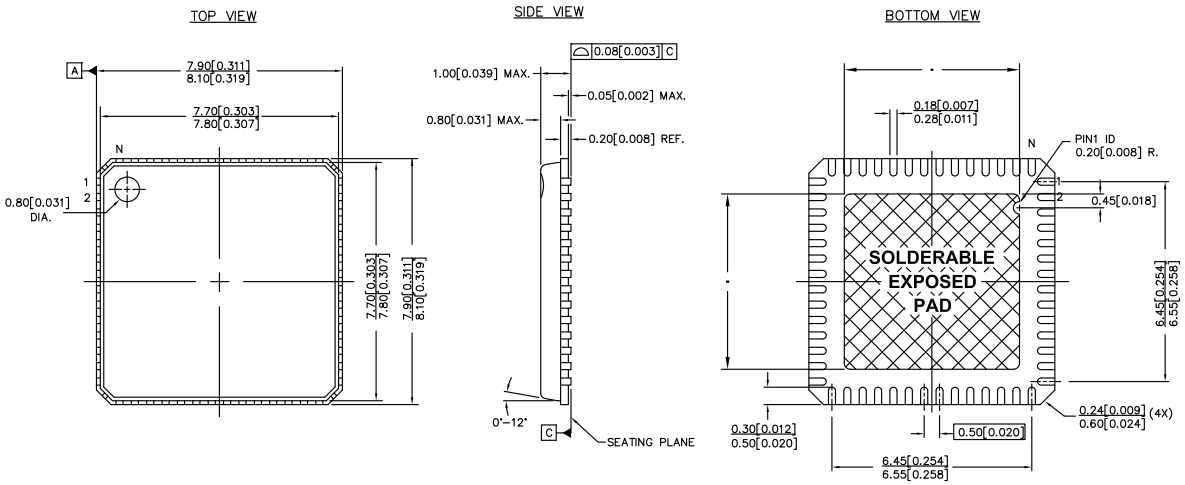
12.5 Accessories (Emulation and Programming)

Table 39. Emulation and Programming Accessories

Part #	Pin Package	Flex-Pod Kit[38]	Foot Kit[39]	Adapter[40]
CY8C24794-24LQXI	56-pin QFN	CY3250-24X94QFN	None	Adapters can be found at http://www.emulation.com.

Notes
38. Flex-Pod kit includes a practice flex-pod and a practice PCB, in addition to two flex-pods.
39. Foot kit includes surface mount feet that are soldered to the target PCB.
40. Programming adapter converts non-DIP package to DIP footprint. Specific details and ordering information for each of the adapters are found at http://www.emulation.com.

Figure 17. 56-pin QFN (8 × 8 × 1.0 mm) LF56A/LY56A 4.5 × 5.21 E-Pad (Subcon Punch Type Pkg.) Package Outline, 001-12921

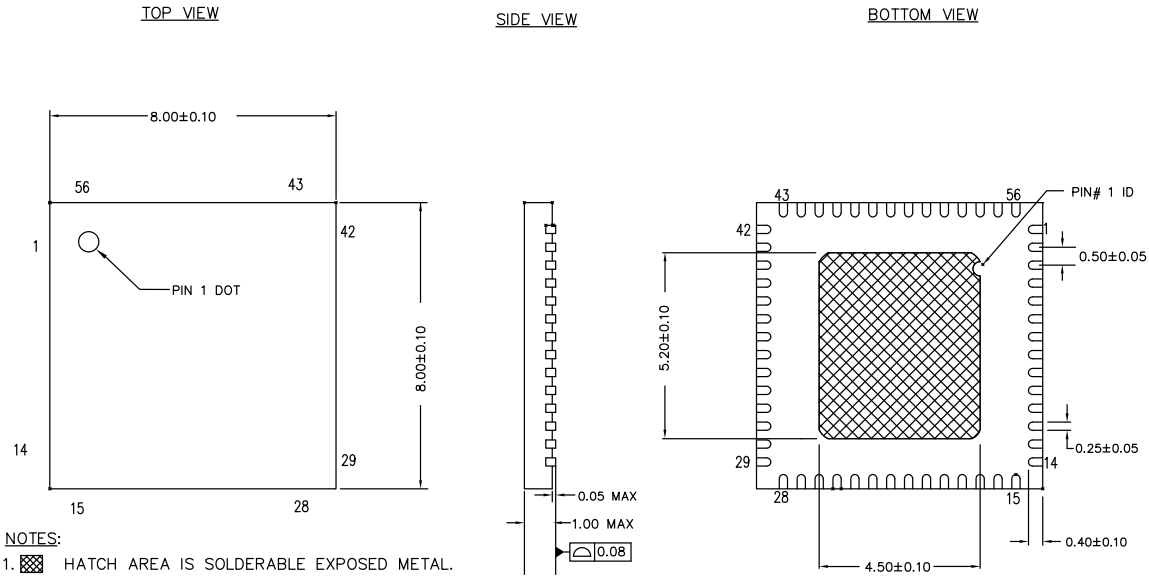


NOTES:
1. HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO–220
3. PACKAGE WEIGHT: 0.162g
4. ALL DIMENSIONS ARE IN MM [MIN/MAX]
5. PACKAGE CODE

PART #	DESCRIPTION
LF56A	STANDARD
LY56A	PB–FREE

001-12921 *C

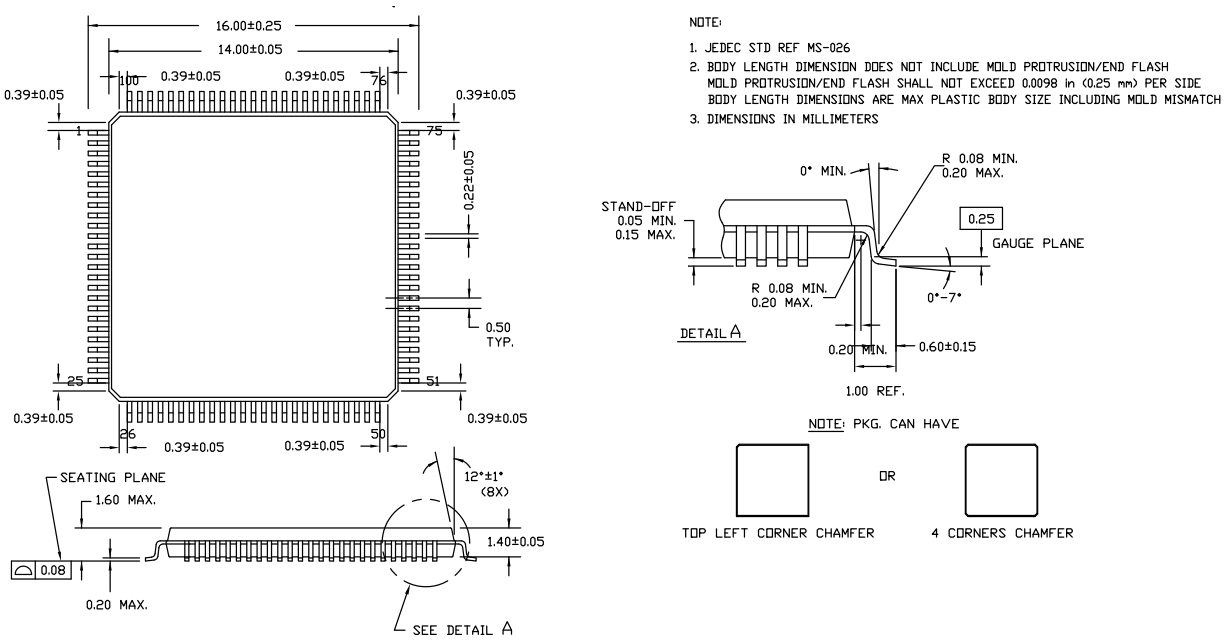
Figure 18. 56-pin QFN (8 × 8 × 1.0 mm) LT56B 4.5 × 5.2 E-Pad (Sawn) Package Outline, 001-53450



NOTES:
1. HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO–220
3. PACKAGE WEIGHT: 162 ± 16 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-53450 *D

Figure 21. 100-pin TQFP (14 × 14 × 1.4 mm) A100SA Package Outline, 51-85048



51-85048 *J

Important Note

- For information on the preferred dimensions for mounting QFN packages, see the Application Note, *Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages* available at http://www.amkor.com.
- Pinned vias for thermal conduction are not required for the low power PSoC device.

When Vdd is pulled below ground before power on, an internal Flash reference may deviate from its nominal voltage. The reference deviation tends to result in the first Flash read from that page returning 0xFF. During the first read from each page, the reference is reset resulting in all future reads returning the correct value. A short delay of 5 µs before the first real read provides time for the reference voltage to stabilize.

■ **WORKAROUND**

To prevent an invalid Flash read, a dummy read from each Flash page must occur before use of the pages. A delay of 5 µs must occur after the dummy read and before a real read. The dummy reads occurs as soon as possible and must be located in Flash page 0 before a read from any other Flash page. An example for reading a byte of memory from each Flash page is listed below. Placed it in boot.tpl and boot.asm immediately after the ‘start:’ label.

```
// dummy read from each 8K Flash page
// page 1
mov  A, 0x20        // MSB
mov  X, 0x00        // LSB
romx
// wait at least 5 µs
mov  X, 14
loop1:
dec  X
jnz  loop1
```

19. Document History Page

Document Title: CY8C24094/CY8C24794/CY8C24894/CY8C24994, PSoC® Programmable System-on-Chip™ Document Number: 38-12018				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	133189	NWJ	01/27/2004	New silicon and new document – Advance datasheet.
*A	251672	SFV	See ECN	First Preliminary datasheet. Changed title to encompass only the CY8C24794 because the CY8C24494 and CY8C24694 are not being offered by Cypress.
*B	289742	HMT	See ECN	Add standard DS items from SFV memo. Add Analog Input Mux on pinouts. 2 MACs. Change 512 bytes of SRAM to 1 K. Add dimension key to package. Remove HAPI. Update diagrams, registers and specs.
*C	335236	HMT	See ECN	Add CY logo. Update CY copyright. Update new CY.com URLs. Re-add ISSP programming pinout notation. Add Reflow Temp. table. Update features (MAC, Oscillator, and voltage range), registers (INT_CLR2/MSK2, second MAC), and specs. (Rext, IMO, analog output buffer...).
*D	344318	HMT	See ECN	Add new color and logo. Expand analog arch. diagram. Fix I/O #. Update Electrical Specifications.
*E	346774	HMT	See ECN	Add USB temperature specifications. Make datasheet Final.
*F	349566	HMT	See ECN	Remove USB logo. Add URL to preferred dimensions for mounting MLF packages.
*G	393164	HMT	See ECN	Add new device, CY8C24894 56-pin MLF with XRES pin. Add Fimousb3v char. to specs. Upgrade to CY Perform logo and update corporate address and copyright.
*H	469243	HMT	See ECN	Add ISSP note to pinout tables. Update typical and recommended Storage Temperature per industrial specs. Update Low Output Level maximum I/OL budget. Add FLS_PR1 to Register Map Bank 1 for users to specify which Flash bank should be used for SROM operations. Add two new devices for a 68-pin QFN and 100-ball VFBGA under RPNs: CY8C24094 and CY8C24994. Add two packages for 68-pin QFN. Add OCD non-production pinouts and package diagrams. Update CY branding and QFN convention. Add new Dev. Tool section. Update copyright and trademarks.
*I	561158	HMT	See ECN	Add Low Power Comparator (LPC) AC/DC electrical spec. tables. Add CY8C20x34 to PSoC Device Characteristics table. Add detailed dimensions to 56-pin QFN package diagram and update revision. Secure one package diagram/manufacturing per QFN. Update emulation pod/feet kit part numbers. Fix pinout type-o per TestTrack.
*J	728238	HMT	See ECN	Add CapSense SNR requirement reference. Update figure standards. Update Technical Training paragraphs. Add QFN package clarifications and dimensions. Update ECN-ed Amkor dimensioned QFN package diagram revisions. Reword SNR reference. Add new 56-pin QFN spec.
*K	2552459	AZIE / PYRS	08/14/08	Add footnote on AGND descriptions to avoid using P2[4] for digital signaling as it may add noise to AGND. Remove reference to CMP_GO_EN1 in Map Bank 1 Table on Address 65; this register has no functionality on 24xxx. Add footnote on die sales. Add description 'Optional External Clock Input' on P1[4] to match description of P1[4].
*L	2616550	OGNE / PYRS	12/05/08	Updated Programmable Pin Configuration detail. Changed title from PSoC® Mixed-Signal Array to PSoC® Programmable System-on-Chip™
*M	2657956	DPT / PYRS	02/11/09	Added package diagram 001-09618 and updated Ordering Information table

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