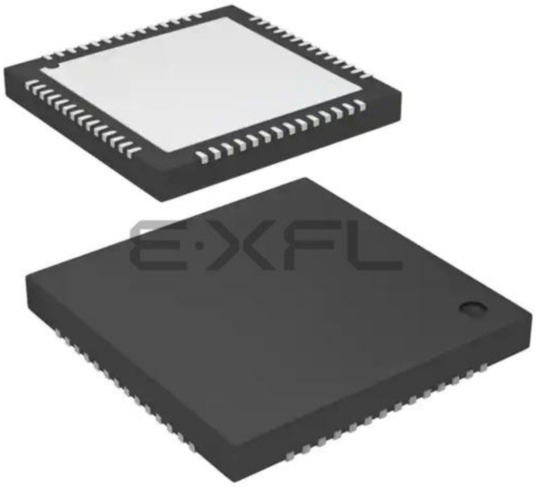

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SPI, UART/USART, USB
Peripherals	POR, PWM, WDT
Number of I/O	50
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	A/D 48x14b; D/A 2x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	56-VFQFN Exposed Pad
Supplier Device Package	56-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c24794-24ltxit

3. More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right PSoC device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the knowledge base article KBA92181, Resources Available for CapSense® Controllers. Following is an abbreviated list for CapSense devices:

- Overview: CapSense Portfolio, CapSense Roadmap
- Product Selectors: CapSense, CapSense Plus, CapSense Express, PSoC3 with CapSense, PSoC5 with CapSense, PSoC4. In addition, PSoC Designer offers a device selection tool at the time of creating a new project.
- Application notes: Cypress offers CapSense application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with CapSense are:
  - AN64846: Getting Started With CapSense
  - AN2397: CapSense® Data Viewing Tools
- Technical Reference Manual (TRM):
  - CY8CPLC20, CY8CLED16P01, CY8C29x66, CY8C27x43, CY8C24x94, CY8C24x23, CY8C24x23A, CY8C22x13, CY8C21x34, CY8C21x34B, CY8C21x23, CY7C64215, CY7C603xx, CY8CNP1xx, and CYWUSB6953 PSoC® Programmable System-on-Chip TRM
- Development Kits:
  - CY3280-24x94 Universal CapSense Controller Board features a predefined control circuitry and plug-in hardware to make prototyping and debugging easy. Programming and I2C-to-USB Bridge hardware are included for tuning and data acquisition.
  - CY3280-BMM Matrix Button Module Kit consists of eight CapSense sensors organized in a 4x4 matrix format to form 16 physical buttons and eight LEDs. This module connects to any CY3280 Universal CapSense Controller Board, including CY3280-20x66 Universal CapSense Controller.
  - CY3280-BSM Simple Button Module Kit consists of ten CapSense buttons and ten LEDs. This module connects to any CY3280 Universal CapSense Controller Board, including CY3280-20x66 Universal CapSense Controller.

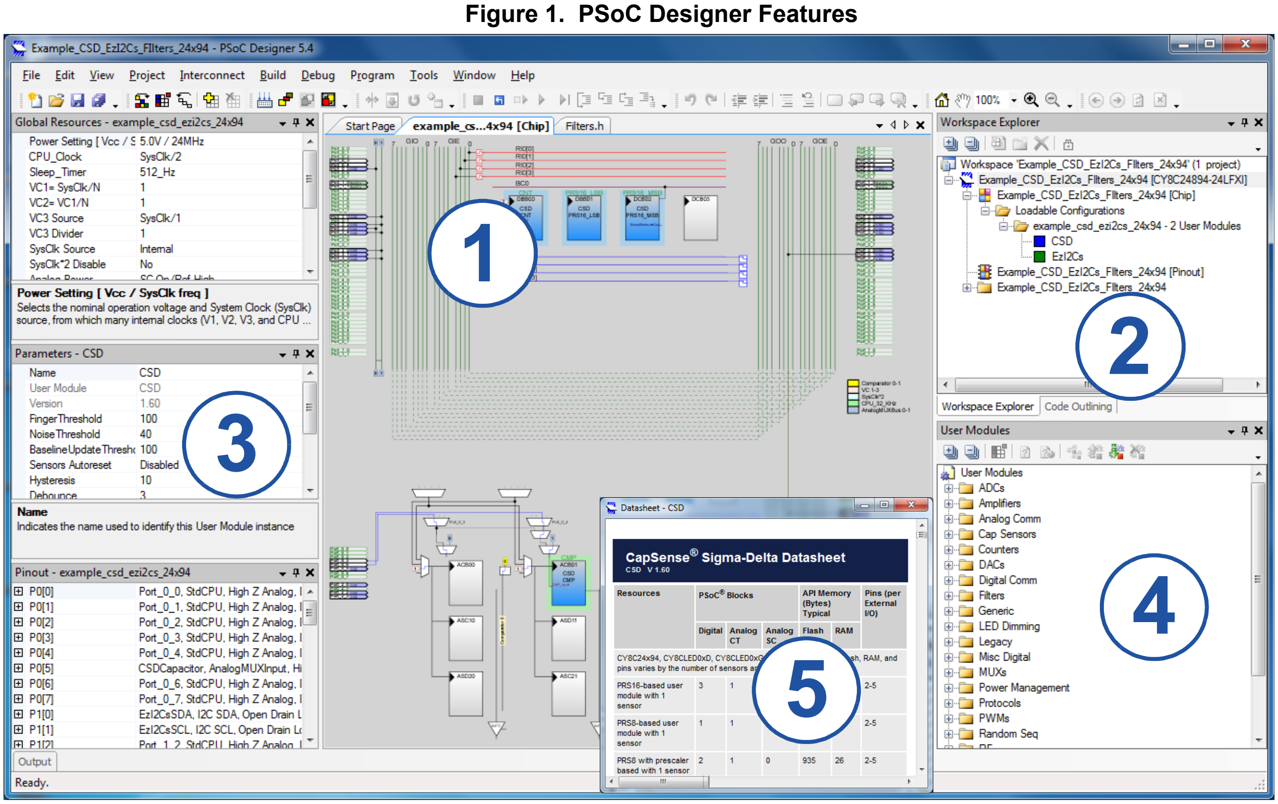
The CY3217-MiniProg1 and CY8CKIT-002 PSoC® MiniProg3 device provides an interface for flash programming.

3.1 PSoC Designer

PSoC Designer is a free Windows-based Integrated Design Environment (IDE). It enables concurrent hardware and firmware design of systems based on CapSense (see Figure 1). With PSoC Designer, you can:

1. Drag and drop User Modules to build your hardware system design in the main design workspace
2. Codesign your application firmware with the PSoC hardware, using the PSoC Designer IDE C compiler
3. Configure User Module
4. Explore the library of user modules
5. Review user module datasheets

Figure 1. PSoC Designer Features



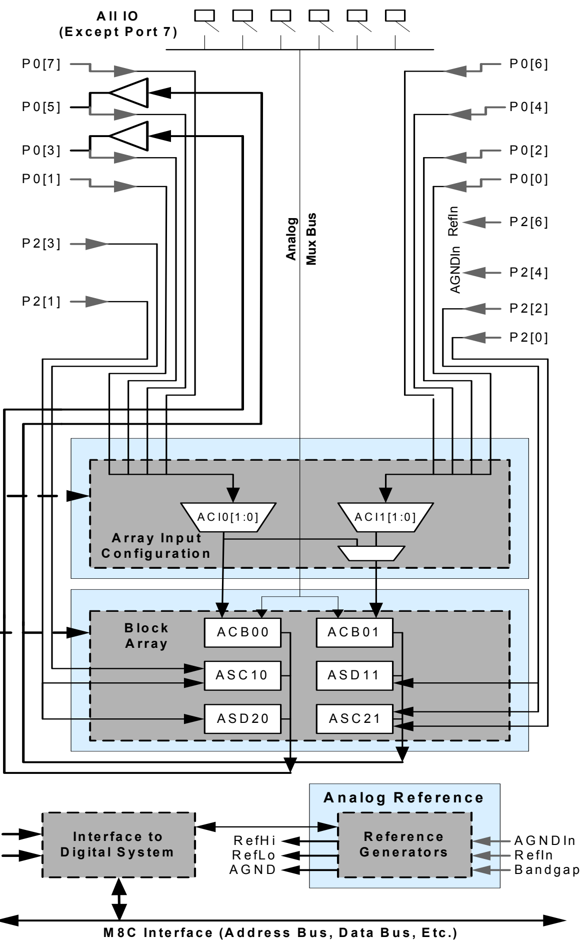
5.3 The Analog System

The analog system is composed of six configurable blocks, each comprised of an opamp circuit allowing the creation of complex analog signal flows. Analog peripherals are very flexible and can be customized to support specific application requirements. Some of the more common PSoC analog functions (most available as user modules) are as follows.

- ADCs (up to two, with 6- to 14-bit resolution, selectable as incremental, delta sigma, and successive approximation register (SAR))
- Filters (2 and 4 pole band-pass, low-pass, and notch)
- Amplifiers (up to two, with selectable gain to 48x)
- Instrumentation amplifiers (one with selectable gain to 93x)
- Comparators (up to two, with 16 selectable thresholds)
- DACs (up to two, with 6- to 9-bit resolution)
- Multiplying DACs (up to two, with 6- to 9-bit resolution)
- High current output drivers (two with 30 mA drive as a PSoC core resource)
- 1.3-V reference (as a system resource)
- DTMF dialer
- Modulators
- Correlators
- Peak detectors
- Many other topologies possible

Analog blocks are arranged in a column of three, which includes one continuous time (CT) and two switched capacitor (SC) blocks, as shown in Figure 3.

Figure 3. Analog System Block Diagram



5.3.1 The Analog Multiplexer System

The analog mux bus can connect to every GPIO pin in ports 0–5. Pins are connected to the bus individually or in any combination. The bus also connects to the analog system for analysis with comparators and analog-to-digital converters. It is split into two sections for simultaneous dual-channel processing. An additional 8:1 analog input multiplexer provides a second path to bring Port 0 pins to the analog array.

Switch-control logic enables selected pins to precharge continuously under hardware control. This enables capacitive measurement for applications such as touch sensing. Other multiplexer applications include:

- Track pad, finger sensing
- Chip-wide mux that enables analog input from up to 48 I/O pins
- Crosspoint connection between any I/O pin combinations

5.4 Additional System Resources

System resources provide additional capability useful to complete systems. Additional resources include a multiplier, decimator, low-voltage detection, and power-on reset (POR). Brief statements describing the merits of each resource follow.

- Full speed USB (12 Mbps) with five configurable endpoints and 256 bytes of RAM. No external components required except for two series resistors. Wider than commercial temperature USB operation (–10 °C to +85 °C).
- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks can be routed to both the digital and analog systems. Additional clocks are generated using digital PSoC blocks as clock dividers.
- Two multiply accumulates (MACs) provide fast 8-bit multipliers with 32-bit accumulate, to assist in both general math and digital filters.
- Decimator provides a custom hardware filter for digital signal processing applications including creation of Delta Sigma ADCs.
- The I^2C module provides 100- and 400-kHz communication over two wires. Slave, master, multi-master are supported.
- Low-voltage detection interrupts signal the application of falling voltage levels, while the advanced POR circuit eliminates the need for a system supervisor.
- An internal 1.3-V reference provides an absolute reference for the analog system, including ADCs and DACs.
- Versatile analog multiplexer system.

5.5 PSoC Device Characteristics

Depending on your PSoC device characteristics, the digital and analog systems can have 16, 8, or 4 digital blocks and 12, 6, or 4 analog blocks. The following table lists the resources available for specific PSoC device groups. The device covered by this datasheet is shown in the highlighted row of the table.

Table 1. PSoC Device Characteristics

PSoC Part Number	Digital I/O	Digital Rows	Digital Blocks	Analog Inputs	Analog Outputs	Analog Columns	Analog Blocks	SRAM Size	Flash Size
CY8C29x66	up to 64	4	16	up to 12	4	4	12	2 K	32 K
CY8C28xxx	up to 44	up to 3	up to 12	up to 44	up to 4	up to 6	up to 12 + 4[1]	1 K	16 K
CY8C27x43	up to 44	2	8	up to 12	4	4	12	256	16 K
CY8C24x94	up to 56	1	4	up to 48	2	2	6	1 K	16 K
CY8C24x23A	up to 24	1	4	up to 12	2	2	6	256	4 K
CY8C23x33	up to 26	1	4	up to 12	2	2	4	256	8 K
CY8C22x45	up to 38	2	8	up to 38	0	4	6[1]	1 K	16 K
CY8C21x45	up to 24	1	4	up to 24	0	4	6[1]	512	8 K
CY8C21x34	up to 28	1	4	up to 28	0	2	4[1]	512	8 K
CY8C21x23	up to 16	1	4	up to 8	0	2	4[1]	256	4 K
CY8C20x34	up to 28	0	0	up to 28	0	0	3[1,2]	512	8 K
CY8C20xx6	up to 36	0	0	up to 36	0	0	3[1,2]	up to 2 K	up to 32 K

Notes
1. Limited analog functionality.
2. Two analog blocks and one CapSense®.

9.3 68-Pin Part Pinout

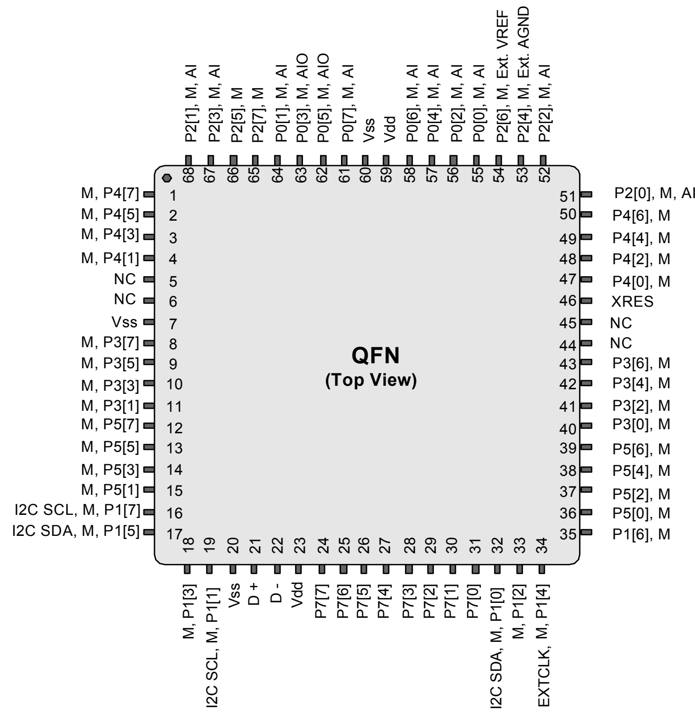
The following 68-pin QFN part table and drawing is for the CY8C24994 PSoC device.

Table 4. 68-Pin Part Pinout (QFN[9])

Pin No.	Type Digital	Type Analog	Name	Description
1	I/O	M	P4[7]	
2	I/O	M	P4[5]	
3	I/O	M	P4[3]	
4	I/O	M	P4[1]	
5			NC	No connection. Pin must be left floating
6			NC	No connection. Pin must be left floating
7	Power		V_{SS}	Ground connection [10]
8	I/O	M	P3[7]	
9	I/O	M	P3[5]	
10	I/O	M	P3[3]	
11	I/O	M	P3[1]	
12	I/O	M	P5[7]	
13	I/O	M	P5[5]	
14	I/O	M	P5[3]	
15	I/O	M	P5[1]	
16	I/O	M	P1[7]	I^{2}C SCL
17	I/O	M	P1[5]	I^{2}C SDA
18	I/O	M	P1[3]	
19	I/O	M	P1[1]	I2C SCL ISSP SCLK[11]
20	Power		V_{SS}	Ground connection [10]
21	USB		D+	
22	USB		D–	
23	Power		V_{DD}	Supply voltage
24	I/O		P7[7]	
25	I/O		P7[6]	
26	I/O		P7[5]	
27	I/O		P7[4]	
28	I/O		P7[3]	
29	I/O		P7[2]	
30	I/O		P7[1]	
31	I/O		P7[0]	
32	I/O	M	P1[0]	I^{2}C SDA, ISSP SDATA[11]
33	I/O	M	P1[2]	
34	I/O	M	P1[4]	Optional EXTCLK
35	I/O	M	P1[6]	
36	I/O	M	P5[0]	
37	I/O	M	P5[2]	
38	I/O	M	P5[4]	
39	I/O	M	P5[6]	
40	I/O	M	P3[0]	
41	I/O	M	P3[2]	
42	I/O	M	P3[4]	
43	I/O	M	P3[6]	
44			NC	No connection. Pin must be left floating.
45			NC	No connection. Pin must be left floating.
46	Input		XRES	Active high pin reset with internal pull-down.
47	I/O	M	P4[0]	
48	I/O	M	P4[2]	
49	I/O	M	P4[4]	
50	I/O	M	P4[6]	
51	I/O	I, M	P2[0]	Direct switched capacitor block input
52	I/O	I, M	P2[2]	Direct switched capacitor block input
53	I/O	M	P2[4]	External AGND input
54	I/O	M	P2[6]	External VREF input
55	I/O	I, M	P0[0]	Analog column mux input
56	I/O	I, M	P0[2]	Analog column mux input and column output
57	I/O	I, M	P0[4]	Analog column mux input and column output
58	I/O	I, M	P0[6]	Analog column mux input
59	Power		V_{DD}	Supply voltage
60	Power		V_{SS}	Ground connection [10]
61	I/O	I, M	P0[7]	Analog column mux input, integration input #1
62	I/O	I/O, M	P0[5]	Analog column mux input and column output, integration input #2
63	I/O	I/O, M	P0[3]	Analog column mux input and column output
64	I/O	I, M	P0[1]	Analog column mux input
65	I/O	M	P2[7]	
66	I/O	M	P2[5]	
67	I/O	I, M	P2[3]	Direct switched capacitor block input
68	I/O	I, M	P2[1]	Direct switched capacitor block input

LEGEND A = Analog, I = Input, O = Output, NC = No connection. Pin must be left floating, M = Analog Mux Input.

Figure 6. CY8C24994 68-Pin PSoC Device



Notes

9. The center pad on the QFN package should be connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it should be electrically floated and not connected to any other signal.
10. All V_{SS} pins should be brought out to one common GND plane.
11. These are the ISSP pins, which are not High Z at POR. See the PSoC Technical Reference Manual for details.

9.5 100-Ball VFBGA Part Pinout

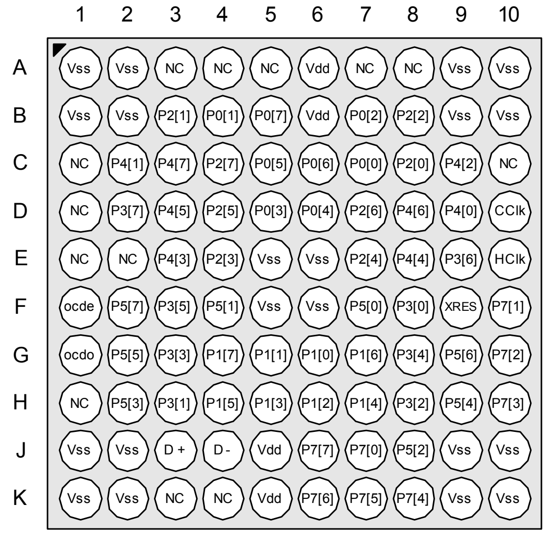
The 100-ball VFBGA part is for the CY8C24994 PSoC device.

Table 6. 100-Ball Part Pinout (VFBGA[15])

Pin No.	Digital	Analog	Name	Description	Pin No.	Digital	Analog	Name	Description
A1	Power		V_{SS}	Ground connection	F1			NC	No connection. Pin must be left floating
A2	Power		V_{SS}	Ground connection	F2	I/O	M	P5[7]	
A3			NC	No connection. Pin must be left floating	F3	I/O	M	P3[5]	
A4			NC	No connection. Pin must be left floating	F4	I/O	M	P5[1]	
A5			NC	No connection. Pin must be left floating	F5	Power		V_{SS}	Ground connection
A6	Power		V_{DD}	Supply voltage	F6	Power		V_{SS}	Ground connection
A7			NC	No connection. Pin must be left floating	F7	I/O	M	P5[0]	
A8			NC	No connection. Pin must be left floating	F8	I/O	M	P3[0]	
A9	Power		V_{SS}	Ground connection	F9			XRES	Active high pin reset with internal pull-down
A10	Power		V_{SS}	Ground connection	F10	I/O		P7[1]	
B1	Power		V_{SS}	Ground connection	G1			NC	No connection. Pin must be left floating
B2	Power		V_{SS}	Ground connection	G2	I/O	M	P5[5]	
B3	I/O	I, M	P2[1]	Direct switched capacitor block input	G3	I/O	M	P3[3]	
B4	I/O	I, M	P0[1]	Analog column mux input	G4	I/O	M	P1[7]	I^{2}C SCL
B5	I/O	I, M	P0[7]	Analog column mux input	G5	I/O	M	P1[1]	I^{2}C SCL, ISSP SCLK[16]
B6	Power		V_{DD}	Supply voltage	G6	I/O	M	P1[0]	I^{2}C SDA, ISSP SDATA[16]
B7	I/O	I, M	P0[2]	Analog column mux input	G7	I/O	M	P1[6]	
B8	I/O	I, M	P2[2]	Direct switched capacitor block input	G8	I/O	M	P3[4]	
B9	Power		V_{SS}	Ground connection	G9	I/O	M	P5[6]	
B10	Power		V_{SS}	Ground connection	G10	I/O		P7[2]	
C1			NC	No connection. Pin must be left floating	H1			NC	No connection. Pin must be left floating
C2	I/O	M	P4[1]		H2	I/O	M	P5[3]	
C3	I/O	M	P4[7]		H3	I/O	M	P3[1]	
C4	I/O	M	P2[7]		H4	I/O	M	P1[5]	I^{2}C SDA
C5	I/O	I/O, M	P0[5]	Analog column mux input and column output	H5	I/O	M	P1[3]	
C6	I/O	I, M	P0[6]	Analog column mux input	H6	I/O	M	P1[2]	
C7	I/O	I, M	P0[0]	Analog column mux input	H7	I/O	M	P1[4]	Optional EXTCLK
C8	I/O	I, M	P2[0]	Direct switched capacitor block input	H8	I/O	M	P3[2]	
C9	I/O	M	P4[2]		H9	I/O	M	P5[4]	
C10			NC	No connection. Pin must be left floating	H10	I/O		P7[3]	
D1			NC	No connection. Pin must be left floating	J1	Power		V_{SS}	Ground connection
D2	I/O	M	P3[7]		J2	Power		V_{SS}	Ground connection
D3	I/O	M	P4[5]		J3	USB		D+	
D4	I/O	M	P2[5]		J4	USB		D–	
D5	I/O	I/O, M	P0[3]	Analog column mux input and column output	J5	Power		V_{DD}	Supply voltage
D6	I/O	I,M	P0[4]	Analog column mux input	J6	I/O		P7[7]	
D7	I/O	M	P2[6]	External VREF input	J7	I/O		P7[0]	
D8	I/O	M	P4[6]		J8	I/O	M	P5[2]	
D9	I/O	M	P4[0]		J9	Power		V_{SS}	Ground connection
D10			NC	No connection. Pin must be left floating	J10	Power		V_{SS}	Ground connection
E1			NC	No connection. Pin must be left floating	K1	Power		V_{SS}	Ground connection
E2			NC	No connection. Pin must be left floating	K2	Power		V_{SS}	Ground connection
E3	I/O	M	P4[3]		K3			NC	No connection. Pin must be left floating
E4	I/O	I, M	P2[3]	Direct switched capacitor block input	K4			NC	No connection. Pin must be left floating
E5	Power		V_{SS}	Ground connection	K5	Power		V_{DD}	Supply voltage
E6	Power		V_{SS}	Ground connection	K6	I/O		P7[6]	
E7	I/O	M	P2[4]	External AGND input	K7	I/O		P7[5]	
E8	I/O	M	P4[4]		K8	I/O		P7[4]	
E9	I/O	M	P3[6]		K9	Power		V_{SS}	Ground connection
E10			NC	No connection. Pin must be left floating	K10	Power		V_{SS}	Ground connection

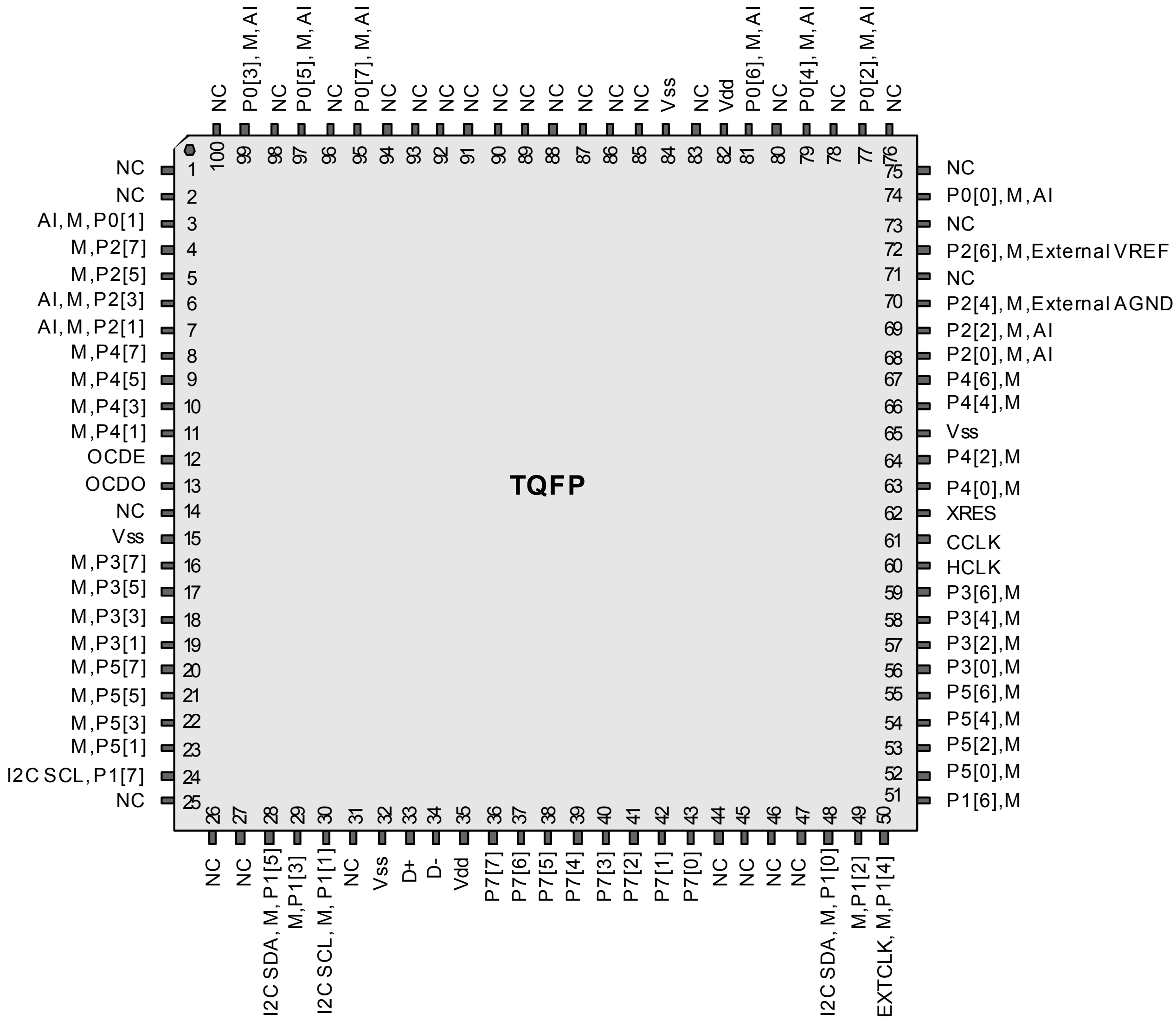
LEGEND A = Analog, I = Input, O = Output, M = Analog Mux Input, NC = No connection. Pin must be left floating.

Figure 9. CY8C24094 OCD (Not for Production)



BGA (Top View)

Figure 10. CY8C24094 OCD (Not for Production)



10. Register Reference

This section lists the registers of the CY8C24x94 PSoC device family. For detailed register information, see the *PSoC Technical Reference Manual*.

10.1 Register Conventions

The register conventions specific to this section are listed in the following table.

Convention	Description
R	Read register or bit(s)
W	Write register or bit(s)
L	Logical register or bit(s)
C	Clearable register or bit(s)
#	Access is bit specific

10.2 Register Mapping Tables

The PSoC device has a total register address space of 512 bytes. The register space is referred to as I/O space and is divided into two banks, Bank 0 and Bank 1. The XOI bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XOI bit is set to 1, the user is in Bank 1.

Note In the following register mapping tables, blank fields are Reserved and should not be accessed.

10.4 Register Map Bank 1 Table: Configuration Space

Name	Addr (1, Hex)	Access	Name	Addr (1, Hex)	Access	Name	Addr (1, Hex)	Access	Name	Addr (1, Hex)	Access
PRT0DM0	00	RW	PMA0_WA	40	RW	ASC10CR0	80	RW	USBI/O_CR2	C0	RW
PRT0DM1	01	RW	PMA1_WA	41	RW	ASC10CR1	81	RW	USB_CR1	C1	#
PRT0IC0	02	RW	PMA2_WA	42	RW	ASC10CR2	82	RW			
PRT0IC1	03	RW	PMA3_WA	43	RW	ASC10CR3	83	RW			
PRT1DM0	04	RW	PMA4_WA	44	RW	ASD11CR0	84	RW	EP1_CR0	C4	#
PRT1DM1	05	RW	PMA5_WA	45	RW	ASD11CR1	85	RW	EP2_CR0	C5	#
PRT1IC0	06	RW	PMA6_WA	46	RW	ASD11CR2	86	RW	EP3_CR0	C6	#
PRT1IC1	07	RW	PMA7_WA	47	RW	ASD11CR3	87	RW	EP4_CR0	C7	#
PRT2DM0	08	RW		48			88			C8	
PRT2DM1	09	RW		49			89			C9	
PRT2IC0	0A	RW		4A			8A			CA	
PRT2IC1	0B	RW		4B			8B			CB	
PRT3DM0	0C	RW		4C			8C			CC	
PRT3DM1	0D	RW		4D			8D			CD	
PRT3IC0	0E	RW		4E			8E			CE	
PRT3IC1	0F	RW		4F			8F			CF	
PRT4DM0	10	RW	PMA0_RA	50	RW		90		GDI_O_IN	D0	RW
PRT4DM1	11	RW	PMA1_RA	51	RW	ASD20CR1	91	RW	GDI_E_IN	D1	RW
PRT4IC0	12	RW	PMA2_RA	52	RW	ASD20CR2	92	RW	GDI_O_OU	D2	RW
PRT4IC1	13	RW	PMA3_RA	53	RW	ASD20CR3	93	RW	GDI_E_OU	D3	RW
PRT5DM0	14	RW	PMA4_RA	54	RW	ASC21CR0	94	RW		D4	
PRT5DM1	15	RW	PMA5_RA	55	RW	ASC21CR1	95	RW		D5	
PRT5IC0	16	RW	PMA6_RA	56	RW	ASC21CR2	96	RW		D6	
PRT5IC1	17	RW	PMA7_RA	57	RW	ASC21CR3	97	RW		D7	
	18			58			98		MUX_CR0	D8	RW
	19			59			99		MUX_CR1	D9	RW
	1A			5A			9A		MUX_CR2	DA	RW
	1B			5B			9B		MUX_CR3	DB	RW
PRT7DM0	1C	RW		5C			9C			DC	
PRT7DM1	1D	RW		5D			9D		OSC_GO_EN	DD	RW
PRT7IC0	1E	RW		5E			9E		OSC_CR4	DE	RW
PRT7IC1	1F	RW		5F			9F		OSC_CR3	DF	RW
DBB00FN	20	RW	CLK_CR0	60	RW		A0		OSC_CR0	E0	RW
DBB00IN	21	RW	CLK_CR1	61	RW		A1		OSC_CR1	E1	RW
DBB00OU	22	RW	ABF_CR0	62	RW		A2		OSC_CR2	E2	RW
	23		AMD_CR0	63	RW		A3		VLT_CR	E3	RW
DBB01FN	24	RW	CMP_GO_EN	64	RW		A4		VLT_CMP	E4	R
DBB01IN	25	RW		65			A5			E5	
DBB01OU	26	RW	AMD_CR1	66	RW		A6			E6	
	27		ALT_CR0	67	RW		A7			E7	
DCB02FN	28	RW		68			A8		IMO_TR	E8	W
DCB02IN	29	RW		69			A9		ILO_TR	E9	W
DCB02OU	2A	RW		6A			AA		BDG_TR	EA	RW
	2B			6B			AB		ECO_TR	EB	W
DCB03FN	2C	RW	TMP_DR0	6C	RW		AC		MUX_CR4	EC	RW
DCB03IN	2D	RW	TMP_DR1	6D	RW		AD		MUX_CR5	ED	RW
DCB03OU	2E	RW	TMP_DR2	6E	RW		AE			EE	
	2F		TMP_DR3	6F	RW		AF			EF	
	30		ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
	31		ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
	32		ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
	34		ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
	35		ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
	36		ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
	37		ACB01CR2	77	RW		B7		CPU_F	F7	RL
	38			78			B8			F8	
	39			79			B9			F9	
	3A			7A			BA			FA	
	3B			7B			BB			FB	
	3C			7C			BC			FC	
	3D			7D			BD		DAC_CR	FD	RW
	3E			7E			BE		CPU_SCR1	FE	#
	3F			7F			BF		CPU_SCR0	FF	#

Blank fields are reserved and should not be accessed.

Access is bit specific.

11.3.3 DC Full Speed USB Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –10 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –10 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 13. DC Full Speed (12 Mbps) USB Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
USB Interface						
V_{DI}	Differential input sensitivity	0.2	–	–	V	| (D+) – (D–) |
V_{CM}	Differential input common mode range	0.8	–	2.5	V	
V_{SE}	Single ended receiver threshold	0.8	–	2.0	V	
C_{IN}	Transceiver capacitance	–	–	20	pF	
$I_{I/O}$	High Z state data line leakage	–10	–	10	µA	0 V < V_{IN} < 3.3 V.
R_{EXT}	External USB series resistor	23	–	25	Ω	In series with each USB pin.
V_{UOH}	Static output high, driven	2.8	–	3.6	V	15 kΩ ± 5% to ground. Internal pull-up enabled.
V_{UOHI}	Static output high, idle	2.7	–	3.6	V	15 kΩ ± 5% to ground. Internal pull-up enabled.
V_{UOL}	Static output low	–	–	0.3	V	15 kΩ ± 5% to ground. Internal pull-up enabled.
Z_O	USB driver output impedance	28	–	44	Ω	Including R_{EXT} resistor.
V_{CRS}	D+/D– crossover voltage	1.3	–	2.0	V	

Table 15. 3.3-V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input offset voltage (absolute value) Power = low, Opamp bias = high Power = medium, Opamp bias = high Power = high, Opamp bias = high	 – – –	 1.65 1.32 –	 10 8 –	 mV mV mV	Power = high, Opamp bias = high setting is not allowed for 3.3 V V_{DD} operation
TCV_{OSOA}	Average input offset voltage drift	–	7.0	35.0	µV/°C	
I_{EBOA}	Input leakage current (port 0 analog pins)	–	20	–	pA	Gross tested to 1 µA.
C_{INOA}	Input capacitance (port 0 analog pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25 °C.
V_{CMOA}	Common mode voltage range	0.2	–	V_{DD} – 0.2	V	The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
G_{OLOA}	Open loop gain Power = low, Opamp bias = low Power = medium, Opamp bias = low Power = high, Opamp bias = low	 60 60 80	 – – –	 – – –	 dB dB dB	Specification is applicable at Low opamp bias. For high opamp bias mode (except high power, High opamp bias), minimum is 60 dB.
$V_{OHIGHOA}$	High output voltage swing (internal signals) Power = low, Opamp bias = low Power = medium, Opamp bias = low Power = high, Opamp bias = low	 V_{DD} – 0.2 V_{DD} – 0.2 V_{DD} – 0.2	 – – –	 – – –	 V V V	Power = high, Opamp bias = high setting is not allowed for 3.3 V V_{DD} operation
V_{OLOWOA}	Low output voltage swing (internal signals) Power = low, Opamp bias = low Power = medium, Opamp bias = low Power = high, Opamp bias = low	 – – –	 – – –	 0.2 0.2 0.2	 V V V	Power = high, Opamp bias = high setting is not allowed for 3.3 V V_{DD} operation
I_{SOA}	Supply current (including associated AGND buffer) Power = low, Opamp bias = low Power = low, Opamp bias = high Power = medium, Opamp bias = low Power = medium, Opamp bias = high Power = high, Opamp bias = low Power = high, Opamp bias = high	 – – – – – –	 400 500 800 1200 2400 –	 800 900 1000 1600 3200 –	 µA µA µA µA µA µA	Power = high, Opamp bias = high setting is not allowed for 3.3 V V_{DD} operation
$PSRR_{OA}$	Supply voltage rejection ratio	65	80	–	dB	$V_{SS} \le V_{IN} \le (V_{DD} - 2.25)$ or $(V_{DD} - 1.25\ V) \le V_{IN} \le V_{DD}$

11.3.5 DC Low Power Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V at 25 °C and are for design guidance only.

Table 16. DC Low Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{REFLPC}	Low power comparator (LPC) reference voltage range	0.2	–	V_{DD} – 1	V	
I_{SLPC}	LPC supply current	–	10	40	µA	
V_{OSLPC}	LPC voltage offset	–	2.5	30	mV	

Table 19. 5-V DC Analog Reference Specifications *(continued)*

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b001	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.092	P2[4] + P2[6] – 0.011	P2[4] + P2[6] + 0.064	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.031	P2[4] – P2[6] + 0.007	P2[4] – P2[6] + 0.056	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.078	P2[4] + P2[6] – 0.008	P2[4] + P2[6] + 0.063	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.031	P2[4] – P2[6] + 0.004	P2[4] – P2[6] + 0.043	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.073	P2[4] + P2[6] – 0.006	P2[4] + P2[6] + 0.062	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.032	P2[4] – P2[6] + 0.003	P2[4] – P2[6] + 0.038	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.073	P2[4] + P2[6] – 0.006	P2[4] + P2[6] + 0.062	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.034	P2[4] – P2[6] + 0.002	P2[4] – P2[6] + 0.037	V
0b010	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.037	V_{DD} – 0.007	V_{DD}	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.036	V_{DD}/2 – 0.001	V_{DD}/2 + 0.036	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.005	V_{SS} + 0.029	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.034	V_{DD} – 0.006	V_{DD}	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.036	V_{DD}/2 – 0.001	V_{DD}/2 + 0.035	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.004	V_{SS} + 0.024	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.032	V_{DD} – 0.005	V_{DD}	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.036	V_{DD}/2 – 0.001	V_{DD}/2 + 0.035	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.003	V_{SS} + 0.022	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.031	V_{DD} – 0.005	V_{DD}	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.037	V_{DD}/2 – 0.001	V_{DD}/2 + 0.035	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.003	V_{SS} + 0.020	V

Table 19. 5-V DC Analog Reference Specifications *(continued)*

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b101	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	P2[4] + Bandgap (P2[4] = V_{DD}/2)	P2[4] + 1.218	P2[4] + 1.291	P2[4] + 1.354	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap (P2[4] = V_{DD}/2)	P2[4] – 1.335	P2[4] – 1.294	P2[4] – 1.237	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	P2[4] + Bandgap (P2[4] = V_{DD}/2)	P2[4] + 1.221	P2[4] + 1.293	P2[4] + 1.358	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap (P2[4] = V_{DD}/2)	P2[4] – 1.337	P2[4] – 1.297	P2[4] – 1.243	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	P2[4] + Bandgap (P2[4] = V_{DD}/2)	P2[4] + 1.222	P2[4] + 1.294	P2[4] + 1.360	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap (P2[4] = V_{DD}/2)	P2[4] – 1.338	P2[4] – 1.298	P2[4] – 1.245	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	P2[4] + Bandgap (P2[4] = V_{DD}/2)	P2[4] + 1.221	P2[4] + 1.294	P2[4] + 1.362	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap (P2[4] = V_{DD}/2)	P2[4] – 1.340	P2[4] – 1.298	P2[4] – 1.245	V
0b110	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	2 × Bandgap	2.513	2.593	2.672	V
		V_{AGND}	AGND	Bandgap	1.264	1.302	1.340	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.008	V_{SS} + 0.038	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	2 × Bandgap	2.514	2.593	2.674	V
		V_{AGND}	AGND	Bandgap	1.264	1.301	1.340	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.005	V_{SS} + 0.028	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	2 × Bandgap	2.514	2.593	2.676	V
		V_{AGND}	AGND	Bandgap	1.264	1.301	1.340	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.004	V_{SS} + 0.024	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	2 × Bandgap	2.514	2.593	2.677	V
		V_{AGND}	AGND	Bandgap	1.264	1.300	1.340	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.003	V_{SS} + 0.021	V

Table 25. AC Chip Level Specifications *(continued)*

Symbol	Description	Min	Typ	Max	Units	Notes
$t_{POWERUP}$	Time from end of POR to CPU executing code	–	16	100	ms	Power-up from 0 V. See the System Resets section of the PSoC Technical Reference Manual.
t_{jit_IMO}[32]	24 MHz IMO cycle-to-cycle jitter (RMS)	–	200	1200	ps	
	24 MHz IMO long term N cycle-to-cycle jitter (RMS)	–	900	6000	ps	N=32
	24 MHz IMO period jitter (RMS)	–	200	900	ps	

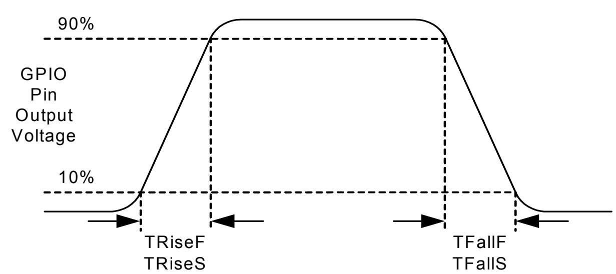
11.4.2 AC GPIO Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 26. AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO operating frequency	0	–	12	MHz	Normal strong mode
t_{RiseF}	Rise time, normal strong mode, Cload = 50 pF	3	–	18	ns	V_{DD} = 4.5 to 5.25 V, 10% to 90%
t_{FallF}	Fall time, normal strong mode, Cload = 50 pF	2	–	18	ns	V_{DD} = 4.5 to 5.25 V, 10% to 90%
t_{RiseS}	Rise time, slow strong mode, Cload = 50 pF	10	27	–	ns	V_{DD} = 3 to 5.25 V, 10% to 90%
t_{FallS}	Fall time, slow strong mode, Cload = 50 pF	10	22	–	ns	V_{DD} = 3 to 5.25 V, 10% to 90%

Figure 12. GPIO Timing Diagram



Notes
29. 4.75 V < V_{DD} < 5.25 V.
30. 3.0 V < V_{DD} < 3.6 V. See application note Adjusting PSoC® Trims for 3.3 V and 2.7 V Operation – AN2012 for information on trimming for operation at 3.3 V.
31. See the individual user module datasheets for information on maximum frequencies for user modules.
32. Refer to Cypress Jitter Specifications application note, Understanding Datasheet Jitter Specifications for Cypress Timing Products – AN5054 for more information.

- Getting Started guide
- USB 2.0 cable

12.4.2 CY3207ISSP In-System Serial Programmer (ISSP)

The CY3207ISSP is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production-programming environment.

Note: CY3207ISSP needs special software and is not compatible with PSoC Programmer. The kit includes:

- CY3207 programmer unit
- PSoC ISSP software CD
- 110 ~ 240 V power supply, Euro-Plug adapter
- USB 2.0 cable

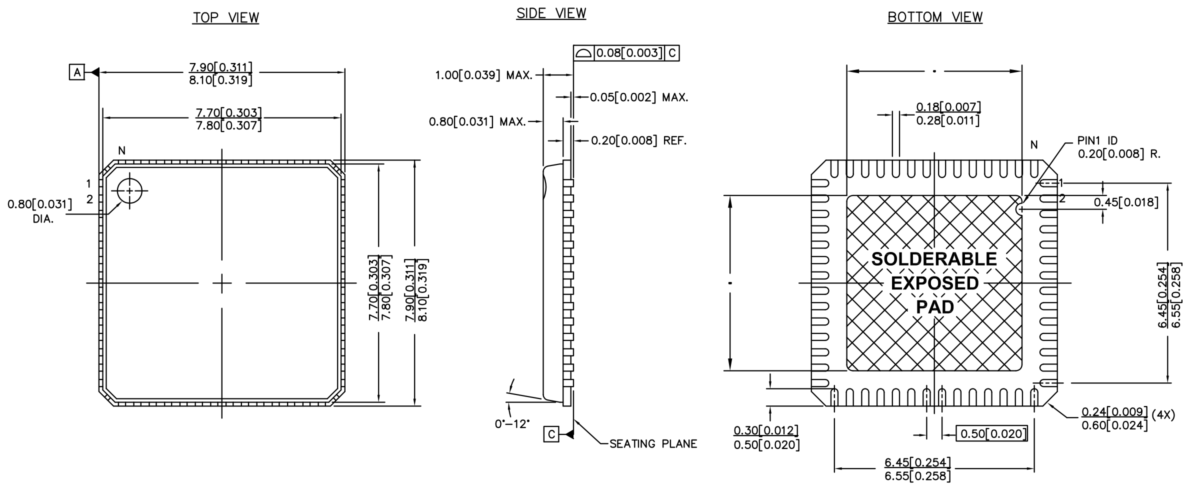
12.5 Accessories (Emulation and Programming)

Table 39. Emulation and Programming Accessories

Part #	Pin Package	Flex-Pod Kit[38]	Foot Kit[39]	Adapter[40]
CY8C24794-24LQXI	56-pin QFN	CY3250-24X94QFN	None	Adapters can be found at http://www.emulation.com.

Notes
38. Flex-Pod kit includes a practice flex-pod and a practice PCB, in addition to two flex-pods.
39. Foot kit includes surface mount feet that are soldered to the target PCB.
40. Programming adapter converts non-DIP package to DIP footprint. Specific details and ordering information for each of the adapters are found at http://www.emulation.com.

Figure 17. 56-pin QFN (8 × 8 × 1.0 mm) LF56A/LY56A 4.5 × 5.21 E-Pad (Subcon Punch Type Pkg.) Package Outline, 001-12921



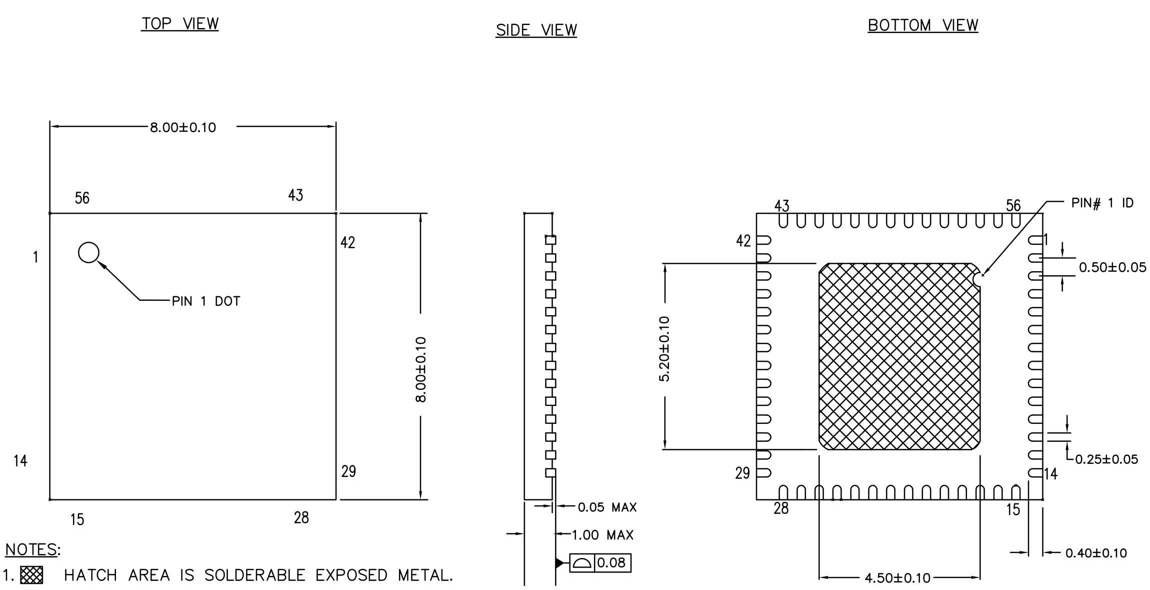
NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO−220
3. PACKAGE WEIGHT: 0.162g
4. ALL DIMENSIONS ARE IN MM [MIN/MAX]
5. PACKAGE CODE

PART #	DESCRIPTION
LF56A	STANDARD
LY56A	PB−FREE

001-12921 *C

Figure 18. 56-pin QFN (8 × 8 × 1.0 mm) LT56B 4.5 × 5.2 E-Pad (Sawn) Package Outline, 001-53450

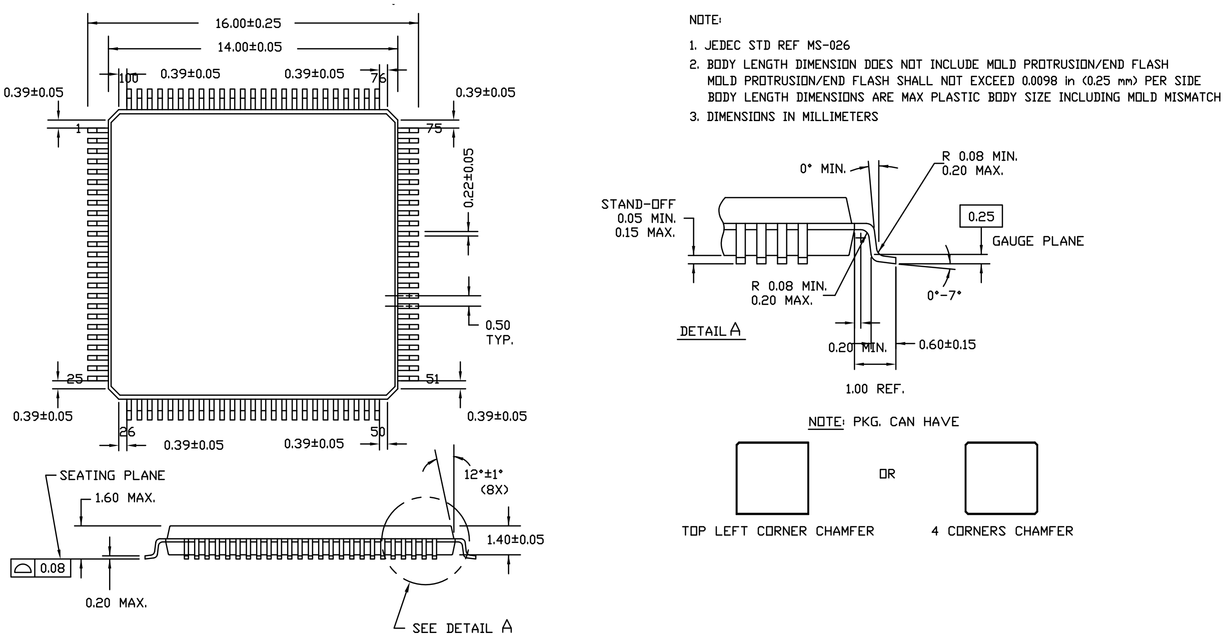


NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO−220
3. PACKAGE WEIGHT: 162 ± 16 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-53450 *D

Figure 21. 100-pin TQFP (14 × 14 × 1.4 mm) A100SA Package Outline, 51-85048



51-85048 *J

Important Note

- For information on the preferred dimensions for mounting QFN packages, see the Application Note, *Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages* available at http://www.amkor.com.
- Pinned vias for thermal conduction are not required for the low power PSoC device.

15. Acronyms

15.1 Acronyms Used

The following table lists the acronyms that are used in this document.

Acronym	Description	Acronym	Description
AC	alternating current	MIPS	million instructions per second
ADC	analog-to-digital converter	OCD	on-chip debug
API	application programming interface	PCB	printed circuit board
CMOS	complementary metal oxide semiconductor	PDIP	plastic dual-in-line package
CPU	central processing unit	PGA	programmable gain amplifier
CRC	cyclic redundancy check	POR	power-on reset
CT	continuous time	PPOR	precision power-on reset
DAC	digital-to-analog converter	PRS	pseudo-random sequence
DC	direct current	PSoC®	Programmable System-on-Chip™
DTMF	dual-tone multi-frequency	PWM	pulse-width modulator
EEPROM	electrically erasable programmable read-only memory	QFN	quad flat no leads
GPIO	general purpose I/O	SAR	successive approximation register
ICE	in-circuit emulator	SC	switched capacitor
IDE	integrated development environment	SLIMO	slow IMO
ILO	internal low-speed oscillator	SOIC	small-outline integrated circuit
IMO	internal main oscillator	SPI™	serial peripheral interface
I/O	input/output	SRAM	static random-access memory
IrDA	infrared data association	SROM	supervisory read-only memory
ISSP	In-System Serial Programming	TQFP	thin quad flat pack
LCD	liquid crystal display	UART	universal asynchronous receiver / transmitter
LED	light-emitting diode	USB	universal serial bus
LPC	low power comparator	VFBGA	very fine-pitch ball grid array
LVD	low-voltage detect	WDT	watchdog timer
MAC	multiply-accumulate	XRES	external reset
MCU	microcontroller unit		

4. The Internal Main Oscillator (IMO) frequency parameter (FIMO245V) may increase over a period of time during usage in the field and exceed the maximum spec limit of 24.96 MHz.

- **PROBLEM DEFINITION**

  When the device has been operating at 4.75 V to 5.25 V for a cumulatively long duration in the field, the IMO Frequency may slowly increase over the duration of usage in the field and eventually exceed the maximum spec limit of 24.96 MHz. This may affect applications that are sensitive to the max value of IMO frequency, such as those using UART communication and result in a functional failure.

- **TRIGGER CONDITION(S)**

  Very long (cumulative) usage of the device in the operating voltage range of 4.75V to 5.25V, with the IMO clock running continuously, could lead to the degradation. Higher power supply voltage and lower ambient temperature are worst-case conditions for the degradation.

- **WORKAROUND**

  Operating the device with the power supply voltage range of 3.0 V to 3.6 V, would avoid the degradation of IMO Frequency beyond the max spec limit of 24.96 MHz.

- **FIX STATUS**

  A new revision of the silicon, with a fix for this issue, is expected to be available from August 1st 2015.

19. Document History Page *(continued)*

Document Title: CY8C24094/CY8C24794/CY8C24894/CY8C24994, PSoC® Programmable System-on-Chip™ Document Number: 38-12018				
*N	2708135	BRW	05/18/2009	Added Note in the Pin Information section on page 8. Removed reference to Hi-Tech Lite Compiler in the section Development Tools Selection on page 42.
*O	2718162	DPT	06/11/2009	Added 56-Pin QFN (Sawn) package diagram and updated ordering information
*P	2762161	RLRM	09/10/2009	Updated the following parameters: DC_{ILO}, F32K_U, F_{IMO6}, $T_{POWERUP}$, T_{ERASE_ALL}, $T_{PROGRAM\_HOT}$, and $T_{PROGRAM\_COLD}$. Added SR_{POWER_UP} parameter in AC specs table.
*Q	2768530	RLRM	09/24/09	Ordering Information table: Changed XRES Pin value for CY8C24894-24LTXI and CY8C24894-24LTXIT to 'Yes'.
*R	2817938	KRIS	11/30/09	Ordering Information: Updated CY8C24894-24LTXI and CY8C24894-24LTXIT parts as Sawn and updated the Digital I/O and Analog Pin values Added Contents page. Updated 68 QFN package diagram (51-85124)
*S	2846641	RLRM	1/12/10	Added package diagram 001-58740 and updated Development Tools section.
*T	2867363	ANUP	01/27/10	Modified Note 9 to remove voltage range 2.4 V to 3.0 V
*U	2901653	NJF	03/30/2010	Updated Cypress website links Added T_{XRST}, DC24M, $T_{BAKETEMP}$ and $T_{BAKETIME}$ parameters Removed reference to 2.4 V Removed sections 'Third Party Tools' 'Build a PSoC Emulator into your Board' Updated package diagrams Removed inactive parts from ordering information table.
*V	2938528	VMAD	05/28/2010	Updated content to match current style guide and datasheet template. No technical updates
*W	3028596	NJF	09/20/10	Added PSoC Device Characteristics table. Added DC I^2C Specifications table. Added F_{32K_U} max limit. Added Tjit_IMO specification, removed existing jitter specifications. Updated Analog reference tables. Updated Units of Measure, Acronyms, Glossary, and References sections. Updated solder reflow specifications. No specific changes were made to AC Digital Block Specifications table and I^2C Timing Diagram. They were updated for clearer understanding. Updated Figure 12 since the labelling for y-axis was incorrect. Template and styles update.
*X	3082244	NXZ	11/09/2010	Sunset review; no updates.
*Y	3111357	BTK / NJF / ARVM	12/15/10	Updated solder reflow specifications. Removed F_{IMO6} spec from AC chip-level specifications table. Removed the following pruned parts from the ordering information table and their references in the datasheet. 1) CY8C24794-24LFXI 2) CY8C24794-24LFXIT 3) CY8C24894-24LFXI 4) CY8C24894-24LFXIT
*Z	3126167	BTK / ANBA / PKS	01/03/11	Updated ordering information. Removed the package diagram spec 51-85214 since there are no MPNs in the ordering information table that corresponds with this package. Updated ordering code definitions for clearer understanding.
AA	3367463	BTK / GIR	09/22/11	Updated V_{REFHI} values for parameter '0b100' under Table 19 on page 31. Updated text under Table 19 on page 31. The text "Pin must be left floating" is included under Description of NC pin in Table 4 on page 12, Table 6 on page 14, Table 7 on page 16, and Table 8 on page 18. Updated Table 38 on page 51 to give more clarity.
AB	3404970	MATT	10/13/11	Removed prune device CY8C24994-24BVXI from Ordering Information.
AC	3461872	CSAI	12/13/2011	Sunset review; no content update