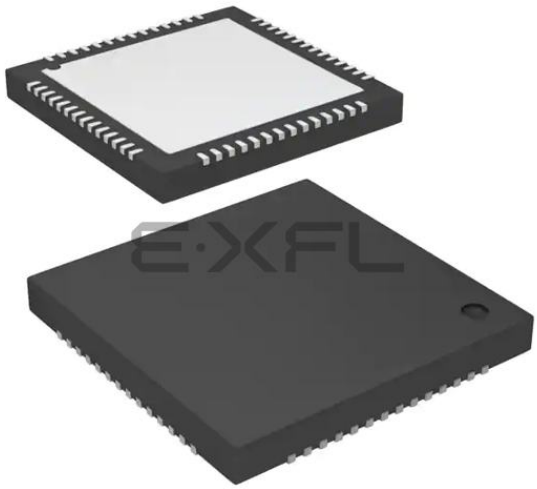

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Details	
Product Status	Active
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Core Size	8-Bit
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Connectivity	I²C, SPI, UART/USART, USB
Peripherals	POR, PWM, WDT
Number of I/O	50
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	A/D 47x14b; D/A 2x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	56-VFQFN Exposed Pad
Supplier Device Package	56-QFN-EP (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c24894-24ltxi

3. More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right PSoC device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the knowledge base article KBA92181, Resources Available for CapSense® Controllers. Following is an abbreviated list for CapSense devices:

- Overview: CapSense Portfolio, CapSense Roadmap
- Product Selectors: CapSense, CapSense Plus, CapSense Express, PSoC3 with CapSense, PSoC5 with CapSense, PSoC4. In addition, PSoC Designer offers a device selection tool at the time of creating a new project.
- Application notes: Cypress offers CapSense application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with CapSense are:
  - AN64846: Getting Started With CapSense
  - AN2397: CapSense® Data Viewing Tools
- Technical Reference Manual (TRM):
  - CY8CPLC20, CY8CLED16P01, CY8C29x66, CY8C27x43, CY8C24x94, CY8C24x23, CY8C24x23A, CY8C22x13, CY8C21x34, CY8C21x34B, CY8C21x23, CY7C64215, CY7C603xx, CY8CNP1xx, and CYWUSB6953 PSoC® Programmable System-on-Chip TRM
- Development Kits:
  - CY3280-24x94 Universal CapSense Controller Board features a predefined control circuitry and plug-in hardware to make prototyping and debugging easy. Programming and I2C-to-USB Bridge hardware are included for tuning and data acquisition.
  - CY3280-BMM Matrix Button Module Kit consists of eight CapSense sensors organized in a 4x4 matrix format to form 16 physical buttons and eight LEDs. This module connects to any CY3280 Universal CapSense Controller Board, including CY3280-20x66 Universal CapSense Controller.
  - CY3280-BSM Simple Button Module Kit consists of ten CapSense buttons and ten LEDs. This module connects to any CY3280 Universal CapSense Controller Board, including CY3280-20x66 Universal CapSense Controller.

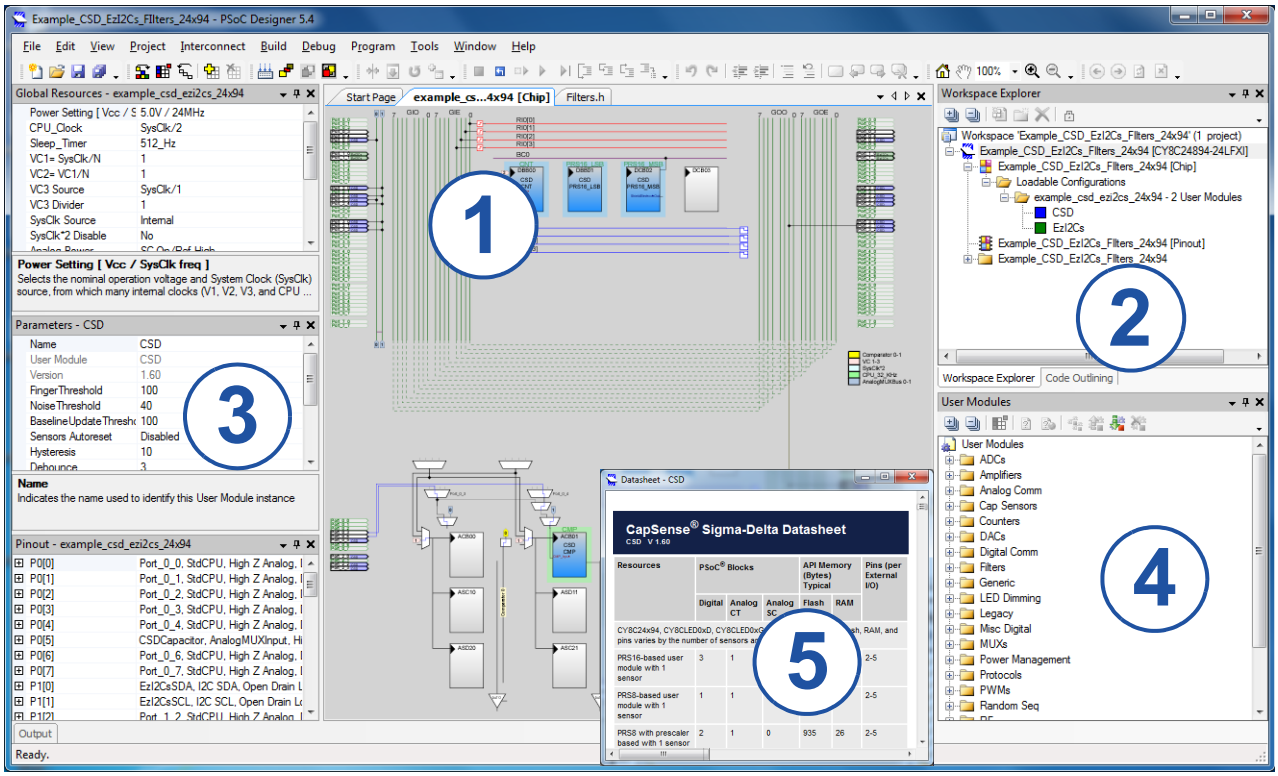
The CY3217-MiniProg1 and CY8CKIT-002 PSoC® MiniProg3 device provides an interface for flash programming.

3.1 PSoC Designer

PSoC Designer is a free Windows-based Integrated Design Environment (IDE). It enables concurrent hardware and firmware design of systems based on CapSense (see Figure 1). With PSoC Designer, you can:

1. Drag and drop User Modules to build your hardware system design in the main design workspace
2. Codesign your application firmware with the PSoC hardware, using the PSoC Designer IDE C compiler
3. Configure User Module
4. Explore the library of user modules
5. Review user module datasheets

Figure 1. PSoC Designer Features



9. Pin Information

This section describes, lists, and illustrates the CY8C24x94 PSoC device family pins and pinout configuration.

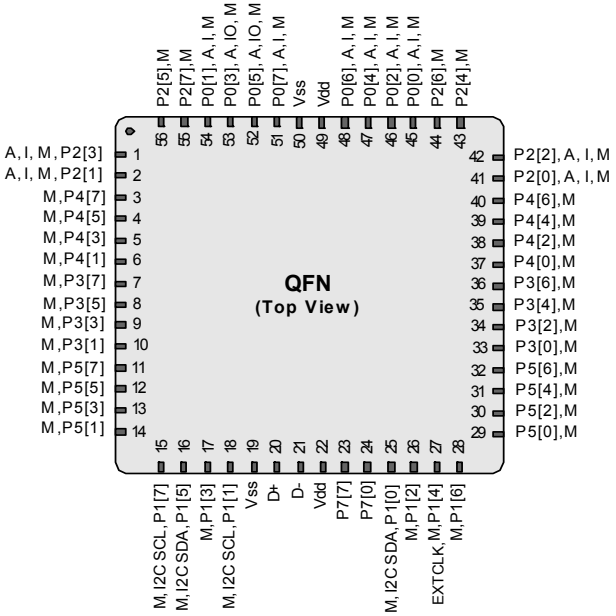
The CY8C24x94 PSoC devices are available in the following packages, all of which are shown on the following pages. Every port pin (labeled with a “P”) is capable of Digital I/O. However, V_{SS}, V_{DD}, and XRES are not capable of Digital I/O.

9.1 56-Pin Part Pinout

Table 2. 56-Pin Part Pinout (QFN[6]) See LEGEND details and footnotes in Table 3 on page 11.

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I, M	P2[3]	Direct switched capacitor block input
2	I/O	I, M	P2[1]	Direct switched capacitor block input
3	I/O	M	P4[7]	
4	I/O	M	P4[5]	
5	I/O	M	P4[3]	
6	I/O	M	P4[1]	
7	I/O	M	P3[7]	
8	I/O	M	P3[5]	
9	I/O	M	P3[3]	
10	I/O	M	P3[1]	
11	I/O	M	P5[7]	
12	I/O	M	P5[5]	
13	I/O	M	P5[3]	
14	I/O	M	P5[1]	
15	I/O	M	P1[7]	I^2C serial clock (SCL)
16	I/O	M	P1[5]	I^2C serial data (SDA)
17	I/O	M	P1[3]	
18	I/O	M	P1[1]	I^2C SCL, ISSP SCLK [4]
19	Power		V_{SS}	Ground connection [5]
20	USB		D+	
21	USB		D–	
22	Power		V_{DD}	Supply voltage
23	I/O		P7[7]	
24	I/O		P7[0]	
25	I/O	M	P1[0]	I^2C SDA, ISSP SDATA[4]
26	I/O	M	P1[2]	
27	I/O	M	P1[4]	Optional external clock input (EXTCLK)
28	I/O	M	P1[6]	
29	I/O	M	P5[0]	
30	I/O	M	P5[2]	
31	I/O	M	P5[4]	
32	I/O	M	P5[6]	
33	I/O	M	P3[0]	
34	I/O	M	P3[2]	
35	I/O	M	P3[4]	
36	I/O	M	P3[6]	
37	I/O	M	P4[0]	
38	I/O	M	P4[2]	
39	I/O	M	P4[4]	
40	I/O	M	P4[6]	
41	I/O	I, M	P2[0]	Direct switched capacitor block input
42	I/O	I, M	P2[2]	Direct switched capacitor block input
43	I/O	M	P2[4]	External analog ground (AGND) input
44	I/O	M	P2[6]	External voltage reference (VREF) input
45	I/O	I, M	P0[0]	Analog column mux input
46	I/O	I, M	P0[2]	Analog column mux input
47	I/O	I, M	P0[4]	Analog column mux input VREF
48	I/O	I, M	P0[6]	Analog column mux input
49	Power		V_{DD}	Supply voltage
50	Power		V_{SS}	Ground connection [5]
51	I/O	I, M	P0[7]	Analog column mux input
52	I/O	I/O, M	P0[5]	Analog column mux input and column output
53	I/O	I/O, M	P0[3]	Analog column mux input and column output
54	I/O	I, M	P0[1]	Analog column mux input
55	I/O	M	P2[7]	
56	I/O	M	P2[5]	

Figure 4. CY8C24794 56-Pin PSoC Device[3]



Notes
3. This part cannot be programmed with Reset mode; use Power Cycle mode when programming.
4. These are the ISSP pins, which are not High Z at POR. See the PSoC Technical Reference Manual for details.
5. All V_{SS} pins should be brought out to one common GND plane.

9.4 68-Pin Part Pinout (On-Chip Debug)

The following 68-pin QFN part table and drawing is for the CY8C24094 OCD PSoC device.

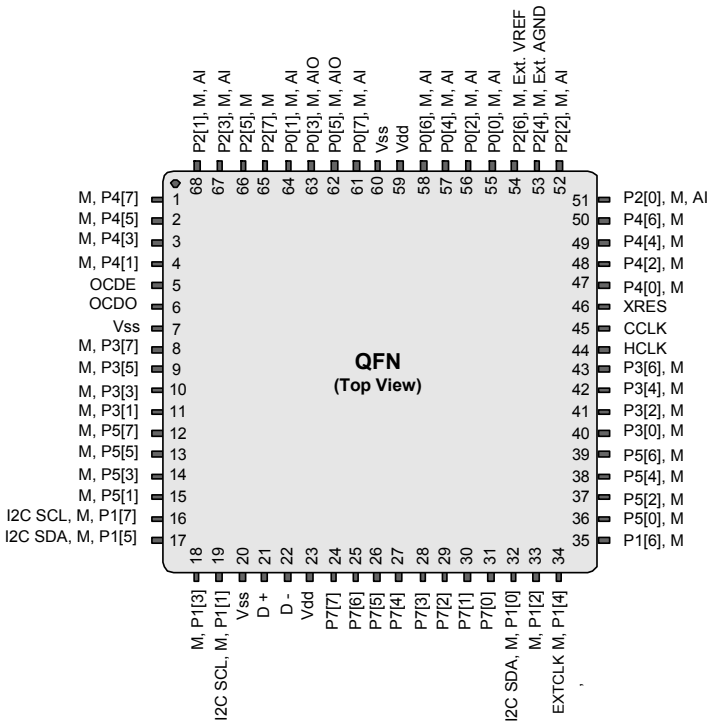
Note This part is only used for in-circuit debugging. It is NOT available for production.

Table 5. 68-Pin Part Pinout (QFN[12])

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	M	P4[7]	
2	I/O	M	P4[5]	
3	I/O	M	P4[3]	
4	I/O	M	P4[1]	
5			OCDE	OCD even data I/O
6			OCDO	OCD odd data output
7	Power		V_{SS}	Ground connection [13]
8	I/O	M	P3[7]	
9	I/O	M	P3[5]	
10	I/O	M	P3[3]	
11	I/O	M	P3[1]	
12	I/O	M	P5[7]	
13	I/O	M	P5[5]	
14	I/O	M	P5[3]	
15	I/O	M	P5[1]	
16	I/O	M	P1[7]	I^2C SCL
17	I/O	M	P1[5]	I^2C SDA
18	I/O	M	P1[3]	
19	I/O	M	P1[1]	I^2C SCL, ISSP SCLK [14]
20	Power		V_{SS}	Ground connection [13]
21	USB		D+	
22	USB		D–	
23	Power		V_{DD}	Supply voltage
24	I/O		P7[7]	
25	I/O		P7[6]	
26	I/O		P7[5]	
27	I/O		P7[4]	
28	I/O		P7[3]	
29	I/O		P7[2]	
30	I/O		P7[1]	
31	I/O		P7[0]	
32	I/O	M	P1[0]	I^2C SDA, ISSP SDATA[14]
33	I/O	M	P1[2]	
34	I/O	M	P1[4]	Optional EXTCLK
35	I/O	M	P1[6]	
36	I/O	M	P5[0]	
37	I/O	M	P5[2]	
38	I/O	M	P5[4]	
39	I/O	M	P5[6]	
40	I/O	M	P3[0]	
41	I/O	M	P3[2]	
42	I/O	M	P3[4]	
43	I/O	M	P3[6]	
44			HCLK	OCD high speed clock output
45			CCLK	OCD CPU clock output
46	Input		XRES	Active high pin reset with internal pull-down
47	I/O	M	P4[0]	
48	I/O	M	P4[2]	
49	I/O	M	P4[4]	
50	I/O	M	P4[6]	
51	I/O	I, M	P2[0]	Direct switched capacitor block input
52	I/O	I, M	P2[2]	Direct switched capacitor block input
53	I/O	M	P2[4]	External AGND input
54	I/O	M	P2[6]	External VREF input
55	I/O	I, M	P0[0]	Analog column mux input
56	I/O	I, M	P0[2]	Analog column mux input and column output
57	I/O	I, M	P0[4]	Analog column mux input and column output
58	I/O	I, M	P0[6]	Analog column mux input
59	Power		V_{DD}	Supply voltage
60	Power		V_{SS}	Ground connection [13]
61	I/O	I, M	P0[7]	Analog column mux input, integration input #1
62	I/O	I/O, M	P0[5]	Analog column mux input and column output, integration input #2
63	I/O	I/O, M	P0[3]	Analog column mux input and column output
64	I/O	I, M	P0[1]	Analog column mux input
65	I/O	M	P2[7]	
66	I/O	M	P2[5]	
67	I/O	I, M	P2[3]	Direct switched capacitor block input
68	I/O	I, M	P2[1]	Direct switched capacitor block input

LEGEND A = Analog, I = Input, O = Output, M = Analog Mux Input, OCD = On-Chip Debugger.

Figure 7. CY8C24094 68-Pin OCD PSoC Device



Notes

12. The center pad on the QFN package should be connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it should be electrically floated and not connected to any other signal.
13. All V_{SS} pins should be brought out to one common GND plane.
14. These are the ISSP pins, which are not High Z at POR. See the PSoC Technical Reference Manual for details.

9.5 100-Ball VFBGA Part Pinout

The 100-ball VFBGA part is for the CY8C24994 PSoC device.

Table 6. 100-Ball Part Pinout (VFBGA[15])

Pin No.	Digital	Analog	Name	Description	Pin No.	Digital	Analog	Name	Description
A1	Power		V_{SS}	Ground connection	F1			NC	No connection. Pin must be left floating
A2	Power		V_{SS}	Ground connection	F2	I/O	M	P5[7]	
A3			NC	No connection. Pin must be left floating	F3	I/O	M	P3[5]	
A4			NC	No connection. Pin must be left floating	F4	I/O	M	P5[1]	
A5			NC	No connection. Pin must be left floating	F5	Power		V_{SS}	Ground connection
A6	Power		V_{DD}	Supply voltage	F6	Power		V_{SS}	Ground connection
A7			NC	No connection. Pin must be left floating	F7	I/O	M	P5[0]	
A8			NC	No connection. Pin must be left floating	F8	I/O	M	P3[0]	
A9	Power		V_{SS}	Ground connection	F9			XRES	Active high pin reset with internal pull-down
A10	Power		V_{SS}	Ground connection	F10	I/O		P7[1]	
B1	Power		V_{SS}	Ground connection	G1			NC	No connection. Pin must be left floating
B2	Power		V_{SS}	Ground connection	G2	I/O	M	P5[5]	
B3	I/O	I, M	P2[1]	Direct switched capacitor block input	G3	I/O	M	P3[3]	
B4	I/O	I, M	P0[1]	Analog column mux input	G4	I/O	M	P1[7]	I^2C SCL
B5	I/O	I, M	P0[7]	Analog column mux input	G5	I/O	M	P1[1]	I^2C SCL, ISSP SCLK[16]
B6	Power		V_{DD}	Supply voltage	G6	I/O	M	P1[0]	I^2C SDA, ISSP SDATA[16]
B7	I/O	I, M	P0[2]	Analog column mux input	G7	I/O	M	P1[6]	
B8	I/O	I, M	P2[2]	Direct switched capacitor block input	G8	I/O	M	P3[4]	
B9	Power		V_{SS}	Ground connection	G9	I/O	M	P5[6]	
B10	Power		V_{SS}	Ground connection	G10	I/O		P7[2]	
C1			NC	No connection. Pin must be left floating	H1			NC	No connection. Pin must be left floating
C2	I/O	M	P4[1]		H2	I/O	M	P5[3]	
C3	I/O	M	P4[7]		H3	I/O	M	P3[1]	
C4	I/O	M	P2[7]		H4	I/O	M	P1[5]	I^2C SDA
C5	I/O	I/O, M	P0[5]	Analog column mux input and column output	H5	I/O	M	P1[3]	
C6	I/O	I, M	P0[6]	Analog column mux input	H6	I/O	M	P1[2]	
C7	I/O	I, M	P0[0]	Analog column mux input	H7	I/O	M	P1[4]	Optional EXTCLK
C8	I/O	I, M	P2[0]	Direct switched capacitor block input	H8	I/O	M	P3[2]	
C9	I/O	M	P4[2]		H9	I/O	M	P5[4]	
C10			NC	No connection. Pin must be left floating	H10	I/O		P7[3]	
D1			NC	No connection. Pin must be left floating	J1	Power		V_{SS}	Ground connection
D2	I/O	M	P3[7]		J2	Power		V_{SS}	Ground connection
D3	I/O	M	P4[5]		J3	USB		D+	
D4	I/O	M	P2[5]		J4	USB		D–	
D5	I/O	I/O, M	P0[3]	Analog column mux input and column output	J5	Power		V_{DD}	Supply voltage
D6	I/O	I,M	P0[4]	Analog column mux input	J6	I/O		P7[7]	
D7	I/O	M	P2[6]	External VREF input	J7	I/O		P7[0]	
D8	I/O	M	P4[6]		J8	I/O	M	P5[2]	
D9	I/O	M	P4[0]		J9	Power		V_{SS}	Ground connection
D10			NC	No connection. Pin must be left floating	J10	Power		V_{SS}	Ground connection
E1			NC	No connection. Pin must be left floating	K1	Power		V_{SS}	Ground connection
E2			NC	No connection. Pin must be left floating	K2	Power		V_{SS}	Ground connection
E3	I/O	M	P4[3]		K3			NC	No connection. Pin must be left floating
E4	I/O	I, M	P2[3]	Direct switched capacitor block input	K4			NC	No connection. Pin must be left floating
E5	Power		V_{SS}	Ground connection	K5	Power		V_{DD}	Supply voltage
E6	Power		V_{SS}	Ground connection	K6	I/O		P7[6]	
E7	I/O	M	P2[4]	External AGND input	K7	I/O		P7[5]	
E8	I/O	M	P4[4]		K8	I/O		P7[4]	
E9	I/O	M	P3[6]		K9	Power		V_{SS}	Ground connection
E10			NC	No connection. Pin must be left floating	K10	Power		V_{SS}	Ground connection

LEGEND A = Analog, I = Input, O = Output, M = Analog Mux Input, NC = No connection. Pin must be left floating.

11.3.2 DC GPIO Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 12. DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull-up resistor	4	5.6	8	kΩ	
R_{PD}	Pull-down resistor	4	5.6	8	kΩ	
V_{OH}	High output level	V_{DD} – 1.0	–	–	V	I_{OH} = 10 mA, V_{DD} = 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or V_{DD} = 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). 80 mA maximum combined I_{OH} budget.
V_{OL}	Low output level	–	–	0.75	V	I_{OL} = 25 mA, V_{DD} = 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or V_{DD} = 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). 200 mA maximum combined I_{OL} budget.
I_{OH}	High level source current	10	–	–	mA	V_{OH} = V_{DD} – 1.0 V, see the limitations of the total current in the note for V_{OH}
I_{OL}	Low level sink current	25	–	–	mA	V_{OL} = 0.75 V, see the limitations of the total current in the note for V_{OL}
V_{IL}	Input low level	–	–	0.8	V	V_{DD} = 3.0 to 5.25.
V_{IH}	Input high level	2.1	–		V	V_{DD} = 3.0 to 5.25.
V_H	Input hysterisis	–	60	–	mV	
I_{IL}	Input leakage (absolute value)	–	1	–	nA	Gross tested to 1 µA.
C_{IN}	Capacitive load on pins as input	–	3.5	10	pF	Package and pin dependent. Temp = 25 °C.
C_{OUT}	Capacitive load on pins as output	–	3.5	10	pF	Package and pin dependent. Temp = 25 °C.

11.3.4 DC Operational Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V and 3.3 V at 25 °C and are for design guidance only.

The operational amplifier is a component of both the analog continuous time PSoC blocks and the analog switched capacitor PSoC blocks. The guaranteed specifications are measured in the analog continuous time PSoC block.

Table 14. 5-V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input offset voltage (absolute value) Power = low, Opamp bias = high Power = medium, Opamp bias = high Power = high, Opamp bias = high	 – – –	 1.6 1.3 1.2	 10 8 7.5	 mV mV mV	
TCV_{OSOA}	Average input offset voltage drift	–	7.0	35.0	µV/°C	
I_{EBOA}	Input leakage current (Port 0 analog pins)	–	20	–	pA	Gross tested to 1 µA.
C_{INOA}	Input capacitance (Port 0 analog pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25 °C.
V_{CMOA}	Common mode voltage range Common mode voltage range (high power or high Opamp bias)	0.0 0.5	– –	V_{DD} V_{DD} – 0.5	V V	The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
G_{OLOA}	Open loop gain Power = low, Opamp bias = high Power = medium, Opamp bias = high Power = high, Opamp bias = high	 60 60 80	 – – –	 – – –	 dB dB dB	
$V_{OHIGHOA}$	High output voltage swing (internal signals) Power = low, Opamp bias = high Power = medium, Opamp bias = high Power = high, Opamp bias = high	 V_{DD} – 0.2 V_{DD} – 0.2 V_{DD} – 0.5	 – – –	 – – –	 V V V	
V_{OLOWOA}	Low output voltage swing (internal signals) Power = low, Opamp bias = high Power = medium, Opamp bias = high Power = high, Opamp bias = high	 – – –	 – – –	 0.2 0.2 0.5	 V V V	
I_{SOA}	Supply current (including associated AGND buffer) Power = low, Opamp bias = low Power = low, Opamp bias = high Power = medium, Opamp bias = low Power = medium, Opamp bias = high Power = high, Opamp bias = low Power = high, Opamp bias = high	 – – – – – –	 400 500 800 1200 2400 4600	 800 900 1000 1600 3200 6400	 µA µA µA µA µA µA	
$PSRR_{OA}$	Supply voltage rejection ratio	65	80	–	dB	$V_{SS} \le V_{IN} \le (V_{DD} – 2.25)$ or $(V_{DD} – 1.25\ V) \le V_{IN} \le V_{DD}$.

11.3.6 DC Analog Output Buffer Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 17. 5-V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
C_L	Load Capacitance	–	–	200	pF	This specification applies to the external circuit that is being driven by the analog output buffer.
V_{OSOB}	Input offset voltage (absolute value)	–	3	12	mV	
TCV_{OSOB}	Average input offset voltage drift	–	+6	–	µV/°C	
V_{CMOB}	Common mode input voltage range	0.5	–	V_{DD} – 1.0	V	
R_{OUTOB}	Output resistance Power = low Power = high	 – –	 0.6 0.6	 – –	 Ω Ω	
$V_{OHIGHOB}$	High output voltage swing (Load = 32 ohms to V_{DD}/2) Power = low Power = high	 0.5 × V_{DD} + 1.1 0.5 × V_{DD} + 1.1	 – –	 – –	 V V	
V_{OLOWOB}	Low output voltage swing (Load = 32 ohms to V_{DD}/2) Power = low Power = high	 – –	 – –	 0.5 × V_{DD} – 1.3 0.5 × V_{DD} – 1.3	 V V	
I_{SOB}	Supply current including opamp bias cell (No Load) Power = low Power = high	 – –	 1.1 2.6	 5.1 8.8	 mA mA	
$PSRR_{OB}$	Supply voltage rejection ratio	53	64	–	dB	(0.5 × V_{DD} – 1.3) ≤ V_{OUT} ≤ (V_{DD} – 2.3).

Table 18. 3.3-V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
C_L	Load Capacitance	–	–	200	pF	This specification applies to the external circuit that is being driven by the analog output buffer.
V_{OSOB}	Input offset voltage (absolute value)	–	3	12	mV	
TCV_{OSOB}	Average input offset voltage drift	–	+6	–	µV/°C	
V_{CMOB}	Common mode input voltage range	0.5	–	V_{DD} – 1.0	V	
R_{OUTOB}	Output resistance Power = low Power = high	 – –	 1 1	 – –	 W W	
$V_{OHIGHOB}$	High output voltage swing (Load = 1 K ohms to $V_{DD}/2$) Power = low Power = high	 $0.5 \times V_{DD} + 1.0$ $0.5 \times V_{DD} + 1.0$	 – –	 – –	 V V	
V_{OLOWOB}	Low output voltage swing (Load = 1 K ohms to $V_{DD}/2$) Power = low Power = high	 – –	 – –	 $0.5 \times V_{DD} - 1.0$ $0.5 \times V_{DD} - 1.0$	 V V	
I_{SOB}	Supply current including opamp bias cell (No load) Power = low Power = high	 – –	 0.8 2.0	 2.0 4.3	 mA mA	
$PSRR_{OB}$	Supply voltage rejection ratio	34	64	–	dB	$(0.5 \times V_{DD} - 1.0) \le V_{OUT} \le (0.5 \times V_{DD} + 0.9)$.

Table 19. 5-V DC Analog Reference Specifications *(continued)*

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b001	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.092	P2[4] + P2[6] – 0.011	P2[4] + P2[6] + 0.064	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.031	P2[4] – P2[6] + 0.007	P2[4] – P2[6] + 0.056	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.078	P2[4] + P2[6] – 0.008	P2[4] + P2[6] + 0.063	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.031	P2[4] – P2[6] + 0.004	P2[4] – P2[6] + 0.043	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.073	P2[4] + P2[6] – 0.006	P2[4] + P2[6] + 0.062	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.032	P2[4] – P2[6] + 0.003	P2[4] – P2[6] + 0.038	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.073	P2[4] + P2[6] – 0.006	P2[4] + P2[6] + 0.062	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.034	P2[4] – P2[6] + 0.002	P2[4] – P2[6] + 0.037	V
0b010	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.037	V_{DD} – 0.007	V_{DD}	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.036	V_{DD}/2 – 0.001	V_{DD}/2 + 0.036	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.005	V_{SS} + 0.029	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.034	V_{DD} – 0.006	V_{DD}	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.036	V_{DD}/2 – 0.001	V_{DD}/2 + 0.035	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.004	V_{SS} + 0.024	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.032	V_{DD} – 0.005	V_{DD}	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.036	V_{DD}/2 – 0.001	V_{DD}/2 + 0.035	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.003	V_{SS} + 0.022	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.031	V_{DD} – 0.005	V_{DD}	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.037	V_{DD}/2 – 0.001	V_{DD}/2 + 0.035	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.003	V_{SS} + 0.020	V

Table 20. 3.3-V DC Analog Reference Specifications

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b000	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.200	$V_{DD}/2$ + 1.290	$V_{DD}/2$ + 1.365	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.030	$V_{DD}/2$	$V_{DD}/2$ + 0.034	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.346	$V_{DD}/2$ – 1.292	$V_{DD}/2$ – 1.208	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.196	$V_{DD}/2$ + 1.292	$V_{DD}/2$ + 1.374	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.029	$V_{DD}/2$	$V_{DD}/2$ + 0.031	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.349	$V_{DD}/2$ – 1.295	$V_{DD}/2$ – 1.227	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.204	$V_{DD}/2$ + 1.293	$V_{DD}/2$ + 1.369	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.030	$V_{DD}/2$	$V_{DD}/2$ + 0.030	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.351	$V_{DD}/2$ – 1.297	$V_{DD}/2$ – 1.229	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.189	$V_{DD}/2$ + 1.294	$V_{DD}/2$ + 1.384	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.032	$V_{DD}/2$	$V_{DD}/2$ + 0.029	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.353	$V_{DD}/2$ – 1.297	$V_{DD}/2$ – 1.230	V
0b001	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.105	P2[4] + P2[6] – 0.008	P2[4] + P2[6] + 0.095	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.035	P2[4] – P2[6] + 0.006	P2[4] – P2[6] + 0.053	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.094	P2[4] + P2[6] – 0.005	P2[4] + P2[6] + 0.073	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.033	P2[4] – P2[6] + 0.002	P2[4] – P2[6] + 0.042	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.094	P2[4] + P2[6] – 0.003	P2[4] + P2[6] + 0.075	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.035	P2[4] – P2[6]	P2[4] – P2[6] + 0.038	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.095	P2[4] + P2[6] – 0.003	P2[4] + P2[6] + 0.080	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.038	P2[4] – P2[6]	P2[4] – P2[6] + 0.038	V

Table 20. 3.3-V DC Analog Reference Specifications *(continued)*

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b110	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	2 × Bandgap	2.510	2.595	2.655	V
		V_{AGND}	AGND	Bandgap	1.276	1.301	1.332	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.006	V_{SS} + 0.031	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	2 × Bandgap	2.513	2.594	2.656	V
		V_{AGND}	AGND	Bandgap	1.275	1.301	1.331	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.004	V_{SS} + 0.021	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	2 × Bandgap	2.516	2.595	2.657	V
		V_{AGND}	AGND	Bandgap	1.275	1.301	1.331	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.003	V_{SS} + 0.017	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	2 × Bandgap	2.520	2.595	2.658	V
		V_{AGND}	AGND	Bandgap	1.275	1.300	1.331	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.002	V_{SS} + 0.015	V
0b111	All power settings. Not allowed for 3.3 V.	–	–	–	–	–	–	–

11.3.8 DC Analog PSoC Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 21. DC Analog PSoC Block Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{CT}	Resistor unit value (continuous time)	–	12.2	–	kΩ	
C_{SC}	Capacitor unit value (switched capacitor)	–	80	–	fF	

11.3.9 DC POR and LVD Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V or 3.3 V at 25 °C and are for design guidance only.

11.4 AC Electrical Characteristics

11.4.1 AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 25. AC Chip Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
$F_{IMO245V}$	Internal main oscillator frequency for 24 MHz (5 V)	23.04	24	24.96[29]	MHz	Trimmed for 5 V operation using factory trim values.
$F_{IMO243V}$	Internal main oscillator frequency for 24 MHz (3.3 V)	22.08	24	25.92[30]	MHz	Trimmed for 3.3 V operation using factory trim values.
$F_{IMOUSB5V}$	Internal main oscillator frequency with USB (5 V) Frequency locking enabled and USB traffic present.	23.94	24	24.06	MHz	–10 °C ≤ T_A ≤ 85 °C 4.35 ≤ V_{DD} ≤ 5.15
$F_{IMOUSB3V}$	Internal main oscillator frequency with USB (3.3 V) Frequency locking enabled and USB traffic present.	23.94	24	24.06	MHz	–0 °C ≤ T_A ≤ 70 °C 3.15 ≤ V_{DD} ≤ 3.45
F_{CPU1}	CPU frequency (5 V nominal)	0.093	24	24.96[29]	MHz	SLIMO Mode = 0.
F_{CPU2}	CPU frequency (3.3 V nominal)	0.086	12	12.96[30]	MHz	SLIMO Mode = 0.
F_{BLK5}	Digital PSoC block frequency (5 V nominal)	0	48	49.92[29,31]	MHz	Refer to the AC digital block Specifications.
F_{BLK3}	Digital PSoC block frequency (3.3 V nominal)	0	24	25.92[31]	MHz	
F_{32K1}	Internal low speed oscillator frequency	15	32	64	kHz	
F_{32K_U}	Internal low speed oscillator untrimmed frequency	5	–	100	kHz	After a reset and before the M8C starts to run, the ILO is not trimmed. See the System Resets section of the PSoC Technical Reference Manual for details on this timing
t_{XRST}	External reset pulse width	10	–	–	µs	
DC24M	24 MHz duty cycle	40	50	60	%	
DC_{ILO}	Internal low speed oscillator duty cycle	20	50	80	%	
Step24M	24 MHz trim step size	–	50	–	kHz	
Fout48M	48 MHz output frequency	46.08	48.0	49.92[29,30]	MHz	Trimmed. Utilizing factory trim values.
F_{MAX}	Maximum frequency of signal on row input or row output.	–	–	12.96	MHz	
SR_{POWER_UP}	Power supply slew rate	–	–	250	V/ms	V_{DD} slew rate during power-up.

Notes

26. The 50,000 cycle flash endurance per block is only guaranteed if the flash is operating within one voltage range. Voltage ranges are 3.0 V to 3.6 V and 4.75 V to 5.25 V.
27. A maximum of 36 × 50,000 block endurance cycles is allowed. This may be balanced between operations on 36 × 1 blocks of 50,000 maximum cycles each, 36 × 2 blocks of 25,000 maximum cycles each, or 36 × 4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36 × 50,000 and ensure that no single block ever sees more than 50,000 cycles).
For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. See the Flash APIs application note Design Aids – Reading and Writing PSoC® Flash – AN2015 for more information.
28. All GPIOs meet the DC GPIO V_{IL} and V_{IH} specifications found in the DC GPIO Specifications sections. The I^2C GPIO pins also meet the mentioned specifications.

11.4.9 AC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 35. AC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{RSCLK}	Rise time of SCLK	1	–	20	ns	
t_{FSCLK}	Fall time of SCLK	1	–	20	ns	
t_{SSCLK}	Data setup time to falling edge of SCLK	40	–	–	ns	
t_{HSCLK}	Data hold time from falling edge of SCLK	40	–	–	ns	
F_{SCLK}	Frequency of SCLK	0	–	8	MHz	
t_{ERASEB}	Flash erase time (block)	–	10	–	ms	
t_{WRITE}	Flash block write time	–	40	–	ms	
t_{DSCLK}	Data out delay from falling edge of SCLK	–	–	45	ns	V_{DD} > 3.6
t_{DSCLK3}	Data out delay from falling edge of SCLK	–	–	50	ns	3.0 ≤ V_{DD} ≤ 3.6
$t_{ERASEALL}$	Flash erase time (bulk)	–	40	–	ms	Erase all blocks and protection fields at once
$t_{PROGRAM\_HOT}$	Flash block erase + flash block write time	–	–	100[34]	ms	0 °C ≤ Tj ≤ 100 °C
$t_{PROGRAM\_COLD}$	Flash block erase + flash block write time	–	–	200[34]	ms	–40 °C ≤ Tj ≤ 0 °C

Note

34. For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. See the Flash APIs application note Design Aids – Reading and Writing PSoC® Flash – AN2015 for more information.

- Getting Started guide
- USB 2.0 cable

12.4.2 CY3207ISSP In-System Serial Programmer (ISSP)

The CY3207ISSP is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production-programming environment.

Note: CY3207ISSP needs special software and is not compatible with PSoC Programmer. The kit includes:

- CY3207 programmer unit
- PSoC ISSP software CD
- 110 ~ 240 V power supply, Euro-Plug adapter
- USB 2.0 cable

12.5 Accessories (Emulation and Programming)

Table 39. Emulation and Programming Accessories

Part #	Pin Package	Flex-Pod Kit[38]	Foot Kit[39]	Adapter[40]
CY8C24794-24LQXI	56-pin QFN	CY3250-24X94QFN	None	Adapters can be found at http://www.emulation.com.

Notes
38. Flex-Pod kit includes a practice flex-pod and a practice PCB, in addition to two flex-pods.
39. Foot kit includes surface mount feet that are soldered to the target PCB.
40. Programming adapter converts non-DIP package to DIP footprint. Specific details and ordering information for each of the adapters are found at http://www.emulation.com.

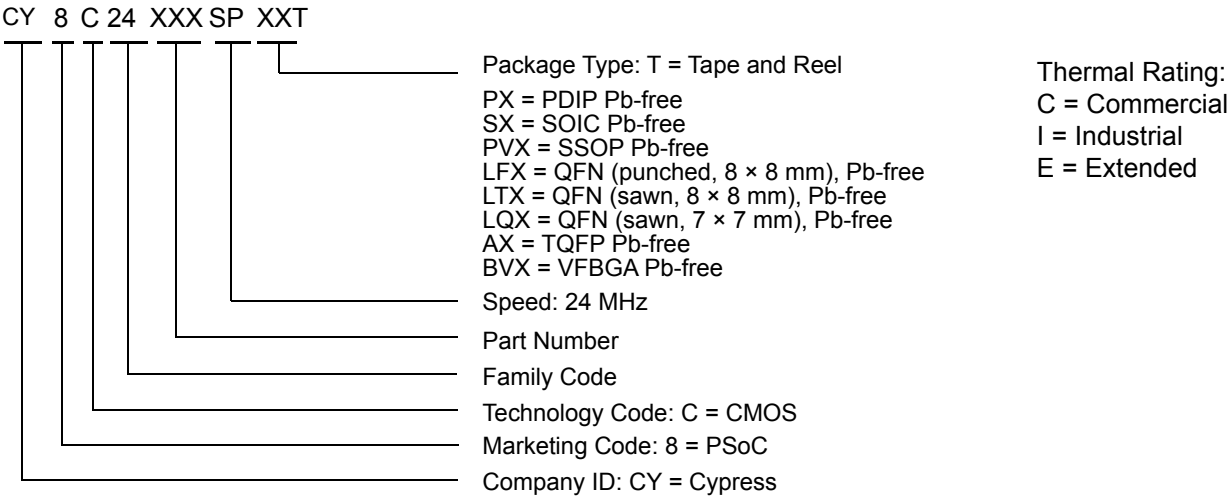
13. Ordering Information

Table 40. CY8C24x94 PSoC Device's Key Features and Ordering Information

Package	Package diagram	Ordering Code	Flash (Bytes)	SRAM (Bytes)	Temperature Range	Digital Blocks	Analog Blocks	Digital I/O Pins	Analog Inputs	Analog Outputs	XRES Pin
100-pin OCD TQFP[41]	51-85048	CY8C24094-24AXI	16 K	1 K	–40 °C to +85 °C	4	6	56	48	2	Yes
56-pin (7 × 7 mm) QFN	001-58740	CY8C24794-24LQXI	16 K	1 K	–40 °C to +85 °C	4	6	50	48	2	No
56-pin (7 × 7 mm) QFN (Tape and Reel)		CY8C24794-24LQXIT	16 K	1 K	–40 °C to +85 °C	4	6	50	48	2	No
56-pin (8 × 8 mm) QFN (Sawn)	001-53450	CY8C24794-24LTXI	16 K	1 K	–40 °C to +85 °C	4	6	50	48	2	No
56-pin (8 × 8 mm) QFN (Sawn) (Tape and Reel)		CY8C24794-24LTXIT	16 K	1 K	–40 °C to +85 °C	4	6	50	48	2	No
56-pin (8 × 8 mm) QFN (Sawn)	001-53450	CY8C24894-24LTXI	16 K	1 K	–40 °C to +85 °C	4	6	49	47	2	Yes
56-pin (8 × 8 mm) QFN (Sawn) (Tape and Reel)		CY8C24894-24LTXIT	16 K	1 K	–40 °C to +85 °C	4	6	49	47	2	Yes
68-pin (8 × 8 mm) QFN (Sawn)	001-09618	CY8C24994-24LTXI	16 K	1 K	–40 °C to +85 °C	4	6	56	48	2	Yes
68-pin QFN (8 × 8 mm) (Sawn) (Tape and Reel)		CY8C24994-24LTXIT	16 K	1 K	–40 °C to +85 °C	4	6	56	48	2	Yes

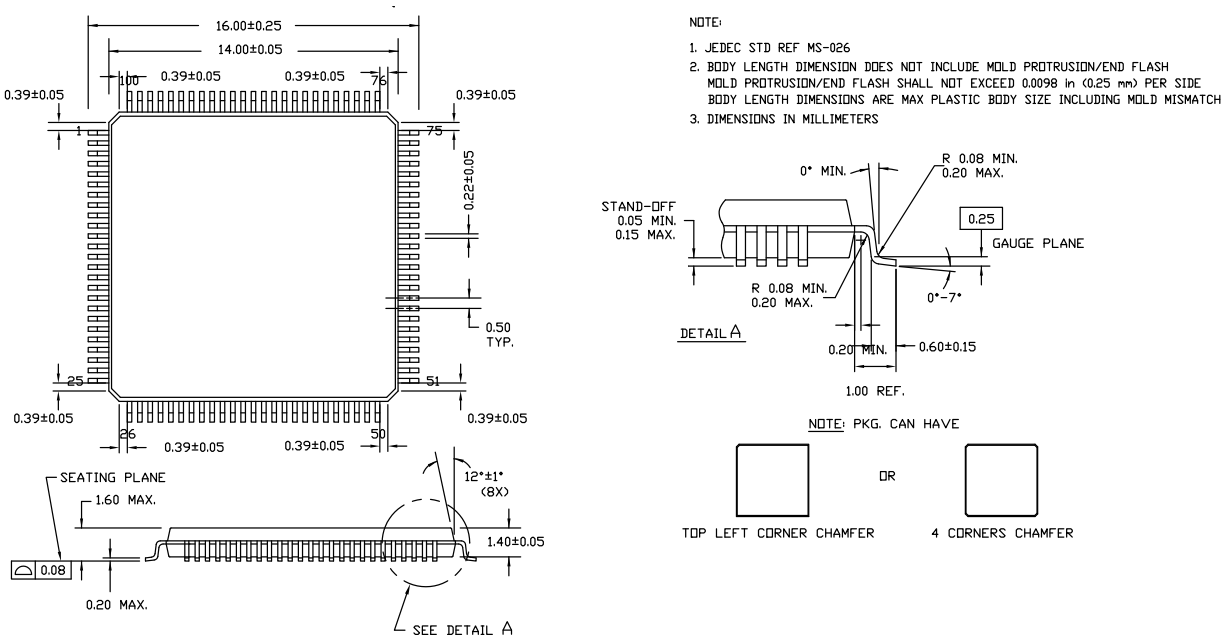
Note For die sales information, contact a local Cypress sales office or Field Applications Engineer (FAE).

13.1 Ordering Code Definitions



Note
41. This part may be used for in-circuit debugging. It is NOT available for production.

Figure 21. 100-pin TQFP (14 × 14 × 1.4 mm) A100SA Package Outline, 51-85048



51-85048 *J

Important Note

- For information on the preferred dimensions for mounting QFN packages, see the Application Note, *Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages* available at http://www.amkor.com.
- Pinned vias for thermal conduction are not required for the low power PSoC device.

15. Acronyms

15.1 Acronyms Used

The following table lists the acronyms that are used in this document.

Acronym	Description	Acronym	Description
AC	alternating current	MIPS	million instructions per second
ADC	analog-to-digital converter	OCD	on-chip debug
API	application programming interface	PCB	printed circuit board
CMOS	complementary metal oxide semiconductor	PDIP	plastic dual-in-line package
CPU	central processing unit	PGA	programmable gain amplifier
CRC	cyclic redundancy check	POR	power-on reset
CT	continuous time	PPOR	precision power-on reset
DAC	digital-to-analog converter	PRS	pseudo-random sequence
DC	direct current	PSoC®	Programmable System-on-Chip™
DTMF	dual-tone multi-frequency	PWM	pulse-width modulator
EEPROM	electrically erasable programmable read-only memory	QFN	quad flat no leads
GPIO	general purpose I/O	SAR	successive approximation register
ICE	in-circuit emulator	SC	switched capacitor
IDE	integrated development environment	SLIMO	slow IMO
ILO	internal low-speed oscillator	SOIC	small-outline integrated circuit
IMO	internal main oscillator	SPI™	serial peripheral interface
I/O	input/output	SRAM	static random-access memory
IrDA	infrared data association	SROM	supervisory read-only memory
ISSP	In-System Serial Programming	TQFP	thin quad flat pack
LCD	liquid crystal display	UART	universal asynchronous receiver / transmitter
LED	light-emitting diode	USB	universal serial bus
LPC	low power comparator	VFBGA	very fine-pitch ball grid array
LVD	low-voltage detect	WDT	watchdog timer
MAC	multiply-accumulate	XRES	external reset
MCU	microcontroller unit		

17. Glossary *(continued)*

modulator	A device that imposes a signal on a carrier.
noise	1. A disturbance that affects a signal and that may distort the information carried by the signal. 2. The random variations of one or more characteristics of any entity such as voltage, current, or data.
oscillator	A circuit that may be crystal controlled and is used to generate a clock frequency.
parity	A technique for testing transmitting data. Typically, a binary digit is added to the data to make the sum of all the digits of the binary data either always even (even parity) or always odd (odd parity).
phase-locked loop (PLL)	An electronic circuit that controls an ***oscillator*** so that it maintains a constant phase angle relative to a reference signal.
pinouts	The pin number assignment: the relation between the logical inputs and outputs of the PSoC device and their physical counterparts in the printed circuit board (PCB) package. Pinouts involve pin numbers as a link between schematic and PCB design (both being computer generated files) and may also involve pin names.
port	A group of pins, usually eight.
power on reset (POR)	A circuit that forces the PSoC device to reset when the voltage is lower than a pre-set level. This is one type of hardware reset.
PSoC®	Cypress Semiconductor's PSoC® is a registered trademark and Programmable System-on-Chip™ is a trademark of Cypress.
PSoC Designer™	The software for Cypress' Programmable System-on-Chip technology.
pulse width modulator (PWM)	An output in the form of duty cycle which varies as a function of the applied measurand
RAM	An acronym for random access memory. A data-storage device from which data can be read out and new data can be written in.
register	A storage device with a specific capacity, such as a bit or byte.
reset	A means of bringing a system back to a know state. See hardware reset and software reset.
ROM	An acronym for read only memory. A data-storage device from which data can be read out, but new data cannot be written in.
serial	1. Pertaining to a process in which all events occur one after the other. 2. Pertaining to the sequential or consecutive occurrence of two or more related activities in a single device or channel.
settling time	The time it takes for an output signal or value to stabilize after the input has changed from one value to another.
shift register	A memory storage device that sequentially shifts a word either left or right to output a stream of serial data.
slave device	A device that allows another device to control the timing for data exchanges between two devices. Or when devices are cascaded in width, the slave device is the one that allows another device to control the timing of data exchanges between the cascaded devices and an external interface. The controlling device is called the master device.

4. The Internal Main Oscillator (IMO) frequency parameter (FIMO245V) may increase over a period of time during usage in the field and exceed the maximum spec limit of 24.96 MHz.

■ **PROBLEM DEFINITION**

When the device has been operating at 4.75 V to 5.25 V for a cumulatively long duration in the field, the IMO Frequency may slowly increase over the duration of usage in the field and eventually exceed the maximum spec limit of 24.96 MHz. This may affect applications that are sensitive to the max value of IMO frequency, such as those using UART communication and result in a functional failure.

■ **TRIGGER CONDITION(S)**

Very long (cumulative) usage of the device in the operating voltage range of 4.75V to 5.25V, with the IMO clock running continuously, could lead to the degradation. Higher power supply voltage and lower ambient temperature are worst-case conditions for the degradation.

■ **WORKAROUND**

Operating the device with the power supply voltage range of 3.0 V to 3.6 V, would avoid the degradation of IMO Frequency beyond the max spec limit of 24.96 MHz.

■ **FIX STATUS**

A new revision of the silicon, with a fix for this issue, is expected to be available from August 1st 2015.

19. Document History Page

Document Title: CY8C24094/CY8C24794/CY8C24894/CY8C24994, PSoC® Programmable System-on-Chip™ Document Number: 38-12018				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	133189	NWJ	01/27/2004	New silicon and new document – Advance datasheet.
*A	251672	SFV	See ECN	First Preliminary datasheet. Changed title to encompass only the CY8C24794 because the CY8C24494 and CY8C24694 are not being offered by Cypress.
*B	289742	HMT	See ECN	Add standard DS items from SFV memo. Add Analog Input Mux on pinouts. 2 MACs. Change 512 bytes of SRAM to 1 K. Add dimension key to package. Remove HAPI. Update diagrams, registers and specs.
*C	335236	HMT	See ECN	Add CY logo. Update CY copyright. Update new CY.com URLs. Re-add ISSP programming pinout notation. Add Reflow Temp. table. Update features (MAC, Oscillator, and voltage range), registers (INT_CLR2/MSK2, second MAC), and specs. (Rext, IMO, analog output buffer...).
*D	344318	HMT	See ECN	Add new color and logo. Expand analog arch. diagram. Fix I/O #. Update Electrical Specifications.
*E	346774	HMT	See ECN	Add USB temperature specifications. Make datasheet Final.
*F	349566	HMT	See ECN	Remove USB logo. Add URL to preferred dimensions for mounting MLF packages.
*G	393164	HMT	See ECN	Add new device, CY8C24894 56-pin MLF with XRES pin. Add Fimousb3v char. to specs. Upgrade to CY Perform logo and update corporate address and copyright.
*H	469243	HMT	See ECN	Add ISSP note to pinout tables. Update typical and recommended Storage Temperature per industrial specs. Update Low Output Level maximum I/OL budget. Add FLS_PR1 to Register Map Bank 1 for users to specify which Flash bank should be used for SROM operations. Add two new devices for a 68-pin QFN and 100-ball VFBGA under RPNs: CY8C24094 and CY8C24994. Add two packages for 68-pin QFN. Add OCD non-production pinouts and package diagrams. Update CY branding and QFN convention. Add new Dev. Tool section. Update copyright and trademarks.
*I	561158	HMT	See ECN	Add Low Power Comparator (LPC) AC/DC electrical spec. tables. Add CY8C20x34 to PSoC Device Characteristics table. Add detailed dimensions to 56-pin QFN package diagram and update revision. Secure one package diagram/manufacturing per QFN. Update emulation pod/feet kit part numbers. Fix pinout type-o per TestTrack.
*J	728238	HMT	See ECN	Add CapSense SNR requirement reference. Update figure standards. Update Technical Training paragraphs. Add QFN package clarifications and dimensions. Update ECN-ed Amkor dimensioned QFN package diagram revisions. Reword SNR reference. Add new 56-pin QFN spec.
*K	2552459	AZIE / PYRS	08/14/08	Add footnote on AGND descriptions to avoid using P2[4] for digital signaling as it may add noise to AGND. Remove reference to CMP_GO_EN1 in Map Bank 1 Table on Address 65; this register has no functionality on 24xxx. Add footnote on die sales. Add description 'Optional External Clock Input' on P1[4] to match description of P1[4].
*L	2616550	OGNE / PYRS	12/05/08	Updated Programmable Pin Configuration detail. Changed title from PSoC® Mixed-Signal Array to PSoC® Programmable System-on-Chip™
*M	2657956	DPT / PYRS	02/11/09	Added package diagram 001-09618 and updated Ordering Information table