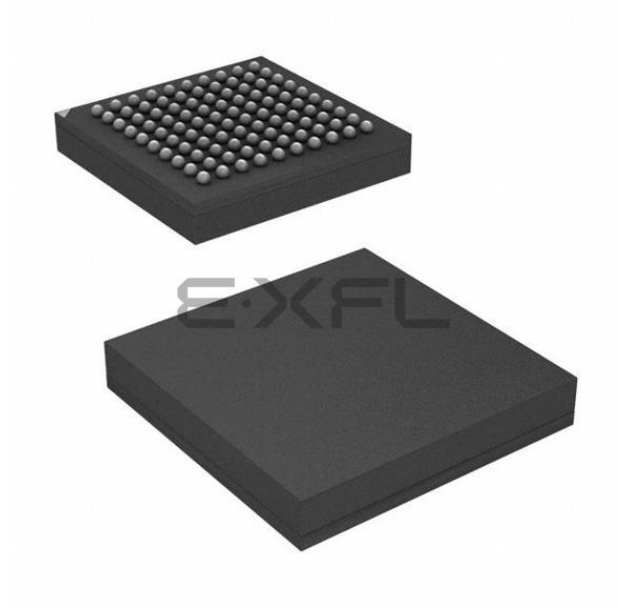

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SPI, UART/USART, USB
Peripherals	POR, PWM, WDT
Number of I/O	56
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	A/D 48x14b; D/A 2x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-VFBGA
Supplier Device Package	100-VFBGA (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c24994-24bvxi

5. PSoC Functional Overview

The PSoC family consists of many devices with on-chip controllers. These devices are designed to replace multiple traditional MCU-based system components with one low-cost single-chip programmable component. A PSoC device includes configurable blocks of analog and digital logic, and programmable interconnect. This architecture makes it possible for you to create customized peripheral configurations, to match the requirements of each individual application. Additionally, a fast central processing unit (CPU), flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts.

The PSoC architecture, shown in "Logic Block Diagram" on page 1, consists of four main areas: the core, the system resources, the digital system, and the analog system. Configurable global bus resources allow combining all of the device resources into a complete custom system. Each CY8C24x94 PSoC device includes four digital blocks and six analog blocks. Depending on the PSoC package, up to 56 GPIOs are also included. The GPIOs provide access to the global digital and analog interconnects.

5.1 The PSoC Core

The PSoC core is a powerful engine that supports a rich instruction set. It encompasses SRAM for data storage, an interrupt controller, sleep and watchdog timers, and internal main oscillator (IMO) and internal low-speed oscillator (ILO). The CPU core, called the M8C, is a powerful processor with speeds up to 24 MHz. The M8C is a four-million instructions per second (MIPS) 8-bit Harvard-architecture microprocessor.

System resources provide these additional capabilities:

- Digital clocks for increased flexibility
- I^2C functionality to implement an I^2C master and slave
- An internal voltage reference, multi-master, that provides an absolute value of 1.3 V to a number of PSoC subsystems
- A switch-mode pump (SMP) that generates normal operating voltages from a single battery cell
- Various system resets supported by the M8C

The digital system consists of an array of digital PSoC blocks that may be configured into any number of digital peripherals. The digital blocks are connected to the GPIOs through a series of global buses. These buses can route any signal to any pin, freeing designs from the constraints of a fixed peripheral controller.

The analog system consists of six analog PSoC blocks, supporting comparators, and analog-to-digital conversion up to 10-bits of precision.

5.2 The Digital System

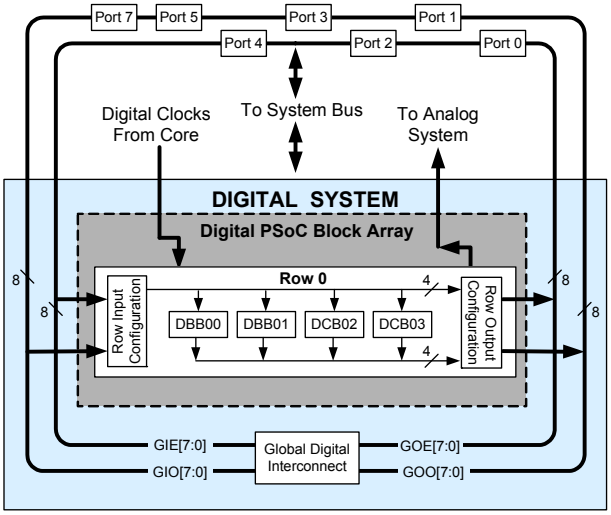
The digital system consists of four digital PSoC blocks. Each block is an 8-bit resource that is used alone or combined with other blocks to form 8-, 16-, 24-, and 32-bit peripherals, which are called user modules. Digital peripheral configurations include:

- PWMs (8- to 32-bit)
- PWMs with dead band (8- to 32-bit)
- Counters (8- to 32-bit)
- Timers (8- to 32-bit)
- UART 8-bit with selectable parity
- SPI master and slave
- I^2C slave and multi-master
- CRC/generator (8-bit)
- IrDA
- PRS generators (8- to 32-bit)

The digital blocks are connected to any GPIO through a series of global buses that can route any signal to any pin. The buses also allow for signal multiplexing and for performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

Digital blocks are provided in rows of four, where the number of blocks varies by PSoC device family. This allows the optimum choice of system resources for your application. Family resources are shown in Table 1 on page 7.

Figure 2. Digital System Block Diagram



6. Getting Started

For in-depth information, along with detailed programming information, see the Technical Reference Manual for this PSoC device.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device datasheets on the web at http://www.cypress.com.

6.1 Application Notes

Cypress application notes are an excellent introduction to the wide variety of possible PSoC designs.

6.2 Development Kits

PSoC Development Kits are available online from and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

6.3 Training

Free PSoC technical training (on demand, webinars, and workshops), which is available online via www.cypress.com, covers a wide variety of topics and skill levels to assist you in your designs.

6.4 CYPros Consultants

Certified PSoC consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC consultant go to the CYPros Consultants web site.

6.5 Solutions Library

Visit our growing library of solution-focused designs. Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

6.6 Technical Support

Technical support – including a searchable Knowledge Base articles and technical forums – is also available online. If you cannot find an answer to your question, call our Technical Support hotline at 1-800-541-4736.

7. Development Tools

PSoC Designer™ is the revolutionary Integrated Design Environment (IDE) that you can use to customize PSoC to meet your specific application requirements. PSoC Designer software accelerates system design and time to market. Develop your applications using a library of precharacterized analog and digital peripherals (called user modules) in a drag-and-drop design environment. Then, customize your design by leveraging the dynamically generated application programming interface (API) libraries of code. Finally, debug and test your designs with the integrated debug environment, including in-circuit emulation and standard software debug features. PSoC Designer includes:

- Application editor graphical user interface (GUI) for device and user module configuration and dynamic reconfiguration
- Extensive user module catalog
- Integrated source-code editor (C and assembly)
- Free C compiler with no size restrictions or time limits
- Built-in debugger
- In-circuit emulation
- Built-in support for communication interfaces:
  - Hardware and software I^2C slaves and masters
  - Full speed USB 2.0
  - Up to four full-duplex universal asynchronous receiver/transmitters (UARTs), SPI master and slave, and wireless

PSoC Designer supports the entire library of PSoC 1 devices and runs on Windows XP, Windows Vista, and Windows 7.

7.1 PSoC Designer Software Subsystems

7.1.1 Design Entry

In the chip-level view, choose a base device to work with. Then select different onboard analog and digital components that use the PSoC blocks, which are called user modules. Examples of user modules are analog-to-digital converters (ADCs), digital-to-analog converters (DACs), amplifiers, and filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration makes it possible to change configurations at run time. In essence, this allows you to use more than 100 percent of PSoC's resources for an application.

7.1.2 Code Generation Tools

The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. You can develop your design in C, assembly, or a combination of the two.

Assemblers. The assemblers allow you to merge assembly code seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and are linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all of the features of C, tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

7.1.3 Debugger

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow you to read and program and

9. Pin Information

This section describes, lists, and illustrates the CY8C24x94 PSoC device family pins and pinout configuration.

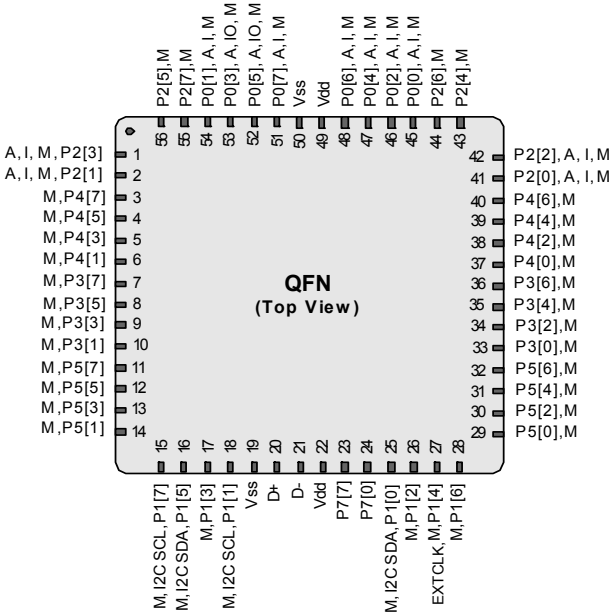
The CY8C24x94 PSoC devices are available in the following packages, all of which are shown on the following pages. Every port pin (labeled with a “P”) is capable of Digital I/O. However, V_{SS}, V_{DD}, and XRES are not capable of Digital I/O.

9.1 56-Pin Part Pinout

Table 2. 56-Pin Part Pinout (QFN[6]) See LEGEND details and footnotes in Table 3 on page 11.

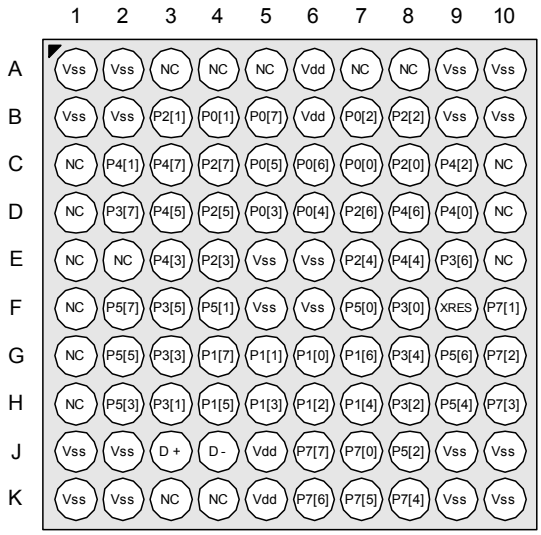
Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I, M	P2[3]	Direct switched capacitor block input
2	I/O	I, M	P2[1]	Direct switched capacitor block input
3	I/O	M	P4[7]	
4	I/O	M	P4[5]	
5	I/O	M	P4[3]	
6	I/O	M	P4[1]	
7	I/O	M	P3[7]	
8	I/O	M	P3[5]	
9	I/O	M	P3[3]	
10	I/O	M	P3[1]	
11	I/O	M	P5[7]	
12	I/O	M	P5[5]	
13	I/O	M	P5[3]	
14	I/O	M	P5[1]	
15	I/O	M	P1[7]	I^2C serial clock (SCL)
16	I/O	M	P1[5]	I^2C serial data (SDA)
17	I/O	M	P1[3]	
18	I/O	M	P1[1]	I^2C SCL, ISSP SCLK [4]
19	Power		V_{SS}	Ground connection [5]
20	USB		D+	
21	USB		D–	
22	Power		V_{DD}	Supply voltage
23	I/O		P7[7]	
24	I/O		P7[0]	
25	I/O	M	P1[0]	I^2C SDA, ISSP SDATA[4]
26	I/O	M	P1[2]	
27	I/O	M	P1[4]	Optional external clock input (EXTCLK)
28	I/O	M	P1[6]	
29	I/O	M	P5[0]	
30	I/O	M	P5[2]	
31	I/O	M	P5[4]	
32	I/O	M	P5[6]	
33	I/O	M	P3[0]	
34	I/O	M	P3[2]	
35	I/O	M	P3[4]	
36	I/O	M	P3[6]	
37	I/O	M	P4[0]	
38	I/O	M	P4[2]	
39	I/O	M	P4[4]	
40	I/O	M	P4[6]	
41	I/O	I, M	P2[0]	Direct switched capacitor block input
42	I/O	I, M	P2[2]	Direct switched capacitor block input
43	I/O	M	P2[4]	External analog ground (AGND) input
44	I/O	M	P2[6]	External voltage reference (VREF) input
45	I/O	I, M	P0[0]	Analog column mux input
46	I/O	I, M	P0[2]	Analog column mux input
47	I/O	I, M	P0[4]	Analog column mux input VREF
48	I/O	I, M	P0[6]	Analog column mux input
49	Power		V_{DD}	Supply voltage
50	Power		V_{SS}	Ground connection [5]
51	I/O	I, M	P0[7]	Analog column mux input
52	I/O	I/O, M	P0[5]	Analog column mux input and column output
53	I/O	I/O, M	P0[3]	Analog column mux input and column output
54	I/O	I, M	P0[1]	Analog column mux input
55	I/O	M	P2[7]	
56	I/O	M	P2[5]	

Figure 4. CY8C24794 56-Pin PSoC Device[3]



Notes
3. This part cannot be programmed with Reset mode; use Power Cycle mode when programming.
4. These are the ISSP pins, which are not High Z at POR. See the PSoC Technical Reference Manual for details.
5. All V_{SS} pins should be brought out to one common GND plane.

Figure 8. CY8C24094 OCD (Not for Production)



BGA (Top View)

Notes
15. All V_{SS} pins should be brought out to one common GND plane.
16. These are the ISSP pins, which are not High Z at POR. See the PSoC Technical Reference Manual for details.

9.7 100-Pin Part Pinout (On-Chip Debug)

The 100-pin TQFP part is for the CY8C24094 OCD PSoC device.

Note This part is only used for in-circuit debugging. It is NOT available for production.

Table 8. 100-Pin Part Pinout (TQFP[19])

Pin No.	Digital	Analog	Name	Description	Pin No.	Digital	Analog	Name	Description
1			NC	No connection. Pin must be left floating	51	I/O	M	P1[6]	
2			NC	No connection. Pin must be left floating	52	I/O	M	P5[0]	
3	I/O	I, M	P0[1]	Analog column mux input	53	I/O	M	P5[2]	
4	I/O	M	P2[7]		54	I/O	M	P5[4]	
5	I/O	M	P2[5]		55	I/O	M	P5[6]	
6	I/O	I, M	P2[3]	Direct switched capacitor block input	56	I/O	M	P3[0]	
7	I/O	I, M	P2[1]	Direct switched capacitor block input	57	I/O	M	P3[2]	
8	I/O	M	P4[7]		58	I/O	M	P3[4]	
9	I/O	M	P4[5]		59	I/O	M	P3[6]	
10	I/O	M	P4[3]		60			HCLK	OCD high speed clock output
11	I/O	M	P4[1]		61			CCLK	OCD CPU clock output
12			OCDE	OCD even data I/O	62	Input		XRES	Active high pin reset with internal pull-down
13			OCDO	OCD odd data output	63	I/O	M	P4[0]	
14			NC	No connection. Pin must be left floating	64	I/O	M	P4[2]	
15	Power		V_{SS}	Ground connection	65	Power		V_{SS}	Ground connection
16	I/O	M	P3[7]		66	I/O	M	P4[4]	
17	I/O	M	P3[5]		67	I/O	M	P4[6]	
18	I/O	M	P3[3]		68	I/O	I, M	P2[0]	Direct switched capacitor block input
19	I/O	M	P3[1]		69	I/O	I, M	P2[2]	Direct switched capacitor block input
20	I/O	M	P5[7]		70	I/O		P2[4]	External AGND input
21	I/O	M	P5[5]		71			NC	No connection. Pin must be left floating
22	I/O	M	P5[3]		72	I/O		P2[6]	External VREF input
23	I/O	M	P5[1]		73			NC	No connection. Pin must be left floating
24	I/O	M	P1[7]	I^2C SCL	74	I/O	I	P0[0]	Analog column mux input
25			NC	No connection. Pin must be left floating	75			NC	No connection. Pin must be left floating
26			NC	No connection. Pin must be left floating	76			NC	No connection. Pin must be left floating
27			NC	No connection. Pin must be left floating	77	I/O	I, M	P0[2]	Analog column mux input and column output
28	I/O		P1[5]	I^2C SDA	78			NC	No connection. Pin must be left floating
29	I/O		P1[3]		79	I/O	I, M	P0[4]	Analog column mux input and column output
30	I/O		P1[1]	Crystal (XTALin), I^2C SCL, ISSP SCLK[20]	80			NC	No connection. Pin must be left floating
31			NC	No connection. Pin must be left floating	81	I/O	I, M	P0[6]	Analog column mux input
32	Power		V_{SS}	Ground connection	82	Power		V_{DD}	Supply voltage
33	USB		D+		83			NC	No connection. Pin must be left floating
34	USB		D-		84	Power		V_{SS}	Ground connection
35	Power		V_{DD}	Supply voltage	85			NC	No connection. Pin must be left floating
36	I/O		P7[7]		86			NC	No connection. Pin must be left floating
37	I/O		P7[6]		87			NC	No connection. Pin must be left floating
38	I/O		P7[5]		88			NC	No connection. Pin must be left floating
39	I/O		P7[4]		89			NC	No connection. Pin must be left floating
40	I/O		P7[3]		90			NC	No connection. Pin must be left floating
41	I/O		P7[2]		91			NC	No connection. Pin must be left floating
42	I/O		P7[1]		92			NC	No connection. Pin must be left floating
43	I/O		P7[0]		93			NC	No connection. Pin must be left floating
44			NC	No connection. Pin must be left floating	94			NC	No connection. Pin must be left floating
45			NC	No connection. Pin must be left floating	95	I/O	I, M	P0[7]	Analog column mux input
46			NC	No connection. Pin must be left floating	96			NC	No connection. Pin must be left floating
47			NC	No connection. Pin must be left floating	97	I/O	I/O, M	P0[5]	Analog column mux input and column output
48	I/O		P1[0]	Crystal (XTALout), I2C SDA, ISSP SDATA[20]	98			NC	No connection. Pin must be left floating
49	I/O		P1[2]		99	I/O	I/O, M	P0[3]	Analog column mux input and column output
50	I/O		P1[4]	Optional EXTCLK	100			NC	No connection. Pin must be left floating

LEGEND A = Analog, I = Input, O = Output, NC = No connection. Pin must be left floating, M = Analog Mux Input, OCD = On-Chip Debugger.

Notes

19. All V_{SS} pins should be brought out to one common GND plane.
20. These are the ISSP pins, which are not High Z at POR. See the PSoC Technical Reference Manual for details.

11.2 Operating Temperature

Table 10. Operating Temperature

Symbol	Description	Min	Typ	Max	Units	Notes
T_A	Ambient temperature	–40	–	+85	°C	
T_{AUSB}	Ambient temperature using USB	–10	–	+85	°C	
T_J	Junction temperature	–40	–	+100	°C	The temperature rise from ambient to junction is package specific. See Thermal Impedance on page 51. The user must limit the power consumption to comply with this requirement.

11.3 DC Electrical Characteristics

11.3.1 DC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 11. DC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DD}	Supply voltage	3.0	–	5.25	V	See DC POR and LVD specifications, Table 22 on page 39.
I_{DD5}	Supply current, IMO = 24 MHz (5 V)	–	14	27	mA	Conditions are V_{DD} = 5.0 V, T_A = 25 °C, CPU = 3 MHz, SYSCLK doubler disabled, VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 93.75 kHz, analog power = off.
I_{DD3}	Supply current, IMO = 24 MHz (3.3 V)	–	8	14	mA	Conditions are V_{DD} = 3.3 V, T_A = 25 °C, CPU = 3 MHz, SYSCLK doubler disabled, VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 0.367 kHz, analog power = off.
I_{SB}	Sleep [21] (mode) current with POR, LVD, sleep timer, and WDT.[22]	–	3	6.5	µA	Conditions are with internal slow speed oscillator, V_{DD} = 3.3 V, –40 °C ≤ T_A ≤ 55 °C, analog power = off.
I_{SBH}	Sleep (mode) current with POR, LVD, Sleep Timer, and WDT at high temperature.[22]	–	4	25	µA	Conditions are with internal slow speed oscillator, V_{DD} = 3.3 V, 55 °C < T_A ≤ 85 °C, analog power = off.

Notes
21. Errata: When the device is operating at 4.75 V to 5.25 V and the 3.3 V regulator is enabled, a short low pulse may be created on the DP signal line during device wake-up. The 15-20 µs low pulse of the DP line may be interpreted by the host computer as a deattach or the beginning of a wake-up. More details in "Errata" on page 66.
22. Standby current includes all functions (POR, LVD, WDT, Sleep Time) needed for reliable system operation. This should be compared with devices that have similar functions enabled.

11.3.4 DC Operational Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V and 3.3 V at 25 °C and are for design guidance only.

The operational amplifier is a component of both the analog continuous time PSoC blocks and the analog switched capacitor PSoC blocks. The guaranteed specifications are measured in the analog continuous time PSoC block.

Table 14. 5-V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input offset voltage (absolute value) Power = low, Opamp bias = high Power = medium, Opamp bias = high Power = high, Opamp bias = high	 – – –	 1.6 1.3 1.2	 10 8 7.5	 mV mV mV	
TCV_{OSOA}	Average input offset voltage drift	–	7.0	35.0	µV/°C	
I_{EBOA}	Input leakage current (Port 0 analog pins)	–	20	–	pA	Gross tested to 1 µA.
C_{INOA}	Input capacitance (Port 0 analog pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25 °C.
V_{CMOA}	Common mode voltage range Common mode voltage range (high power or high Opamp bias)	0.0 0.5	– –	V_{DD} V_{DD} – 0.5	V V	The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
G_{OLOA}	Open loop gain Power = low, Opamp bias = high Power = medium, Opamp bias = high Power = high, Opamp bias = high	 60 60 80	 – – –	 – – –	 dB dB dB	
$V_{OHIGHOA}$	High output voltage swing (internal signals) Power = low, Opamp bias = high Power = medium, Opamp bias = high Power = high, Opamp bias = high	 V_{DD} – 0.2 V_{DD} – 0.2 V_{DD} – 0.5	 – – –	 – – –	 V V V	
V_{OLOWOA}	Low output voltage swing (internal signals) Power = low, Opamp bias = high Power = medium, Opamp bias = high Power = high, Opamp bias = high	 – – –	 – – –	 0.2 0.2 0.5	 V V V	
I_{SOA}	Supply current (including associated AGND buffer) Power = low, Opamp bias = low Power = low, Opamp bias = high Power = medium, Opamp bias = low Power = medium, Opamp bias = high Power = high, Opamp bias = low Power = high, Opamp bias = high	 – – – – – –	 400 500 800 1200 2400 4600	 800 900 1000 1600 3200 6400	 µA µA µA µA µA µA	
$PSRR_{OA}$	Supply voltage rejection ratio	65	80	–	dB	$V_{SS} \le V_{IN} \le (V_{DD} – 2.25)$ or $(V_{DD} – 1.25\ V) \le V_{IN} \le V_{DD}$.

Table 19. 5-V DC Analog Reference Specifications *(continued)*

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b001	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.092	P2[4] + P2[6] – 0.011	P2[4] + P2[6] + 0.064	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.031	P2[4] – P2[6] + 0.007	P2[4] – P2[6] + 0.056	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.078	P2[4] + P2[6] – 0.008	P2[4] + P2[6] + 0.063	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.031	P2[4] – P2[6] + 0.004	P2[4] – P2[6] + 0.043	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.073	P2[4] + P2[6] – 0.006	P2[4] + P2[6] + 0.062	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.032	P2[4] – P2[6] + 0.003	P2[4] – P2[6] + 0.038	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.073	P2[4] + P2[6] – 0.006	P2[4] + P2[6] + 0.062	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.034	P2[4] – P2[6] + 0.002	P2[4] – P2[6] + 0.037	V
0b010	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.037	V_{DD} – 0.007	V_{DD}	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.036	V_{DD}/2 – 0.001	V_{DD}/2 + 0.036	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.005	V_{SS} + 0.029	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.034	V_{DD} – 0.006	V_{DD}	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.036	V_{DD}/2 – 0.001	V_{DD}/2 + 0.035	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.004	V_{SS} + 0.024	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.032	V_{DD} – 0.005	V_{DD}	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.036	V_{DD}/2 – 0.001	V_{DD}/2 + 0.035	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.003	V_{SS} + 0.022	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.031	V_{DD} – 0.005	V_{DD}	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.037	V_{DD}/2 – 0.001	V_{DD}/2 + 0.035	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.003	V_{SS} + 0.020	V

Note The bits PORLEV and VM in the following table refer to bits in the VLT_CR register. See the *PSoC Technical Reference Manual* for more information on the VLT_CR register.

Table 22. DC POR and LVD Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
	V_{DD} value for PPOR trip (positive ramp)					
V_{PPOR0R}	PORLEV[1:0] = 00b		2.91		V	
V_{PPOR1R}	PORLEV[1:0] = 01b	–	4.39	–	V	
V_{PPOR2R}	PORLEV[1:0] = 10b		4.55		V	
	V_{DD} value for PPOR trip (negative ramp)					
V_{PPOR0} [23]	PORLEV[1:0] = 00b		2.82		V	
V_{PPOR1} [23]	PORLEV[1:0] = 01b	–	4.39	–	V	
V_{PPOR2} [23]	PORLEV[1:0] = 10b		4.55		V	
	PPOR hysteresis					
V_{PH0}	PORLEV[1:0] = 00b	–	92	–	mV	
V_{PH1}	PORLEV[1:0] = 01b	–	0	–	mV	
V_{PH2}	PORLEV[1:0] = 10b	–	0	–	mV	
	V_{DD} value for LVD trip					
V_{LVD0}	VM[2:0] = 000b	2.86	2.92	2.98[24]	V	
V_{LVD1}	VM[2:0] = 001b	2.96	3.02	3.08	V	
V_{LVD2}	VM[2:0] = 010b	3.07	3.13	3.20	V	
V_{LVD3}	VM[2:0] = 011b	3.92	4.00	4.08	V	
V_{LVD4}	VM[2:0] = 100b	4.39	4.48	4.57	V	
V_{LVD5}	VM[2:0] = 101b	4.55	4.64	4.74[25]	V	
V_{LVD6}	VM[2:0] = 110b	4.63	4.73	4.82	V	
V_{LVD7}	VM[2:0] = 111b	4.72	4.81	4.91	V	

Notes
23. Errata: When V_{DD} of the device is pulled below ground just before power on, the first read from each 8K Flash page may be corrupted. This issue does not affect Flash page 0 because it is the selected page upon reset. More details in "Errata" on page 66.
24. Always greater than 50 mV above PPOR (PORLEV = 00) for falling supply.
25. Always greater than 50 mV above PPOR (PORLEV = 10) for falling supply.

11.3.10 DC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 23. DC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DDP}	V_{DD} for programming and erase	4.5	5	5.5	V	This specification applies to the functional requirements of external programmer tools
V_{DDLV}	Low V_{DD} for verify	3	3.1	3.2	V	This specification applies to the functional requirements of external programmer tools
V_{DDHV}	High V_{DD} for verify	5.1	5.2	5.3	V	This specification applies to the functional requirements of external programmer tools
$V_{DDIWRITE}$	Supply voltage for flash write operation	3		5.25	V	This specification applies to this device when it is executing internal flash writes
I_{DDP}	Supply current during programming or verify	–	15	30	mA	
V_{ILP}	Input low voltage during programming or verify	–	–	0.8	V	
V_{IHP}	Input high voltage during programming or verify	2.1	–	–	V	
I_{ILP}	Input current when applying V_{ILP} to P1[0] or P1[1] during programming or verify	–	–	0.2	mA	Driving internal pull-down resistor.
I_{IHP}	Input current when applying V_{IHP} to P1[0] or P1[1] during programming or verify	–	–	1.5	mA	Driving internal pull-down resistor.
V_{OLV}	Output low voltage during programming or verify	–	–	V_{SS} + 0.75	V	
V_{OHV}	Output high voltage during programming or verify	V_{DD} – 1.0	–	V_{DD}	V	
$Flash_{ENPB}$	Flash endurance (per block)[26]	50,000	–	–	–	Erase/write cycles per block.
$Flash_{ENT}$	Flash endurance (total)[27]	1,800,000	–	–	–	Erase/write cycles.
$Flash_{DR}$	Flash data retention	10	–	–	Years	

11.3.11 DC I²C Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 24. DC I²C Specifications[28]

Symbol	Description	Min	Typ	Max	Units	Notes
V_{ILI2C}	Input low level	–	–	0.3 × V_{DD}	V	3.0 V ≤ V_{DD} ≤ 3.6 V
		–	–	0.25 × V_{DD}	V	4.75 V ≤ V_{DD} ≤ 5.25 V
V_{IHI2C}	Input high level	0.7 × V_{DD}	–	–	V	3.0 V ≤ V_{DD} ≤ 5.25 V

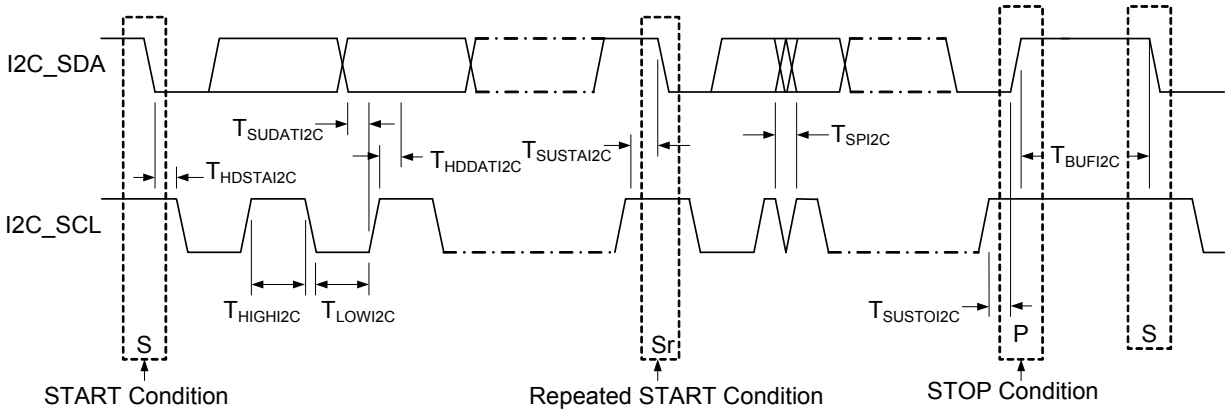
11.4.10 AC I²C Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 36. AC Characteristics of the I²C SDA and SCL Pins for V_{DD}

Symbol	Description	Standard Mode		Fast Mode		Units	Notes
		Min	Max	Min	Max		
F_{SCLI2C}	SCL clock frequency	0	100	0	400	kHz	
$t_{HDSTAI2C}$	Hold time (repeated) start condition. After this period, the first clock pulse is generated	4.0	–	0.6	–	µs	
t_{LOWI2C}	Low period of the SCL clock	4.7	–	1.3	–	µs	
$t_{HIGHI2C}$	High period of the SCL clock	4.0	–	0.6	–	µs	
$t_{SUSTAI2C}$	Setup time for a repeated start condition	4.7	–	0.6	–	µs	
$t_{HDDATI2C}$	Data hold time	0	–	0	–	µs	
$t_{SUDATI2C}$	Data setup time	250	–	100[35]	–	ns	
$t_{SUSTOI2C}$	Setup time for stop condition	4.0	–	0.6	–	µs	
t_{BUFI2C}	Bus free time between a stop and start condition	4.7	–	1.3	–	µs	
t_{SPI2C}	Pulse width of spikes suppressed by the input filter	–	–	0	50	ns	

Figure 15. Definition for Timing for Fast/Standard Mode on the I²C Bus



Note

35. A fast-mode I²C-bus device can be used in a standard-mode I²C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns it must meet. This automatically is the case if the device does not stretch the LOW period of the SCL signal. If the device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the Standard-Mode I²C-bus specification) before the SCL line is released.

11.5 Thermal Impedance

Table 37. Thermal Impedances per Package

Package	Typical θ_{JA} [36]
56-Pin QFN[37]	12.93 °C/W
68-Pin QFN[37]	13.05 °C/W
100-Ball VFBGA	65 °C/W
100-Pin TQFP	51 °C/W

11.6 Solder Reflow Peak Specifications

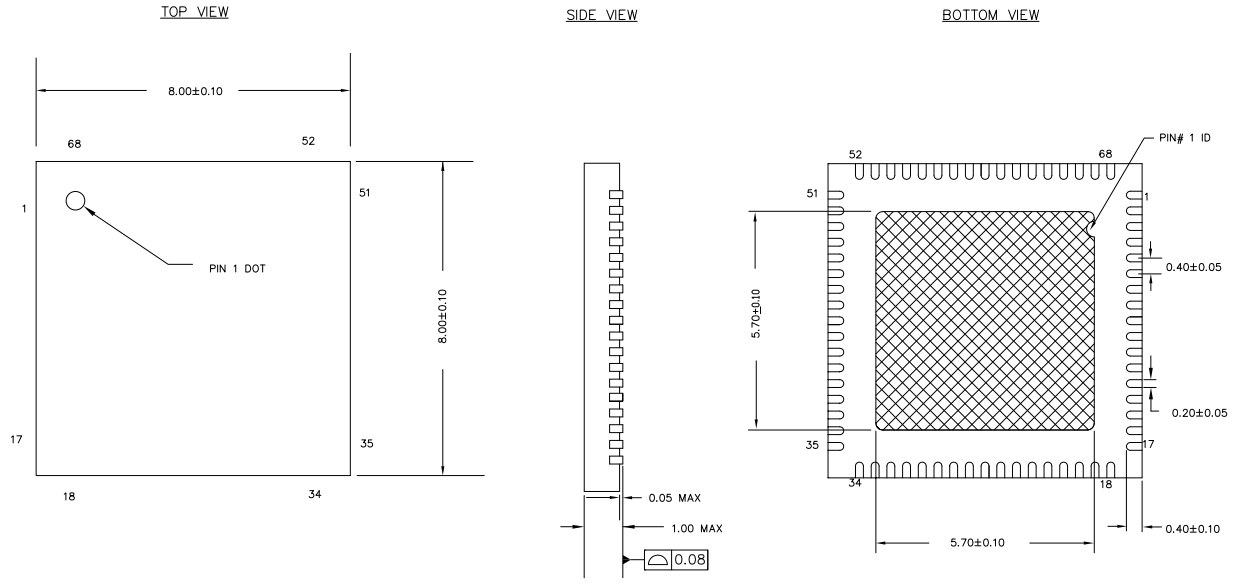
Table 38 shows the solder reflow temperature limits that must not be exceeded.

Table 38. Solder Reflow Specifications

Package	Maximum Peak Temperature (T_C)	Maximum Time above T_C – 5 °C
56-Pin QFN	260 °C	30 seconds
68-Pin QFN	260 °C	30 seconds
100-Ball VFBGA	260 °C	30 seconds
100-Pin TQFP	260 °C	30 seconds

Notes
36. $T_J = T_A + POWER \times \theta_{JA}$.
37. To achieve the thermal impedance specified for the QFN package, see the *Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages* available at http://www.amkor.com.

Figure 19. 68-pin QFN (8 × 8 × 1.0 mm) LT68 5.7 × 5.7 E-Pad (Sawn Type) Package Outline, 001-09618

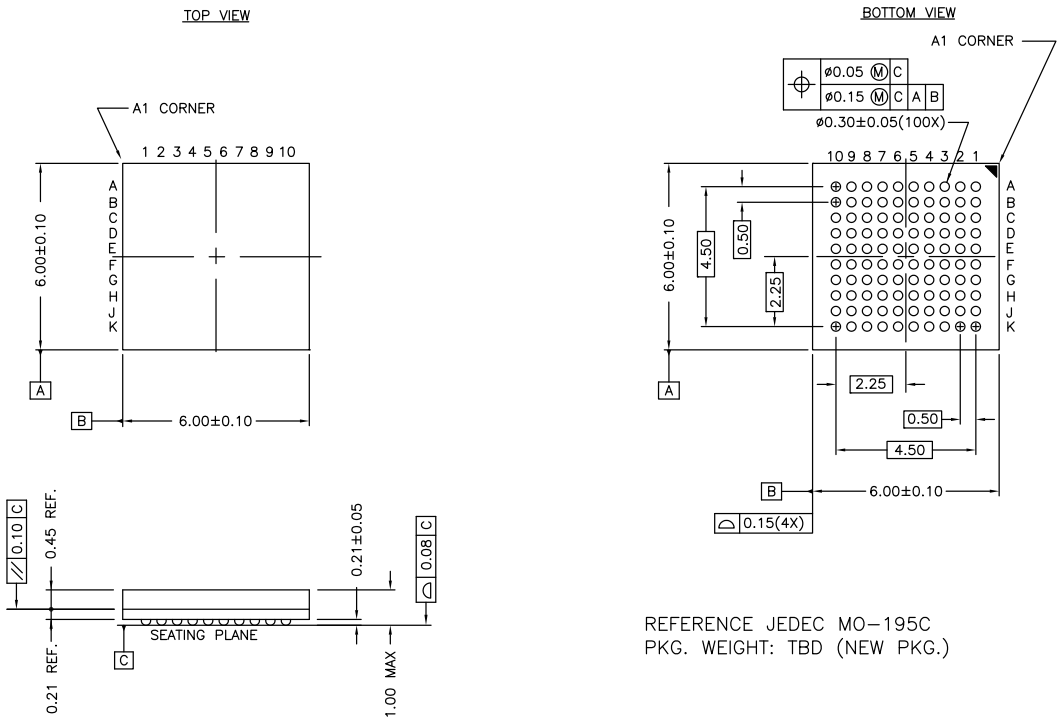


NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO−220
3. PACKAGE WEIGHT: 17 ± 2mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-09618 *E

Figure 20. 100-ball VFBGA (6 × 6 × 1.0 mm) BZ100 Package Outline, 51-85209



17. Glossary *(continued)*

external reset (XRES)	An active high signal that is driven into the PSoC device. It causes all operation of the CPU and blocks to stop and return to a pre-defined state.
flash	An electrically programmable and erasable, non-volatile technology that provides users with the programmability and data storage of EPROMs, plus in-system erasability. Non-volatile means that the data is retained when power is off.
Flash block	The smallest amount of Flash ROM space that may be programmed at one time and the smallest amount of Flash space that may be protected. A Flash block holds 64 bytes.
frequency	The number of cycles or events per unit of time, for a periodic function.
gain	The ratio of output current, voltage, or power to input current, voltage, or power, respectively. Gain is usually expressed in dB.
I^2C	A two-wire serial computer bus by Philips Semiconductors (now NXP Semiconductors). I2C is an Inter-Integrated Circuit. It is used to connect low-speed peripherals in an embedded system. The original system was created in the early 1980s as a battery control interface, but it was later used as a simple internal bus system for building control electronics. I2C uses only two bi-directional pins, clock and data, both running at +5V and pulled high with resistors. The bus operates at 100 kbits/second in standard mode and 400 kbits/second in fast mode.
ICE	The in-circuit emulator that allows users to test the project in a hardware environment, while viewing the debugging device activity in a software environment (PSoC Designer).
input/output (I/O)	A device that introduces data into or extracts data from a system.
interrupt	A suspension of a process, such as the execution of a computer program, caused by an event external to that process, and performed in such a way that the process can be resumed.
interrupt service routine (ISR)	A block of code that normal code execution is diverted to when the M8C receives a hardware interrupt. Many interrupt sources may each exist with its own priority and individual ISR code block. Each ISR code block ends with the RETI instruction, returning the device to the point in the program where it left normal program execution.
jitter	1. A misplacement of the timing of a transition from its ideal position. A typical form of corruption that occurs on serial data streams. 2. The abrupt and unwanted variations of one or more signal characteristics, such as the interval between successive pulses, the amplitude of successive cycles, or the frequency or phase of successive cycles.
low-voltage detect (LVD)	A circuit that senses V_{DD} and provides an interrupt to the system when V_{DD} falls lower than a selected threshold.
M8C	An 8-bit Harvard-architecture microprocessor. The microprocessor coordinates all activity inside a PSoC by interfacing to the Flash, SRAM, and register space.
master device	A device that controls the timing for data exchanges between two devices. Or when devices are cascaded in width, the master device is the one that controls the timing for data exchanges between the cascaded devices and an external interface. The controlled device is called the ***slave device.***
microcontroller	An integrated circuit chip that is designed primarily for control systems and products. In addition to a CPU, a microcontroller typically includes memory, timing circuits, and IO circuitry. The reason for this is to permit the realization of a controller with a minimal quantity of chips, thus achieving maximal possible miniaturization. This in turn, reduces the volume and the cost of the controller. The microcontroller is normally not used for general-purpose computation as is a microprocessor.
mixed-signal	The reference to a circuit containing both analog and digital techniques and components.

17. Glossary *(continued)*

modulator	A device that imposes a signal on a carrier.
noise	1. A disturbance that affects a signal and that may distort the information carried by the signal. 2. The random variations of one or more characteristics of any entity such as voltage, current, or data.
oscillator	A circuit that may be crystal controlled and is used to generate a clock frequency.
parity	A technique for testing transmitting data. Typically, a binary digit is added to the data to make the sum of all the digits of the binary data either always even (even parity) or always odd (odd parity).
phase-locked loop (PLL)	An electronic circuit that controls an ***oscillator*** so that it maintains a constant phase angle relative to a reference signal.
pinouts	The pin number assignment: the relation between the logical inputs and outputs of the PSoC device and their physical counterparts in the printed circuit board (PCB) package. Pinouts involve pin numbers as a link between schematic and PCB design (both being computer generated files) and may also involve pin names.
port	A group of pins, usually eight.
power on reset (POR)	A circuit that forces the PSoC device to reset when the voltage is lower than a pre-set level. This is one type of hardware reset.
PSoC®	Cypress Semiconductor's PSoC® is a registered trademark and Programmable System-on-Chip™ is a trademark of Cypress.
PSoC Designer™	The software for Cypress' Programmable System-on-Chip technology.
pulse width modulator (PWM)	An output in the form of duty cycle which varies as a function of the applied measurand
RAM	An acronym for random access memory. A data-storage device from which data can be read out and new data can be written in.
register	A storage device with a specific capacity, such as a bit or byte.
reset	A means of bringing a system back to a know state. See hardware reset and software reset.
ROM	An acronym for read only memory. A data-storage device from which data can be read out, but new data cannot be written in.
serial	1. Pertaining to a process in which all events occur one after the other. 2. Pertaining to the sequential or consecutive occurrence of two or more related activities in a single device or channel.
settling time	The time it takes for an output signal or value to stabilize after the input has changed from one value to another.
shift register	A memory storage device that sequentially shifts a word either left or right to output a stream of serial data.
slave device	A device that allows another device to control the timing for data exchanges between two devices. Or when devices are cascaded in width, the slave device is the one that allows another device to control the timing of data exchanges between the cascaded devices and an external interface. The controlling device is called the master device.

19. Document History Page *(continued)*

Document Title: CY8C24094/CY8C24794/CY8C24894/CY8C24994, PSoC® Programmable System-on-Chip™ Document Number: 38-12018				
*N	2708135	BRW	05/18/2009	Added Note in the Pin Information section on page 8. Removed reference to Hi-Tech Lite Compiler in the section Development Tools Selection on page 42.
*O	2718162	DPT	06/11/2009	Added 56-Pin QFN (Sawn) package diagram and updated ordering information
*P	2762161	RLRM	09/10/2009	Updated the following parameters: DC_{ILO}, F32K_U, F_{IMO6}, $T_{POWERUP}$, T_{ERASE_ALL}, $T_{PROGRAM\_HOT}$, and $T_{PROGRAM\_COLD}$. Added SR_{POWER_UP} parameter in AC specs table.
*Q	2768530	RLRM	09/24/09	Ordering Information table: Changed XRES Pin value for CY8C24894-24LTXI and CY8C24894-24LTXIT to 'Yes'.
*R	2817938	KRIS	11/30/09	Ordering Information: Updated CY8C24894-24LTXI and CY8C24894-24LTXIT parts as Sawn and updated the Digital I/O and Analog Pin values Added Contents page. Updated 68 QFN package diagram (51-85124)
*S	2846641	RLRM	1/12/10	Added package diagram 001-58740 and updated Development Tools section.
*T	2867363	ANUP	01/27/10	Modified Note 9 to remove voltage range 2.4 V to 3.0 V
*U	2901653	NJF	03/30/2010	Updated Cypress website links Added T_{XRST}, DC24M, $T_{BAKETEMP}$ and $T_{BAKETIME}$ parameters Removed reference to 2.4 V Removed sections 'Third Party Tools' 'Build a PSoC Emulator into your Board' Updated package diagrams Removed inactive parts from ordering information table.
*V	2938528	VMAD	05/28/2010	Updated content to match current style guide and datasheet template. No technical updates
*W	3028596	NJF	09/20/10	Added PSoC Device Characteristics table. Added DC I^2C Specifications table. Added F_{32K_U} max limit. Added Tjit_IMO specification, removed existing jitter specifications. Updated Analog reference tables. Updated Units of Measure, Acronyms, Glossary, and References sections. Updated solder reflow specifications. No specific changes were made to AC Digital Block Specifications table and I^2C Timing Diagram. They were updated for clearer understanding. Updated Figure 12 since the labelling for y-axis was incorrect. Template and styles update.
*X	3082244	NXZ	11/09/2010	Sunset review; no updates.
*Y	3111357	BTK / NJF / ARVM	12/15/10	Updated solder reflow specifications. Removed F_{IMO6} spec from AC chip-level specifications table. Removed the following pruned parts from the ordering information table and their references in the datasheet. 1) CY8C24794-24LFXI 2) CY8C24794-24LFXIT 3) CY8C24894-24LFXI 4) CY8C24894-24LFXIT
*Z	3126167	BTK / ANBA / PKS	01/03/11	Updated ordering information. Removed the package diagram spec 51-85214 since there are no MPNs in the ordering information table that corresponds with this package. Updated ordering code definitions for clearer understanding.
AA	3367463	BTK / GIR	09/22/11	Updated V_{REFHI} values for parameter '0b100' under Table 19 on page 31. Updated text under Table 19 on page 31. The text "Pin must be left floating" is included under Description of NC pin in Table 4 on page 12, Table 6 on page 14, Table 7 on page 16, and Table 8 on page 18. Updated Table 38 on page 51 to give more clarity.
AB	3404970	MATT	10/13/11	Removed prune device CY8C24994-24BVXI from Ordering Information.
AC	3461872	CSAI	12/13/2011	Sunset review; no content update

19. Document History Page *(continued)*

Document Title: CY8C24094/CY8C24794/CY8C24894/CY8C24994, PSoC® Programmable System-on-Chip™ Document Number: 38-12018				
AD	3503402	PMAD	01/20/2012	Updated V_{OH} and V_{OL} section in Table 12.
AE	3545509	PSAI	03/08/2012	Updated link to 'Technical reference Manual'.
AF	3862667	CSAI	01/09/2013	Updated Ordering Information (Updated part numbers). Updated Packaging Dimensions: spec 001-53450 – Changed revision from *B to *C. spec 001-09618 – Changed revision from *D to *E. spec 51-85048 – Changed revision from *E to *G.
AG	3979302	CSAI	04/23/2013	Updated Packaging Dimensions: spec 001-58740 – Changed revision from ** to *A. Added Errata.
AH	4074544	CSAI	07/23/2013	Added Errata Footnotes (Note 21, 23) Updated Electrical Specifications: Updated DC Electrical Characteristics: Updated DC Chip-Level Specifications: Added Note 21 and referred the same note in “Sleep Mode” in description of I_{SB} parameter in Table 11. Updated DC POR and LVD Specifications: Added Note 23 and referred the same note in V_{PPOR0}, V_{PPOR1}, V_{PPOR2} parameters in Table 22. Updated to new template.
AI	4596835	DIMA	12/15/2014	Updated Pin Information: Updated 56-Pin Part Pinout: Updated Table 2: Added Note 5 and referred the same note in description of pin 19 and pin 50. Updated 56-Pin Part Pinout (with XRES): Updated Table 3: Added Note 8 and referred the same note in description of pin 19 and pin 50. Updated 68-Pin Part Pinout: Updated Table 4: Added Note 10 and referred the same note in description of pin 7, pin 20 and pin 60. Updated 68-Pin Part Pinout (On-Chip Debug): Updated Table 5: Added Note 13 and referred the same note in description of pin 7, pin 20 and pin 60. Updated 100-Ball VFBGA Part Pinout: Updated Table 6: Added Note 15 and referred the same note in caption of Table 6. Updated 100-Ball VFBGA Part Pinout (On-Chip Debug): Updated Table 7: Added Note 17 and referred the same note in caption of Table 7. Updated 100-Pin Part Pinout (On-Chip Debug): Updated Table 8: Added Note 19 and referred the same note in caption of Table 8. Updated Packaging Dimensions: spec 001-12921 – Changed revision from *B to *C. spec 001-53450 – Changed revision from *C to *D. spec 51-85209 – Changed revision from *D to *E. spec 51-85048 – Changed revision from *G to *I. Completing Sunset Review.
AJ	4622083	SLAN	01/13/2015	Added More Information section.
AK	4684565	PSI	03/12/2015	Updated Packaging Dimensions: spec 001-58740 – Changed revision from *A to *B. Updated Errata.
AL	5699855	AESATP12	04/20/2017	Updated logo and copyright.

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Forums | WICED IOT Forums | Projects | Video | Blogs | Training | Components

Technical Support

cypress.com/support