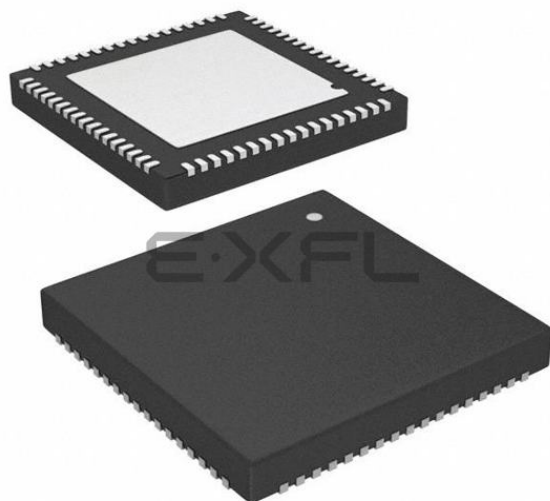




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Details

Product Status	Obsolete
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I ² C, SPI, UART/USART, USB
Peripherals	POR, PWM, WDT
Number of I/O	56
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	A/D 48x14b; D/A 2x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	68-VFQFN Exposed Pad
Supplier Device Package	68-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c24994-24ltxi

3. More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right PSoC device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the knowledge base article [KBA92181, Resources Available for CapSense® Controllers](#). Following is an abbreviated list for CapSense devices:

- Overview: [CapSense Portfolio](#), [CapSense Roadmap](#)
- Product Selectors: [CapSense](#), [CapSense Plus](#), [CapSense Express](#), [PSoC3 with CapSense](#), [PSoC5 with CapSense](#), [PSoC4](#). In addition, [PSoC Designer](#) offers a device selection tool at the time of creating a new project.
- Application notes: Cypress offers CapSense application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with CapSense are:
 - [AN64846](#): Getting Started With CapSense
 - [AN2397](#): CapSense® Data Viewing Tools
- Technical Reference Manual (TRM):
 - [CY8CPLC20](#), [CY8CLED16P01](#), [CY8C29x66](#), [CY8C27x43](#), [CY8C24x94](#), [CY8C24x23](#), [CY8C24x23A](#), [CY8C22x13](#), [CY8C21x34](#), [CY8C21x34B](#), [CY8C21x23](#), [CY7C64215](#), [CY7C603xx](#), [CY8CNP1xx](#), and [CYWUSB6953 PSoC® Programmable System-on-Chip TRM](#)

- Development Kits:
 - [CY3280-24x94 Universal CapSense Controller Board](#) features a predefined control circuitry and plug-in hardware to make prototyping and debugging easy. Programming and I2C-to-USB Bridge hardware are included for tuning and data acquisition.
 - [CY3280-BMM Matrix Button Module Kit](#) consists of eight CapSense sensors organized in a 4x4 matrix format to form 16 physical buttons and eight LEDs. This module connects to any CY3280 Universal CapSense Controller Board, including CY3280-20x66 Universal CapSense Controller.
 - [CY3280-BSM Simple Button Module Kit](#) consists of ten CapSense buttons and ten LEDs. This module connects to any CY3280 Universal CapSense Controller Board, including CY3280-20x66 Universal CapSense Controller.

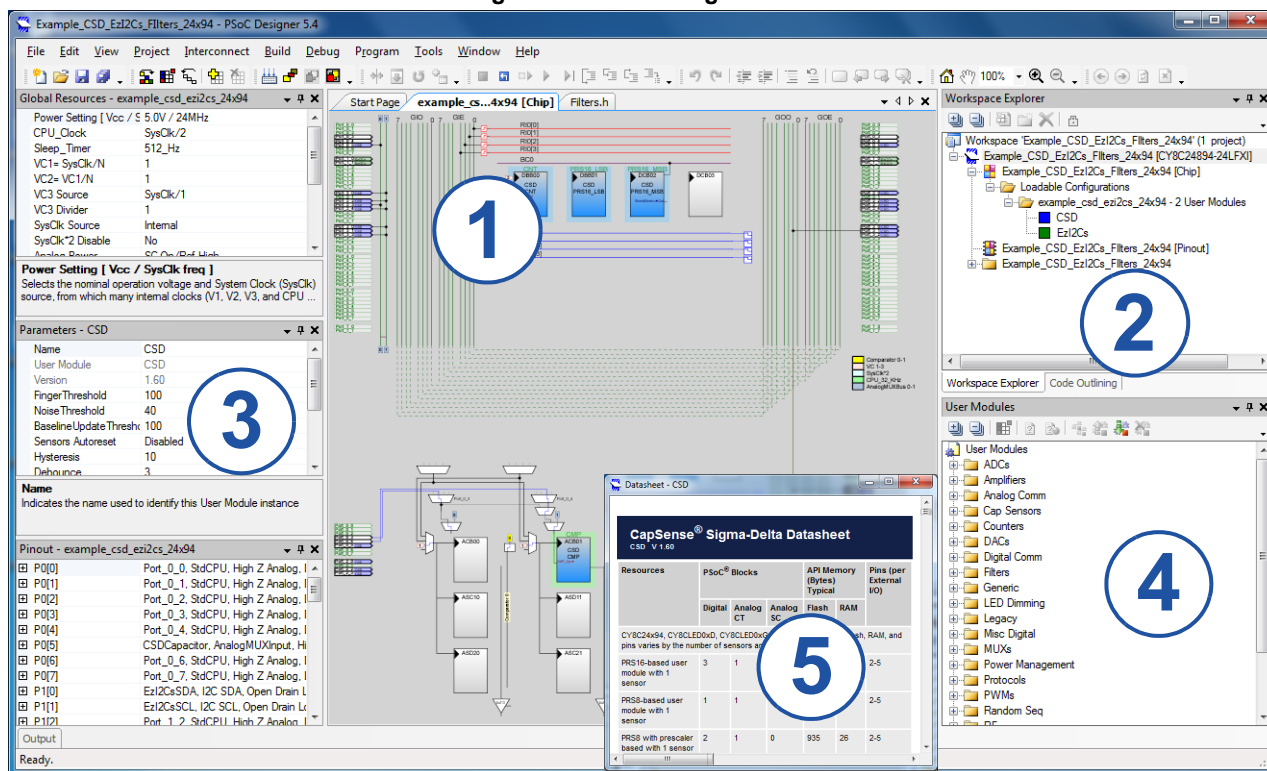
The [CY3217-MiniProg1](#) and [CY8CKIT-002 PSoC® MiniProg3](#) device provides an interface for flash programming.

3.1 PSoC Designer

[PSoC Designer](#) is a free Windows-based Integrated Design Environment (IDE). It enables concurrent hardware and firmware design of systems based on CapSense (see [Figure 1](#)). With PSoC Designer, you can:

1. Drag and drop User Modules to build your hardware system design in the main design workspace
2. Codesign your application firmware with the PSoC hardware, using the PSoC Designer IDE C compiler
3. Configure User Module
4. Explore the library of user modules
5. Review user module datasheets

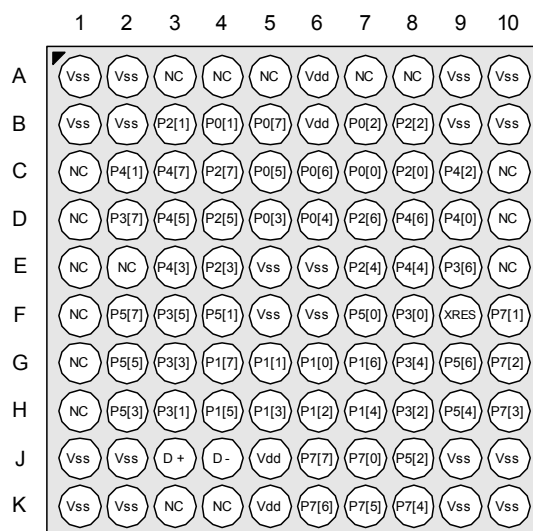
Figure 1. PSoC Designer Features



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Figure 8. CY8C24094 OCD (Not for Production)


BGA (Top View)

Notes

 15. All V_{SS} pins should be brought out to one common GND plane.

 16. These are the ISSP pins, which are not High Z at POR. See the [PSoC Technical Reference Manual](#) for details.

9.6 100-Ball VFBGA Part Pinout (On-Chip Debug)

The following 100-pin VFBGA part table and drawing is for the CY8C24094 OCD PSoC device.

Note This part is only used for in-circuit debugging. It is NOT available for production.

Table 7. 100-Ball Part Pinout (VFBGA^[17])

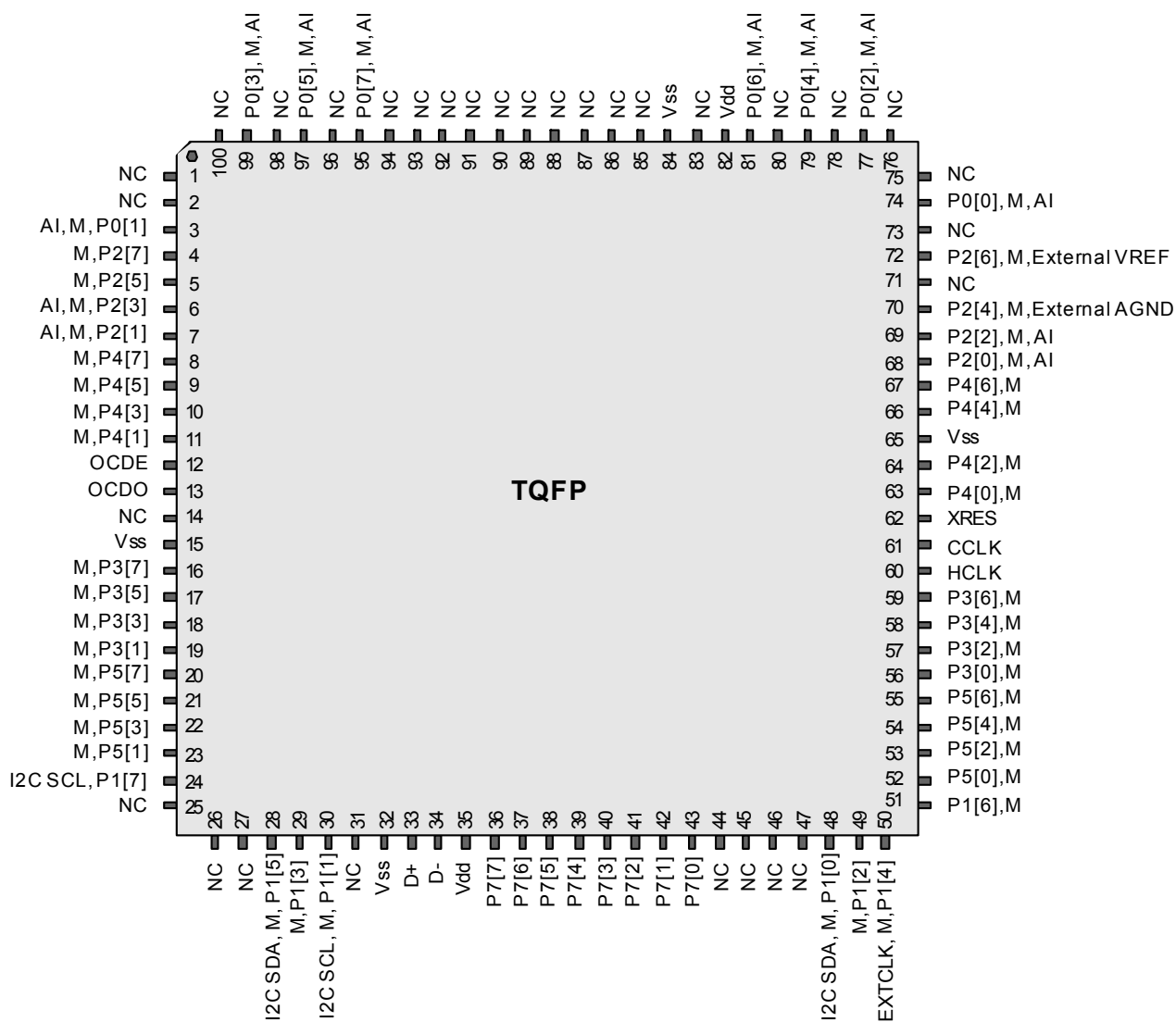
Pin No.	Digital	Analog	Name	Description	Pin No.	Digital	Analog	Name	Description
A1	Power		V _{SS}	Ground connection	F1			OCDE	OCD even data I/O
A2	Power		V _{SS}	Ground connection	F2	I/O	M	P5[7]	
A3			NC	No connection. Pin must be left floating	F3	I/O	M	P3[5]	
A4			NC	No connection. Pin must be left floating	F4	I/O	M	P5[1]	
A5			NC	No connection. Pin must be left floating.	F5	Power		V _{SS}	Ground connection
A6	Power		V _{DD}	Supply voltage.	F6	Power		V _{SS}	Ground connection
A7			NC	No connection. Pin must be left floating.	F7	I/O	M	P5[0]	
A8			NC	No connection. Pin must be left floating.	F8	I/O	M	P3[0]	
A9	Power		V _{SS}	Ground connection	F9			XRES	Active high pin reset with internal pull-down
A10	Power		V _{SS}	Ground connection	F10	I/O		P7[1]	
B1	Power		V _{SS}	Ground connection	G1			OCDO	OCD odd data output
B2	Power		V _{SS}	Ground connection	G2	I/O	M	P5[5]	
B3	I/O	I, M	P2[1]	Direct switched capacitor block input	G3	I/O	M	P3[3]	
B4	I/O	I, M	P0[1]	Analog column mux input	G4	I/O	M	P1[7]	I ² C SCL
B5	I/O	I, M	P0[7]	Analog column mux input	G5	I/O	M	P1[1]	I ² C SCL, ISSP SCLK ^[18]
B6	Power		V _{DD}	Supply voltage	G6	I/O	M	P1[0]	I ² C SDA, ISSP SDATA ^[18]
B7	I/O	I, M	P0[2]	Analog column mux input	G7	I/O	M	P1[6]	
B8	I/O	I, M	P2[2]	Direct switched capacitor block input	G8	I/O	M	P3[4]	
B9	Power		V _{SS}	Ground connection	G9	I/O	M	P5[6]	
B10	Power		V _{SS}	Ground connection	G10	I/O		P7[2]	
C1			NC	No connection. Pin must be left floating	H1			NC	No connection. Pin must be left floating
C2	I/O	M	P4[1]		H2	I/O	M	P5[3]	
C3	I/O	M	P4[7]		H3	I/O	M	P3[1]	
C4	I/O	M	P2[7]		H4	I/O	M	P1[5]	I ² C SDA
C5	I/O	I/O, M	P0[5]	Analog column mux input and column output	H5	I/O	M	P1[3]	
C6	I/O	I, M	P0[6]	Analog column mux input	H6	I/O	M	P1[2]	
C7	I/O	I, M	P0[0]	Analog column mux input	H7	I/O	M	P1[4]	Optional EXTCLK
C8	I/O	I, M	P2[0]	Direct switched capacitor block input	H8	I/O	M	P3[2]	
C9	I/O	M	P4[2]		H9	I/O	M	P5[4]	
C10			NC	No connection. Pin must be left floating	H10	I/O		P7[3]	
D1			NC	No connection. Pin must be left floating	J1	Power		V _{SS}	Ground connection
D2	I/O	M	P3[7]		J2	Power		V _{SS}	Ground connection
D3	I/O	M	P4[5]		J3	USB		D+	
D4	I/O	M	P2[5]		J4	USB		D-	
D5	I/O	I/O, M	P0[3]	Analog column mux input and column output	J5	Power		V _{DD}	Supply voltage
D6	I/O	I, M	P0[4]	Analog column mux input	J6	I/O		P7[7]	
D7	I/O	M	P2[6]	External VREF input	J7	I/O		P7[0]	
D8	I/O	M	P4[6]		J8	I/O	M	P5[2]	
D9	I/O	M	P4[0]		J9	Power		V _{SS}	Ground connection
D10			CCLK	OCD CPU clock output	J10	Power		V _{SS}	Ground connection
E1			NC	No connection. Pin must be left floating	K1	Power		V _{SS}	Ground connection
E2			NC	No connection. Pin must be left floating	K2	Power		V _{SS}	Ground connection
E3	I/O	M	P4[3]		K3			NC	No connection. Pin must be left floating
E4	I/O	I, M	P2[3]	Direct switched capacitor block input	K4			NC	No connection. Pin must be left floating
E5	Power		V _{SS}	Ground connection	K5	Power		V _{DD}	Supply voltage
E6	Power		V _{SS}	Ground connection	K6	I/O		P7[6]	
E7	I/O	M	P2[4]	External AGND input	K7	I/O		P7[5]	
E8	I/O	M	P4[4]		K8	I/O		P7[4]	
E9	I/O	M	P3[6]		K9	Power		V _{SS}	Ground connection
E10			HCLK	OCD high speed clock output	K10	Power		V _{SS}	Ground connection

LEGEND A = Analog, I = Input, O = Output, M = Analog Mux Input, NC = No connection. Pin must be left floating, OCD = On-Chip Debugger.

Notes

17. All V_{SS} pins should be brought out to one common GND plane.

18. These are the ISSP pins, which are not High Z at POR. See the [PSoC Technical Reference Manual](#) for details.

Figure 10. CY8C24094 OCD (Not for Production)


10. Register Reference

This section lists the registers of the CY8C24x94 PSoC device family. For detailed register information, see the [PSoC Technical Reference Manual](#).

10.1 Register Conventions

The register conventions specific to this section are listed in the following table.

Convention	Description
R	Read register or bit(s)
W	Write register or bit(s)
L	Logical register or bit(s)
C	Clearable register or bit(s)
#	Access is bit specific

10.2 Register Mapping Tables

The PSoC device has a total register address space of 512 bytes. The register space is referred to as I/O space and is divided into two banks, Bank 0 and Bank 1. The XO1 bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XO1 bit is set to 1, the user is in Bank 1.

Note In the following register mapping tables, blank fields are Reserved and should not be accessed.

10.4 Register Map Bank 1 Table: Configuration Space

Name	Addr (1, Hex)	Access	Name	Addr (1, Hex)	Access	Name	Addr (1, Hex)	Access	Name	Addr (1, Hex)	Access
PRT0DM0	00	RW	PMA0_WA	40	RW	ASC10CR0	80	RW	USB/O_CR2	C0	RW
PRT0DM1	01	RW	PMA1_WA	41	RW	ASC10CR1	81	RW	USB_CR1	C1	#
PRT0IC0	02	RW	PMA2_WA	42	RW	ASC10CR2	82	RW			
PRT0IC1	03	RW	PMA3_WA	43	RW	ASC10CR3	83	RW			
PRT1DM0	04	RW	PMA4_WA	44	RW	ASD11CR0	84	RW	EP1_CR0	C4	#
PRT1DM1	05	RW	PMA5_WA	45	RW	ASD11CR1	85	RW	EP2_CR0	C5	#
PRT1IC0	06	RW	PMA6_WA	46	RW	ASD11CR2	86	RW	EP3_CR0	C6	#
PRT1IC1	07	RW	PMA7_WA	47	RW	ASD11CR3	87	RW	EP4_CR0	C7	#
PRT2DM0	08	RW		48			88			C8	
PRT2DM1	09	RW		49			89			C9	
PRT2IC0	0A	RW		4A			8A			CA	
PRT2IC1	0B	RW		4B			8B			CB	
PRT3DM0	0C	RW		4C			8C			CC	
PRT3DM1	0D	RW		4D			8D			CD	
PRT3IC0	0E	RW		4E			8E			CE	
PRT3IC1	0F	RW		4F			8F			CF	
PRT4DM0	10	RW	PMA0_RA	50	RW		90		GDI_O_IN	D0	RW
PRT4DM1	11	RW	PMA1_RA	51	RW	ASD20CR1	91	RW	GDI_E_IN	D1	RW
PRT4IC0	12	RW	PMA2_RA	52	RW	ASD20CR2	92	RW	GDI_O_OU	D2	RW
PRT4IC1	13	RW	PMA3_RA	53	RW	ASD20CR3	93	RW	GDI_E_OU	D3	RW
PRT5DM0	14	RW	PMA4_RA	54	RW	ASC21CR0	94	RW		D4	
PRT5DM1	15	RW	PMA5_RA	55	RW	ASC21CR1	95	RW		D5	
PRT5IC0	16	RW	PMA6_RA	56	RW	ASC21CR2	96	RW		D6	
PRT5IC1	17	RW	PMA7_RA	57	RW	ASC21CR3	97	RW		D7	
	18			58			98		MUX_CR0	D8	RW
	19			59			99		MUX_CR1	D9	RW
	1A			5A			9A		MUX_CR2	DA	RW
	1B			5B			9B		MUX_CR3	DB	RW
PRT7DM0	1C	RW		5C			9C			DC	
PRT7DM1	1D	RW		5D			9D		OSC_GO_EN	DD	RW
PRT7IC0	1E	RW		5E			9E		OSC_CR4	DE	RW
PRT7IC1	1F	RW		5F			9F		OSC_CR3	DF	RW
DBB00FN	20	RW	CLK_CR0	60	RW		A0		OSC_CR0	E0	RW
DBB00IN	21	RW	CLK_CR1	61	RW		A1		OSC_CR1	E1	RW
DBB00OU	22	RW	ABF_CR0	62	RW		A2		OSC_CR2	E2	RW
	23		AMD_CR0	63	RW		A3		VLT_CR	E3	RW
DBB01FN	24	RW	CMP_GO_EN	64	RW		A4		VLT_CMP	E4	R
DBB01IN	25	RW		65			A5			E5	
DBB01OU	26	RW	AMD_CR1	66	RW		A6			E6	
	27		ALT_CR0	67	RW		A7			E7	
DCB02FN	28	RW		68			A8		IMO_TR	E8	W
DCB02IN	29	RW		69			A9		ILO_TR	E9	W
DCB02OU	2A	RW		6A			AA		BDG_TR	EA	RW
	2B			6B			AB		ECO_TR	EB	W
DCB03FN	2C	RW	TMP_DR0	6C	RW		AC		MUX_CR4	EC	RW
DCB03IN	2D	RW	TMP_DR1	6D	RW		AD		MUX_CR5	ED	RW
DCB03OU	2E	RW	TMP_DR2	6E	RW		AE			EE	
	2F		TMP_DR3	6F	RW		AF			EF	
	30		ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
	31		ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
	32		ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
	34		ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
	35		ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
	36		ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
	37		ACB01CR2	77	RW		B7		CPU_F	F7	RL
	38			78			B8			F8	
	39			79			B9			F9	
	3A			7A			BA			FA	
	3B			7B			BB			FB	
	3C			7C			BC			FC	
	3D			7D			BD		DAC_CR	FD	RW
	3E			7E			BE		CPU_SCR1	FE	#
	3F			7F			BF		CPU_SCR0	FF	#

Blank fields are reserved and should not be accessed.

Access is bit specific.

11.3.3 DC Full Speed USB Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-10^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-10^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters are measured at 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 13. DC Full Speed (12 Mbps) USB Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
USB Interface						
V_{DI}	Differential input sensitivity	0.2	–	–	V	$ (D+) - (D-) $
V_{CM}	Differential input common mode range	0.8	–	2.5	V	
V_{SE}	Single ended receiver threshold	0.8	–	2.0	V	
C_{IN}	Transceiver capacitance	–	–	20	pF	
$I_{I/O}$	High Z state data line leakage	–10	–	10	μA	$0\text{ V} < V_{IN} < 3.3\text{ V}$.
R_{EXT}	External USB series resistor	23	–	25	Ω	In series with each USB pin.
V_{UOH}	Static output high, driven	2.8	–	3.6	V	15 k Ω $\pm$ 5% to ground. Internal pull-up enabled.
V_{UOHI}	Static output high, idle	2.7	–	3.6	V	15 k Ω $\pm$ 5% to ground. Internal pull-up enabled.
V_{UOL}	Static output low	–	–	0.3	V	15 k Ω $\pm$ 5% to ground. Internal pull-up enabled.
Z_O	USB driver output impedance	28	–	44	Ω	Including R_{EXT} resistor.
V_{CRS}	D+/D– crossover voltage	1.3	–	2.0	V	

Table 18. 3.3-V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
C_L	Load Capacitance	–	–	200	pF	This specification applies to the external circuit that is being driven by the analog output buffer.
V_{OSOB}	Input offset voltage (absolute value)	–	3	12	mV	
TCV_{OSOB}	Average input offset voltage drift	–	+6	–	$\mu V/^\circ C$	
V_{CMOB}	Common mode input voltage range	0.5	–	$V_{DD} - 1.0$	V	
R_{OUTOB}	Output resistance Power = low Power = high	– –	1 1	– –	W W	
$V_{OHIGHOB}$	High output voltage swing (Load = 1 K ohms to $V_{DD}/2$) Power = low Power = high	$0.5 \times V_{DD} + 1.0$ $0.5 \times V_{DD} + 1.0$	– –	– –	V V	
V_{LOWOB}	Low output voltage swing (Load = 1 K ohms to $V_{DD}/2$) Power = low Power = high	– –	– –	$0.5 \times V_{DD} - 1.0$ $0.5 \times V_{DD} - 1.0$	V V	
I_{SOB}	Supply current including opamp bias cell (No load) Power = low Power = high	– –	0.8 2.0	2.0 4.3	mA mA	
$PSRR_{OB}$	Supply voltage rejection ratio	34	64	–	dB	$(0.5 \times V_{DD} - 1.0) \leq V_{OUT} \leq (0.5 \times V_{DD} + 0.9)$.

Table 19. 5-V DC Analog Reference Specifications (continued)

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b011	RefPower = high Opamp bias = high	V _{REFHI}	Ref High	3 × Bandgap	3.760	3.884	4.006	V
		V _{AGND}	AGND	2 × Bandgap	2.522	2.593	2.669	V
		V _{REFLO}	Ref Low	Bandgap	1.252	1.299	1.342	V
	RefPower = high Opamp bias = low	V _{REFHI}	Ref High	3 × Bandgap	3.766	3.887	4.010	V
		V _{AGND}	AGND	2 × Bandgap	2.523	2.594	2.670	V
		V _{REFLO}	Ref Low	Bandgap	1.252	1.297	1.342	V
	RefPower = medium Opamp bias = high	V _{REFHI}	Ref High	3 × Bandgap	3.769	3.888	4.013	V
		V _{AGND}	AGND	2 × Bandgap	2.523	2.594	2.671	V
		V _{REFLO}	Ref Low	Bandgap	1.251	1.296	1.343	V
0b100	RefPower = high Opamp bias = high	V _{REFHI}	Ref High	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.483 + P2[6]	2.582 + P2[6]	2.674 + P2[6]	V
		V _{AGND}	AGND	2 × Bandgap	2.522	2.593	2.669	V
		V _{REFLO}	Ref Low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.524 – P2[6]	2.600 – P2[6]	2.676 – P2[6]	V
	RefPower = high Opamp bias = low	V _{REFHI}	Ref High	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.490 + P2[6]	2.586 + P2[6]	2.679 + P2[6]	V
		V _{AGND}	AGND	2 × Bandgap	2.523	2.594	2.669	V
		V _{REFLO}	Ref Low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.523 – P2[6]	2.598 – P2[6]	2.675 – P2[6]	V
	RefPower = medium Opamp bias = high	V _{REFHI}	Ref High	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.493 + P2[6]	2.588 + P2[6]	2.682 + P2[6]	V
		V _{AGND}	AGND	2 × Bandgap	2.523	2.594	2.670	V
		V _{REFLO}	Ref Low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.523 – P2[6]	2.597 – P2[6]	2.675 – P2[6]	V
	RefPower = medium Opamp bias = low	V _{REFHI}	Ref High	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.494 + P2[6]	2.589 + P2[6]	2.685 + P2[6]	V
		V _{AGND}	AGND	2 × Bandgap	2.523	2.595	2.671	V
		V _{REFLO}	Ref Low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.522 – P2[6]	2.596 – P2[6]	2.676 – P2[6]	V

Table 19. 5-V DC Analog Reference Specifications (continued)

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b101	RefPower = high Opamp bias = high	V _{REFHI}	Ref High	P2[4] + Bandgap (P2[4] = V _{DD} /2)	P2[4] + 1.218	P2[4] + 1.291	P2[4] + 1.354	V
		V _{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V _{REFLO}	Ref Low	P2[4] – Bandgap (P2[4] = V _{DD} /2)	P2[4] – 1.335	P2[4] – 1.294	P2[4] – 1.237	V
	RefPower = high Opamp bias = low	V _{REFHI}	Ref High	P2[4] + Bandgap (P2[4] = V _{DD} /2)	P2[4] + 1.221	P2[4] + 1.293	P2[4] + 1.358	V
		V _{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V _{REFLO}	Ref Low	P2[4] – Bandgap (P2[4] = V _{DD} /2)	P2[4] – 1.337	P2[4] – 1.297	P2[4] – 1.243	V
	RefPower = medium Opamp bias = high	V _{REFHI}	Ref High	P2[4] + Bandgap (P2[4] = V _{DD} /2)	P2[4] + 1.222	P2[4] + 1.294	P2[4] + 1.360	V
		V _{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V _{REFLO}	Ref Low	P2[4] – Bandgap (P2[4] = V _{DD} /2)	P2[4] – 1.338	P2[4] – 1.298	P2[4] – 1.245	V
	RefPower = medium Opamp bias = low	V _{REFHI}	Ref High	P2[4] + Bandgap (P2[4] = V _{DD} /2)	P2[4] + 1.221	P2[4] + 1.294	P2[4] + 1.362	V
		V _{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V _{REFLO}	Ref Low	P2[4] – Bandgap (P2[4] = V _{DD} /2)	P2[4] – 1.340	P2[4] – 1.298	P2[4] – 1.245	V
0b110	RefPower = high Opamp bias = high	V _{REFHI}	Ref High	2 × Bandgap	2.513	2.593	2.672	V
		V _{AGND}	AGND	Bandgap	1.264	1.302	1.340	V
		V _{REFLO}	Ref Low	V _{SS}	V _{SS}	V _{SS} + 0.008	V _{SS} + 0.038	V
	RefPower = high Opamp bias = low	V _{REFHI}	Ref High	2 × Bandgap	2.514	2.593	2.674	V
		V _{AGND}	AGND	Bandgap	1.264	1.301	1.340	V
		V _{REFLO}	Ref Low	V _{SS}	V _{SS}	V _{SS} + 0.005	V _{SS} + 0.028	V
	RefPower = medium Opamp bias = high	V _{REFHI}	Ref High	2 × Bandgap	2.514	2.593	2.676	V
		V _{AGND}	AGND	Bandgap	1.264	1.301	1.340	V
		V _{REFLO}	Ref Low	V _{SS}	V _{SS}	V _{SS} + 0.004	V _{SS} + 0.024	V
	RefPower = medium Opamp bias = low	V _{REFHI}	Ref High	2 × Bandgap	2.514	2.593	2.677	V
		V _{AGND}	AGND	Bandgap	1.264	1.300	1.340	V
		V _{REFLO}	Ref Low	V _{SS}	V _{SS}	V _{SS} + 0.003	V _{SS} + 0.021	V

Table 20. 3.3-V DC Analog Reference Specifications (continued)

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Unit s
0b010	RefPower = high Opamp bias = high	V _{REFHI}	Ref High	V _{DD}	V _{DD} – 0.119	V _{DD} – 0.005	V _{DD}	V
		V _{AGND}	AGND	V _{DD} /2	V _{DD} /2 – 0.028	V _{DD} /2	V _{DD} /2 + 0.029	V
		V _{REFLO}	Ref Low	V _{SS}	V _{SS}	V _{SS} + 0.004	V _{SS} + 0.022	V
	RefPower = high Opamp bias = low	V _{REFHI}	Ref High	V _{DD}	V _{DD} – 0.131	V _{DD} – 0.004	V _{DD}	V
		V _{AGND}	AGND	V _{DD} /2	V _{DD} /2 – 0.028	V _{DD} /2	V _{DD} /2 + 0.028	V
		V _{REFLO}	Ref Low	V _{SS}	V _{SS}	V _{SS} + 0.003	V _{SS} + 0.021	V
	RefPower = medium Opamp bias = high	V _{REFHI}	Ref High	V _{DD}	V _{DD} – 0.111	V _{DD} – 0.003	V _{DD}	V
		V _{AGND}	AGND	V _{DD} /2	V _{DD} /2 – 0.029	V _{DD} /2	V _{DD} /2 + 0.028	V
		V _{REFLO}	Ref Low	V _{SS}	V _{SS}	V _{SS} + 0.002	V _{SS} + 0.017	V
	RefPower = medium Opamp bias = low	V _{REFHI}	Ref High	V _{DD}	V _{DD} – 0.128	V _{DD} – 0.003	V _{DD}	V
		V _{AGND}	AGND	V _{DD} /2	V _{DD} /2 – 0.029	V _{DD} /2	V _{DD} /2 + 0.029	V
		V _{REFLO}	Ref Low	V _{SS}	V _{SS}	V _{SS} + 0.002	V _{SS} + 0.019	V
0b011	All power settings. Not allowed for 3.3 V.	–	–	–	–	–	–	–
0b100	All power settings. Not allowed for 3.3 V.	–	–	–	–	–	–	–
0b101	RefPower = high Opamp bias = high	V _{REFHI}	Ref High	P2[4] + Bandgap (P2[4] = V _{DD} /2)	P2[4] + 1.214	P2[4] + 1.291	P2[4] + 1.359	V
		V _{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V _{REFLO}	Ref Low	P2[4] – Bandgap (P2[4] = V _{DD} /2)	P2[4] – 1.335	P2[4] – 1.292	P2[4] – 1.200	V
	RefPower = high Opamp bias = low	V _{REFHI}	Ref High	P2[4] + Bandgap (P2[4] = V _{DD} /2)	P2[4] + 1.219	P2[4] + 1.293	P2[4] + 1.357	V
		V _{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V _{REFLO}	Ref Low	P2[4] – Bandgap (P2[4] = V _{DD} /2)	P2[4] – 1.335	P2[4] – 1.295	P2[4] – 1.243	V
	RefPower = medium Opamp bias = high	V _{REFHI}	Ref High	P2[4] + Bandgap (P2[4] = V _{DD} /2)	P2[4] + 1.222	P2[4] + 1.294	P2[4] + 1.356	V
		V _{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V _{REFLO}	Ref Low	P2[4] – Bandgap (P2[4] = V _{DD} /2)	P2[4] – 1.337	P2[4] – 1.296	P2[4] – 1.244	V
	RefPower = medium Opamp bias = low	V _{REFHI}	Ref High	P2[4] + Bandgap (P2[4] = V _{DD} /2)	P2[4] + 1.224	P2[4] + 1.295	P2[4] + 1.355	V
		V _{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V _{REFLO}	Ref Low	P2[4] – Bandgap (P2[4] = V _{DD} /2)	P2[4] – 1.339	P2[4] – 1.297	P2[4] – 1.244	V

Note The bits PORLEV and VM in the following table refer to bits in the VLT_CR register. See the [PSoC Technical Reference Manual](#) for more information on the VLT_CR register.

Table 22. DC POR and LVD Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V _{PPOR0R} V _{PPOR1R} V _{PPOR2R}	V _{DD} value for PPOR trip (positive ramp) PORLEV[1:0] = 00b PORLEV[1:0] = 01b PORLEV[1:0] = 10b	—	2.91 4.39 4.55	—	V V V	
V _{PPOR0} ^[23] V _{PPOR1} ^[23] V _{PPOR2} ^[23]	V _{DD} value for PPOR trip (negative ramp) PORLEV[1:0] = 00b PORLEV[1:0] = 01b PORLEV[1:0] = 10b	—	2.82 4.39 4.55	—	V V V	
V _{PH0} V _{PH1} V _{PH2}	PPOR hysteresis PORLEV[1:0] = 00b PORLEV[1:0] = 01b PORLEV[1:0] = 10b	— — —	92 0 0	— — —	mV mV mV	
V _{LVD0} V _{LVD1} V _{LVD2} V _{LVD3} V _{LVD4} V _{LVD5} V _{LVD6} V _{LVD7}	V _{DD} value for LVD trip VM[2:0] = 000b VM[2:0] = 001b VM[2:0] = 010b VM[2:0] = 011b VM[2:0] = 100b VM[2:0] = 101b VM[2:0] = 110b VM[2:0] = 111b	2.86 2.96 3.07 3.92 4.39 4.55 4.63 4.72	2.92 3.02 3.13 4.00 4.48 4.64 4.73 4.81	2.98 ^[24] 3.08 3.20 4.08 4.57 4.74 ^[25] 4.82 4.91	V V V V V V V V	

Notes

23. Errata: When V_{DD} of the device is pulled below ground just before power on, the first read from each 8K Flash page may be corrupted. This issue does not affect Flash page 0 because it is the selected page upon reset. More details in ["Errata"](#) on page 66.

24. Always greater than 50 mV above PPOR (PORLEV = 00) for falling supply.

25. Always greater than 50 mV above PPOR (PORLEV = 10) for falling supply.

11.3.10 DC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters are measured at 5 V and 3.3 V at 25°C and are for design guidance only.

Table 23. DC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DDP}	V_{DD} for programming and erase	4.5	5	5.5	V	This specification applies to the functional requirements of external programmer tools
$V_{DDL V}$	Low V_{DD} for verify	3	3.1	3.2	V	This specification applies to the functional requirements of external programmer tools
V_{DDHV}	High V_{DD} for verify	5.1	5.2	5.3	V	This specification applies to the functional requirements of external programmer tools
$V_{DDIWRITE}$	Supply voltage for flash write operation	3		5.25	V	This specification applies to this device when it is executing internal flash writes
I_{DDP}	Supply current during programming or verify	–	15	30	mA	
V_{ILP}	Input low voltage during programming or verify	–	–	0.8	V	
V_{IHP}	Input high voltage during programming or verify	2.1	–	–	V	
I_{ILP}	Input current when applying V_{ILP} to P1[0] or P1[1] during programming or verify	–	–	0.2	mA	Driving internal pull-down resistor.
I_{IHP}	Input current when applying V_{IHP} to P1[0] or P1[1] during programming or verify	–	–	1.5	mA	Driving internal pull-down resistor.
V_{OLV}	Output low voltage during programming or verify	–	–	$V_{SS} + 0.75$	V	
V_{OHV}	Output high voltage during programming or verify	$V_{DD} - 1.0$	–	V_{DD}	V	
Flash _{ENPB}	Flash endurance (per block) ^[26]	50,000	–	–	–	Erase/write cycles per block.
Flash _{ENT}	Flash endurance (total) ^[27]	1,800,000	–	–	–	Erase/write cycles.
Flash _{DR}	Flash data retention	10	–	–	Years	

11.3.11 DC I²C Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters are measured at 5 V and 3.3 V at 25°C and are for design guidance only.

Table 24. DC I²C Specifications^[28]

Symbol	Description	Min	Typ	Max	Units	Notes
V_{IL2C}	Input low level	–	–	$0.3 \times V_{DD}$	V	$3.0\text{ V} \leq V_{DD} \leq 3.6\text{ V}$
		–	–	$0.25 \times V_{DD}$	V	$4.75\text{ V} \leq V_{DD} \leq 5.25\text{ V}$
V_{IH2C}	Input high level	$0.7 \times V_{DD}$	–	–	V	$3.0\text{ V} \leq V_{DD} \leq 5.25\text{ V}$

11.4.3 AC Full Speed USB Specifications

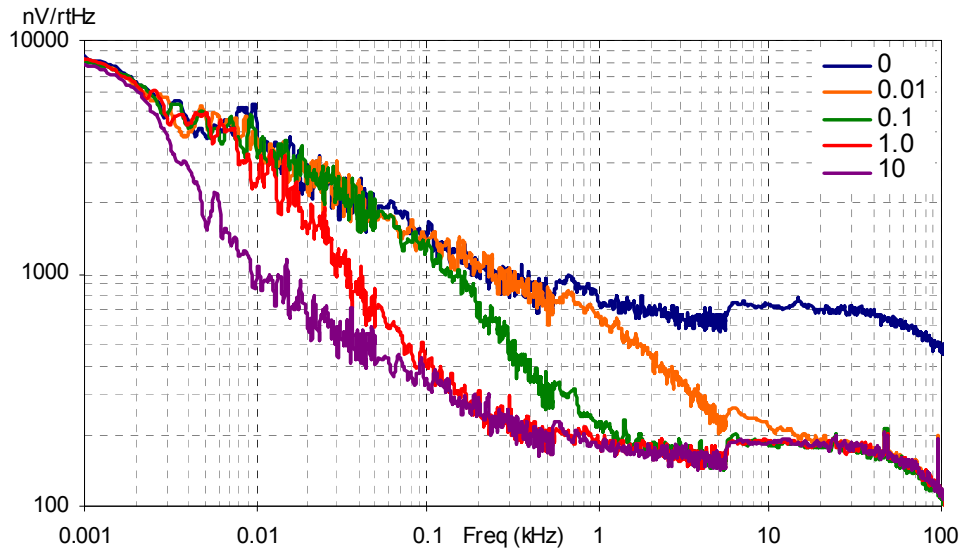
The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-10\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-10\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters are measured at 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 27. AC Full Speed (12 Mbps) USB Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{RFS}	Transition rise time	4	–	20	ns	For 50 pF load
t_{FSS}	Transition fall time	4	–	20	ns	For 50 pF load
t_{RFMFS}	Rise/fall time matching: (t_R/t_F)	90	–	111	%	For 50 pF load
$t_{DRATEFS}$	Full speed data rate	12 – 0.25%	12	12 + 0.25%	Mbps	

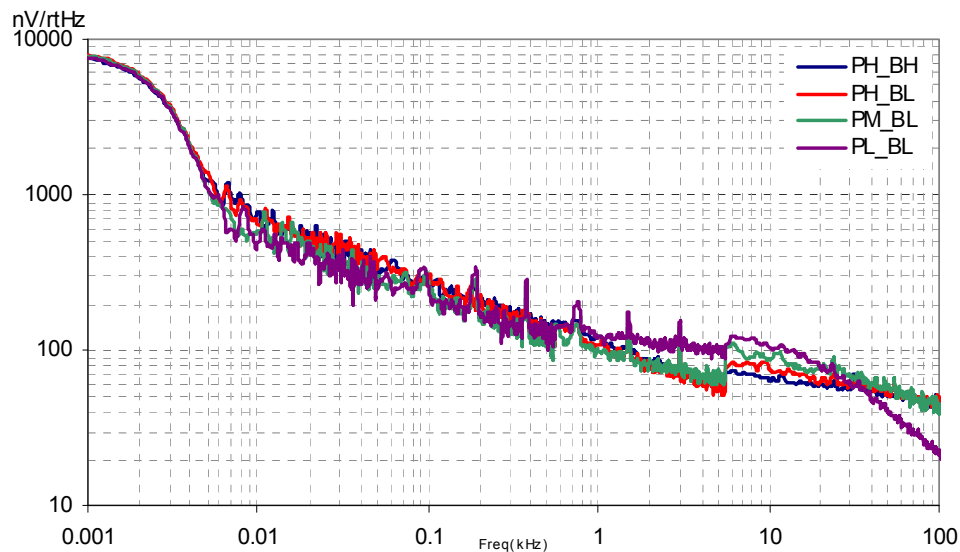
When bypassed by a capacitor on P2[4], the noise of the analog ground signal distributed to each block is reduced by a factor of up to 5 (14 dB). This is at frequencies above the corner frequency defined by the on-chip 8.1 K resistance and the external capacitor.

Figure 13. Typical AGND Noise with P2[4] Bypass



At low frequencies, the opamp noise is proportional to $1/f$, power independent, and determined by device geometry. At high frequencies, increased power level reduces the noise spectrum level.

Figure 14. Typical Opamp Noise



16. Document Conventions

16.1 Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
°C	degree Celsius	mV	millivolt
dB	decibels	nA	nanoampere
fF	femtofarad	ns	nanosecond
kHz	kilohertz	nV	nanovolt
kΩ	kilohms	Ω	ohms
MHz	megahertz	pA	picoampere
μA	microampere	pF	picofarad
μs	microsecond	ps	picosecond
μV	microvolt	%	percent
mA	milliampere	rt-Hz	root hertz
mm	millimeter	V	volt
ms	millisecond	W	watt

16.2 Numeric Conventions

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase 'h' (for example, '14h' or '3Ah'). Hexadecimal numbers may also be represented by a '0x' prefix, the C coding convention. Binary numbers have an appended lowercase 'b' (for example, '01010100b' or '01000011b'). Numbers not indicated by an 'h' or 'b' are decimal.

17. Glossary

active high	6. A logic signal having its asserted state as the logic 1 state. 7. A logic signal having the logic 1 state as the higher voltage of the two states.
analog blocks	The basic programmable opamp circuits. These are SC (switched capacitor) and CT (continuous time) blocks. These blocks can be interconnected to provide ADCs, DACs, multi-pole filters, gain stages, and much more.
analog-to-digital (ADC)	A device that changes an analog signal to a digital signal of corresponding magnitude. Typically, an ADC converts a voltage to a digital number. The digital-to-analog (DAC) converter performs the reverse operation.
API (Application Programming Interface)	A series of software routines that comprise an interface between a computer application and lower level services and functions (for example, user modules and libraries). APIs serve as building blocks for programmers that create software applications.
asynchronous	A signal whose data is acknowledged or acted upon immediately, irrespective of any clock signal.
Bandgap reference	A stable voltage reference design that matches the positive temperature coefficient of VT with the negative temperature coefficient of VBE, to produce a zero temperature coefficient (ideally) reference.
bandwidth	1. The frequency range of a message or information processing system measured in hertz. 2. The width of the spectral region over which an amplifier (or absorber) has substantial gain (or loss); it is sometimes represented more specifically as, for example, full width at half maximum.
bias	1. A systematic deviation of a value from a reference value. 2. The amount by which the average of a set of values departs from a reference value. 3. The electrical, mechanical, magnetic, or other force (field) applied to a device to establish a reference level to operate the device.

When Vdd is pulled below ground before power on, an internal Flash reference may deviate from its nominal voltage. The reference deviation tends to result in the first Flash read from that page returning 0xFF. During the first read from each page, the reference is reset resulting in all future reads returning the correct value. A short delay of 5 μ s before the first real read provides time for the reference voltage to stabilize.

■ WORKAROUND

To prevent an invalid Flash read, a dummy read from each Flash page must occur before use of the pages. A delay of 5 μ s must occur after the dummy read and before a real read. The dummy reads occurs as soon as possible and must be located in Flash page 0 before a read from any other Flash page. An example for reading a byte of memory from each Flash page is listed below. Placed it in boot.tpl and boot.asm immediately after the 'start:' label.

```
// dummy read from each 8K Flash page
// page 1
mov  A, 0x20          // MSB
mov  X, 0x00          // LSB
romx
// wait at least 5  $\mu$ s
mov  X, 14
loop1:
dec  X
jnz  loop1
```