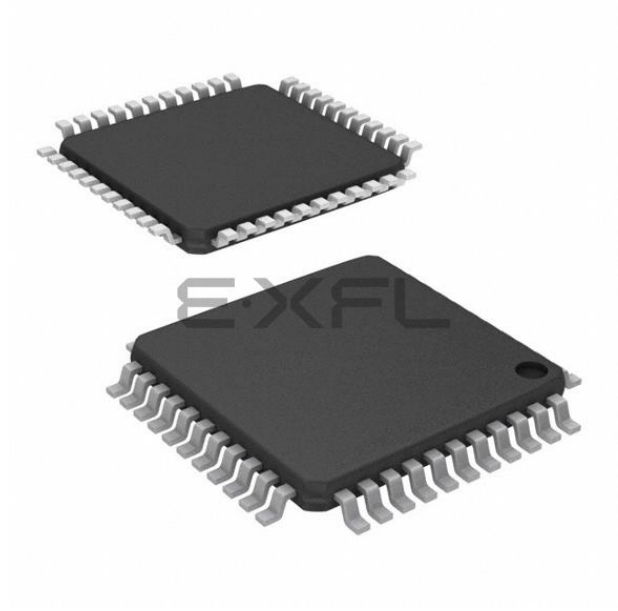


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	LVD, PWM, WDT
Number of I/O	38
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x12b; D/A 2x6b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mke04z128vld4

4. Contents

5. PSoC Functional Overview

The PSoC family consists of many devices with on-chip controllers. These devices are designed to replace multiple traditional MCU-based system components with one low-cost single-chip programmable component. A PSoC device includes configurable blocks of analog and digital logic, and programmable interconnect. This architecture makes it possible for you to create customized peripheral configurations, to match the requirements of each individual application. Additionally, a fast central processing unit (CPU), flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts.

The PSoC architecture, shown in "Logic Block Diagram" on page 1, consists of four main areas: the core, the system resources, the digital system, and the analog system. Configurable global bus resources allow combining all of the device resources into a complete custom system. Each CY8C24x94 PSoC device includes four digital blocks and six analog blocks. Depending on the PSoC package, up to 56 GPIOs are also included. The GPIOs provide access to the global digital and analog interconnects.

5.1 The PSoC Core

The PSoC core is a powerful engine that supports a rich instruction set. It encompasses SRAM for data storage, an interrupt controller, sleep and watchdog timers, and internal main oscillator (IMO) and internal low-speed oscillator (ILO). The CPU core, called the M8C, is a powerful processor with speeds up to 24 MHz. The M8C is a four-million instructions per second (MIPS) 8-bit Harvard-architecture microprocessor.

System resources provide these additional capabilities:

- Digital clocks for increased flexibility
- I^2C functionality to implement an I^2C master and slave
- An internal voltage reference, multi-master, that provides an absolute value of 1.3 V to a number of PSoC subsystems
- A switch-mode pump (SMP) that generates normal operating voltages from a single battery cell
- Various system resets supported by the M8C

The digital system consists of an array of digital PSoC blocks that may be configured into any number of digital peripherals. The digital blocks are connected to the GPIOs through a series of global buses. These buses can route any signal to any pin, freeing designs from the constraints of a fixed peripheral controller.

The analog system consists of six analog PSoC blocks, supporting comparators, and analog-to-digital conversion up to 10-bits of precision.

5.2 The Digital System

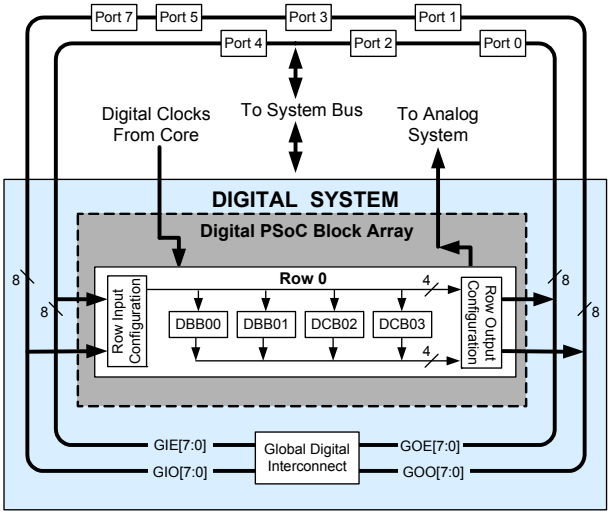
The digital system consists of four digital PSoC blocks. Each block is an 8-bit resource that is used alone or combined with other blocks to form 8-, 16-, 24-, and 32-bit peripherals, which are called user modules. Digital peripheral configurations include:

- PWMs (8- to 32-bit)
- PWMs with dead band (8- to 32-bit)
- Counters (8- to 32-bit)
- Timers (8- to 32-bit)
- UART 8-bit with selectable parity
- SPI master and slave
- I^2C slave and multi-master
- CRC/generator (8-bit)
- IrDA
- PRS generators (8- to 32-bit)

The digital blocks are connected to any GPIO through a series of global buses that can route any signal to any pin. The buses also allow for signal multiplexing and for performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

Digital blocks are provided in rows of four, where the number of blocks varies by PSoC device family. This allows the optimum choice of system resources for your application. Family resources are shown in Table 1 on page 7.

Figure 2. Digital System Block Diagram



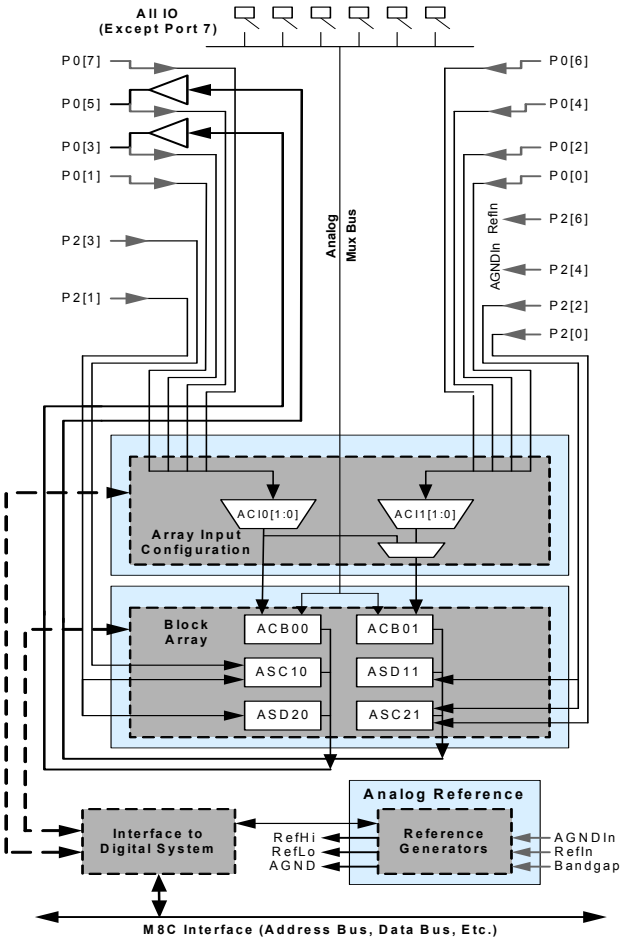
5.3 The Analog System

The analog system is composed of six configurable blocks, each comprised of an opamp circuit allowing the creation of complex analog signal flows. Analog peripherals are very flexible and can be customized to support specific application requirements. Some of the more common PSoC analog functions (most available as user modules) are as follows.

- ADCs (up to two, with 6- to 14-bit resolution, selectable as incremental, delta sigma, and successive approximation register (SAR))
- Filters (2 and 4 pole band-pass, low-pass, and notch)
- Amplifiers (up to two, with selectable gain to 48x)
- Instrumentation amplifiers (one with selectable gain to 93x)
- Comparators (up to two, with 16 selectable thresholds)
- DACs (up to two, with 6- to 9-bit resolution)
- Multiplying DACs (up to two, with 6- to 9-bit resolution)
- High current output drivers (two with 30 mA drive as a PSoC core resource)
- 1.3-V reference (as a system resource)
- DTMF dialer
- Modulators
- Correlators
- Peak detectors
- Many other topologies possible

Analog blocks are arranged in a column of three, which includes one continuous time (CT) and two switched capacitor (SC) blocks, as shown in Figure 3.

Figure 3. Analog System Block Diagram



5.3.1 The Analog Multiplexer System

The analog mux bus can connect to every GPIO pin in ports 0–5. Pins are connected to the bus individually or in any combination. The bus also connects to the analog system for analysis with comparators and analog-to-digital converters. It is split into two sections for simultaneous dual-channel processing. An additional 8:1 analog input multiplexer provides a second path to bring Port 0 pins to the analog array.

Switch-control logic enables selected pins to precharge continuously under hardware control. This enables capacitive measurement for applications such as touch sensing. Other multiplexer applications include:

- Track pad, finger sensing
- Chip-wide mux that enables analog input from up to 48 I/O pins
- Crosspoint connection between any I/O pin combinations

5.4 Additional System Resources

System resources provide additional capability useful to complete systems. Additional resources include a multiplier, decimator, low-voltage detection, and power-on reset (POR). Brief statements describing the merits of each resource follow.

- Full speed USB (12 Mbps) with five configurable endpoints and 256 bytes of RAM. No external components required except for two series resistors. Wider than commercial temperature USB operation (–10 °C to +85 °C).
- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks can be routed to both the digital and analog systems. Additional clocks are generated using digital PSoC blocks as clock dividers.
- Two multiply accumulates (MACs) provide fast 8-bit multipliers with 32-bit accumulate, to assist in both general math and digital filters.
- Decimator provides a custom hardware filter for digital signal processing applications including creation of Delta Sigma ADCs.
- The I^2C module provides 100- and 400-kHz communication over two wires. Slave, master, multi-master are supported.
- Low-voltage detection interrupts signal the application of falling voltage levels, while the advanced POR circuit eliminates the need for a system supervisor.
- An internal 1.3-V reference provides an absolute reference for the analog system, including ADCs and DACs.
- Versatile analog multiplexer system.

5.5 PSoC Device Characteristics

Depending on your PSoC device characteristics, the digital and analog systems can have 16, 8, or 4 digital blocks and 12, 6, or 4 analog blocks. The following table lists the resources available for specific PSoC device groups. The device covered by this datasheet is shown in the highlighted row of the table.

Table 1. PSoC Device Characteristics

PSoC Part Number	Digital I/O	Digital Rows	Digital Blocks	Analog Inputs	Analog Outputs	Analog Columns	Analog Blocks	SRAM Size	Flash Size
CY8C29x66	up to 64	4	16	up to 12	4	4	12	2 K	32 K
CY8C28xxx	up to 44	up to 3	up to 12	up to 44	up to 4	up to 6	up to 12 + 4[1]	1 K	16 K
CY8C27x43	up to 44	2	8	up to 12	4	4	12	256	16 K
CY8C24x94	up to 56	1	4	up to 48	2	2	6	1 K	16 K
CY8C24x23A	up to 24	1	4	up to 12	2	2	6	256	4 K
CY8C23x33	up to 26	1	4	up to 12	2	2	4	256	8 K
CY8C22x45	up to 38	2	8	up to 38	0	4	6[1]	1 K	16 K
CY8C21x45	up to 24	1	4	up to 24	0	4	6[1]	512	8 K
CY8C21x34	up to 28	1	4	up to 28	0	2	4[1]	512	8 K
CY8C21x23	up to 16	1	4	up to 8	0	2	4[1]	256	4 K
CY8C20x34	up to 28	0	0	up to 28	0	0	3[1,2]	512	8 K
CY8C20xx6	up to 36	0	0	up to 36	0	0	3[1,2]	up to 2 K	up to 32 K

Notes
1. Limited analog functionality.
2. Two analog blocks and one CapSense®.

read and write data memory, and read and write I/O registers. You can read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows you to create a trace buffer of registers and memory locations of interest.

7.1.4 Online Help System

The online help system displays online, context-sensitive help. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an online support forum to aid the designer.

7.1.5 In-Circuit Emulator

A low-cost, high-functionality In-Circuit Emulator (ICE) is available for development support. This hardware can program single devices.

The emulator consists of a base unit that connects to the PC using a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full speed (24-MHz) operation.

8. Designing with PSoC Designer

The development process for the PSoC® device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PSoC Blocks, have the ability to implement a wide variety of user-selectable functions. The PSoC development process is summarized in four steps:

1. Select User Modules
2. Configure User Modules
3. Organize and Connect
4. Generate, Verify, and Debug

8.1 Select User Modules

PSoC Designer provides a library of prebuilt, pretested hardware peripheral components called “user modules.” User modules make selecting and implementing peripheral devices, both analog and digital, simple.

8.2 Configure User Modules

Each user module that you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a PWM User Module configures one or more digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit you to establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These user module datasheets explain the internal operation of the user module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information you may need to successfully implement your design.

8.3 Organize and Connect

You build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. You perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

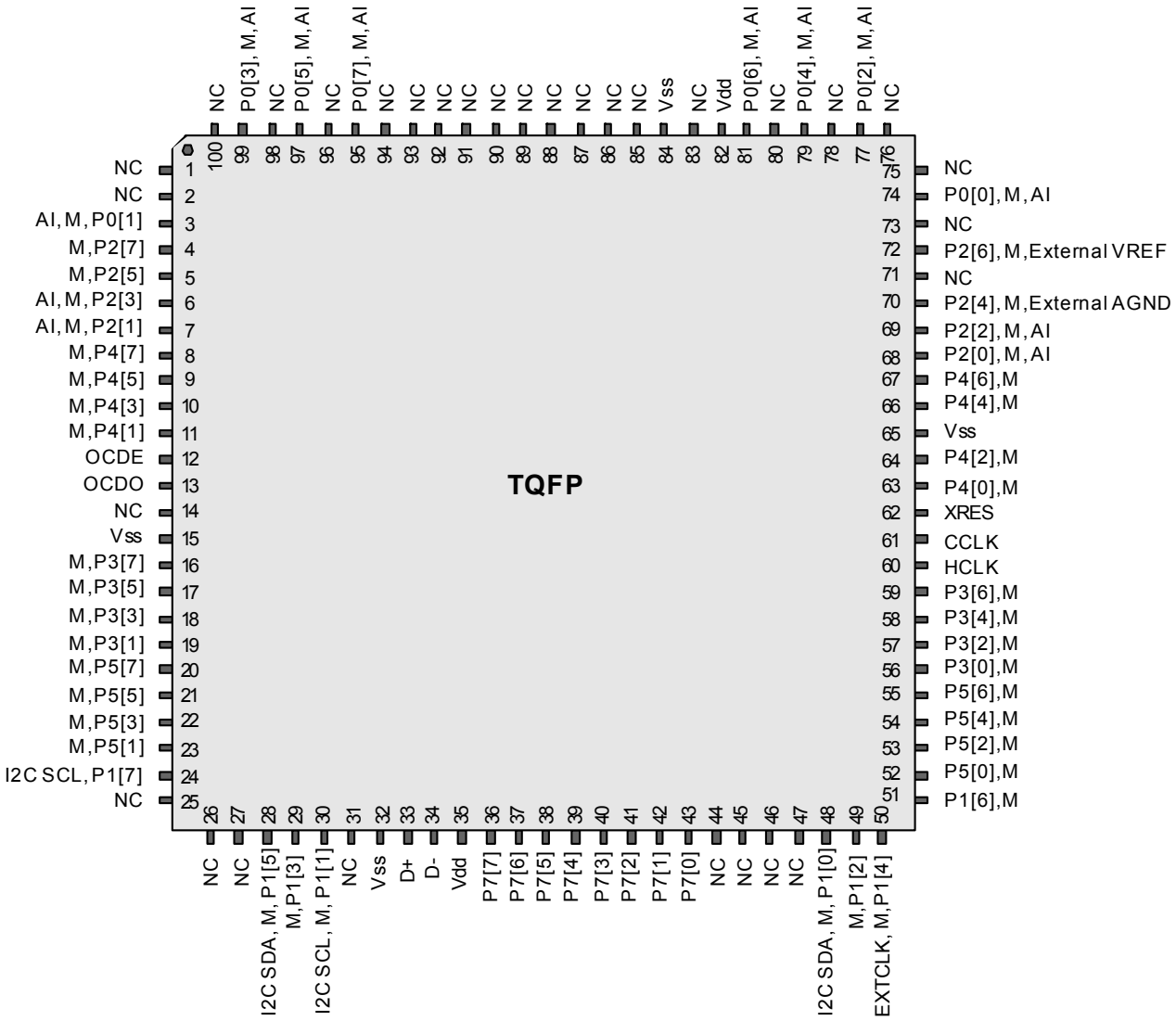
8.4 Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, you perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides application programming interfaces (APIs) with high-level functions to control and respond to hardware events at run time and interrupt service routines that you can adapt as needed.

A complete code development environment allows you to develop and customize your applications in either C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer’s debugger (access by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint, and watch-variable features, the debug interface provides a large trace buffer and allows you to define complex breakpoint events. These include monitoring address and data bus values, memory locations and external signals.

Figure 10. CY8C24094 OCD (Not for Production)



10.3 Register Map Bank 0 Table: User Space

Name	Addr (0, Hex)	Access	Name	Addr (0, Hex)	Access	Name	Addr (0, Hex)	Access	Name	Addr (0, Hex)	Access
PRT0DR	00	RW	PMA0_DR	40	RW	ASC10CR0	80	RW		C0	
PRT0IE	01	RW	PMA1_DR	41	RW	ASC10CR1	81	RW		C1	
PRT0GS	02	RW	PMA2_DR	42	RW	ASC10CR2	82	RW		C2	
PRT0DM2	03	RW	PMA3_DR	43	RW	ASC10CR3	83	RW		C3	
PRT1DR	04	RW	PMA4_DR	44	RW	ASD11CR0	84	RW		C4	
PRT1IE	05	RW	PMA5_DR	45	RW	ASD11CR1	85	RW		C5	
PRT1GS	06	RW	PMA6_DR	46	RW	ASD11CR2	86	RW		C6	
PRT1DM2	07	RW	PMA7_DR	47	RW	ASD11CR3	87	RW		C7	
PRT2DR	08	RW	USB_SOF0	48	R		88			C8	
PRT2IE	09	RW	USB_SOF1	49	R		89			C9	
PRT2GS	0A	RW	USB_CR0	4A	RW		8A			CA	
PRT2DM2	0B	RW	USBI/O_CR0	4B	#		8B			CB	
PRT3DR	0C	RW	USBI/O_CR1	4C	RW		8C			CC	
PRT3IE	0D	RW		4D			8D			CD	
PRT3GS	0E	RW	EP1_CNT1	4E	#		8E			CE	
PRT3DM2	0F	RW	EP1_CNT	4F	RW		8F			CF	
PRT4DR	10	RW	EP2_CNT1	50	#	ASD20CR0	90	RW	CUR_PP	D0	RW
PRT4IE	11	RW	EP2_CNT	51	RW	ASD20CR1	91	RW	STK_PP	D1	RW
PRT4GS	12	RW	EP3_CNT1	52	#	ASD20CR2	92	RW		D2	
PRT4DM2	13	RW	EP3_CNT	53	RW	ASD20CR3	93	RW	IDX_PP	D3	RW
PRT5DR	14	RW	EP4_CNT1	54	#	ASC21CR0	94	RW	MVR_PP	D4	RW
PRT5IE	15	RW	EP4_CNT	55	RW	ASC21CR1	95	RW	MVW_PP	D5	RW
PRT5GS	16	RW	EP0_CR	56	#	ASC21CR2	96	RW	I2C_CFG	D6	RW
PRT5DM2	17	RW	EP0_CNT	57	#	ASC21CR3	97	RW	I2C_SCR	D7	#
	18		EP0_DR0	58	RW		98		I2C_DR	D8	RW
	19		EP0_DR1	59	RW		99		I2C_MSCR	D9	#
	1A		EP0_DR2	5A	RW		9A		INT_CLR0	DA	RW
	1B		EP0_DR3	5B	RW		9B		INT_CLR1	DB	RW
PRT7DR	1C	RW	EP0_DR4	5C	RW		9C		INT_CLR2	DC	RW
PRT7IE	1D	RW	EP0_DR5	5D	RW		9D		INT_CLR3	DD	RW
PRT7GS	1E	RW	EP0_DR6	5E	RW		9E		INT_MSK3	DE	RW
PRT7DM2	1F	RW	EP0_DR7	5F	RW		9F		INT_MSK2	DF	RW
DBB00DR0	20	#	AMX_IN	60	RW		A0		INT_MSK0	E0	RW
DBB00DR1	21	W	AMUXCFG	61	RW		A1		INT_MSK1	E1	RW
DBB00DR2	22	RW		62			A2		INT_VC	E2	RC
DBB00CR0	23	#	ARF_CR	63	RW		A3		RES_WDT	E3	W
DBB01DR0	24	#	CMP_CR0	64	#		A4		DEC_DH	E4	RC
DBB01DR1	25	W	ASY_CR	65	#		A5		DEC_DL	E5	RC
DBB01DR2	26	RW	CMP_CR1	66	RW		A6		DEC_CR0	E6	RW
DBB01CR0	27	#		67			A7		DEC_CR1	E7	RW
DCB02DR0	28	#		68		MUL1_X	A8	W	MUL0_X	E8	W
DCB02DR1	29	W		69		MUL1_Y	A9	W	MUL0_Y	E9	W
DCB02DR2	2A	RW		6A		MUL1_DH	AA	R	MUL0_DH	EA	R
DCB02CR0	2B	#		6B		MUL1_DL	AB	R	MUL0_DL	EB	R
DCB03DR0	2C	#	TMP_DR0	6C	RW	ACC1_DR1	AC	RW	ACC0_DR1	EC	RW
DCB03DR1	2D	W	TMP_DR1	6D	RW	ACC1_DR0	AD	RW	ACC0_DR0	ED	RW
DCB03DR2	2E	RW	TMP_DR2	6E	RW	ACC1_DR3	AE	RW	ACC0_DR3	EE	RW
DCB03CR0	2F	#	TMP_DR3	6F	RW	ACC1_DR2	AF	RW	ACC0_DR2	EF	RW
	30		ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
	31		ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
	32		ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
	34		ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
	35		ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
	36		ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
	37		ACB01CR2	77	RW		B7		CPU_F	F7	RL
	38			78			B8			F8	
	39			79			B9			F9	
	3A			7A			BA			FA	
	3B			7B			BB			FB	
	3C			7C			BC			FC	
	3D			7D			BD		DAC_D	FD	RW
	3E			7E			BE		CPU_SCR1	FE	#
	3F			7F			BF		CPU_SCR0	FF	#

Blank fields are reserved and should not be accessed. # Access is bit specific.

11.3.3 DC Full Speed USB Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –10 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –10 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 13. DC Full Speed (12 Mbps) USB Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
USB Interface						
V_{DI}	Differential input sensitivity	0.2	–	–	V	| (D+) – (D–) |
V_{CM}	Differential input common mode range	0.8	–	2.5	V	
V_{SE}	Single ended receiver threshold	0.8	–	2.0	V	
C_{IN}	Transceiver capacitance	–	–	20	pF	
$I_{I/O}$	High Z state data line leakage	–10	–	10	µA	0 V < V_{IN} < 3.3 V.
R_{EXT}	External USB series resistor	23	–	25	Ω	In series with each USB pin.
V_{UOH}	Static output high, driven	2.8	–	3.6	V	15 kΩ ± 5% to ground. Internal pull-up enabled.
V_{UOHI}	Static output high, idle	2.7	–	3.6	V	15 kΩ ± 5% to ground. Internal pull-up enabled.
V_{UOL}	Static output low	–	–	0.3	V	15 kΩ ± 5% to ground. Internal pull-up enabled.
Z_O	USB driver output impedance	28	–	44	Ω	Including R_{EXT} resistor.
V_{CRS}	D+/D– crossover voltage	1.3	–	2.0	V	

Table 18. 3.3-V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
C_L	Load Capacitance	–	–	200	pF	This specification applies to the external circuit that is being driven by the analog output buffer.
V_{OSOB}	Input offset voltage (absolute value)	–	3	12	mV	
TCV_{OSOB}	Average input offset voltage drift	–	+6	–	µV/°C	
V_{CMOB}	Common mode input voltage range	0.5	–	V_{DD} – 1.0	V	
R_{OUTOB}	Output resistance Power = low Power = high	 – –	 1 1	 – –	 W W	
$V_{OHIGHOB}$	High output voltage swing (Load = 1 K ohms to $V_{DD}/2$) Power = low Power = high	 $0.5 \times V_{DD} + 1.0$ $0.5 \times V_{DD} + 1.0$	 – –	 – –	 V V	
V_{OLOWOB}	Low output voltage swing (Load = 1 K ohms to $V_{DD}/2$) Power = low Power = high	 – –	 – –	 $0.5 \times V_{DD} - 1.0$ $0.5 \times V_{DD} - 1.0$	 V V	
I_{SOB}	Supply current including opamp bias cell (No load) Power = low Power = high	 – –	 0.8 2.0	 2.0 4.3	 mA mA	
$PSRR_{OB}$	Supply voltage rejection ratio	34	64	–	dB	$(0.5 \times V_{DD} - 1.0) \le V_{OUT} \le (0.5 \times V_{DD} + 0.9)$.

Table 19. 5-V DC Analog Reference Specifications *(continued)*

Refer-ence ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b111	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	3.2 × Bandgap	4.028	4.144	4.242	V
		V_{AGND}	AGND	1.6 × Bandgap	2.028	2.076	2.125	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.008	V_{SS} + 0.034	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	3.2 × Bandgap	4.032	4.142	4.245	V
		V_{AGND}	AGND	1.6 × Bandgap	2.029	2.076	2.126	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.005	V_{SS} + 0.025	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	3.2 × Bandgap	4.034	4.143	4.247	V
		V_{AGND}	AGND	1.6 × Bandgap	2.029	2.076	2.126	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.004	V_{SS} + 0.021	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	3.2 × Bandgap	4.036	4.144	4.249	V
		V_{AGND}	AGND	1.6 × Bandgap	2.029	2.076	2.126	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.003	V_{SS} + 0.019	V

Table 20. 3.3-V DC Analog Reference Specifications *(continued)*

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b110	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	2 × Bandgap	2.510	2.595	2.655	V
		V_{AGND}	AGND	Bandgap	1.276	1.301	1.332	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.006	V_{SS} + 0.031	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	2 × Bandgap	2.513	2.594	2.656	V
		V_{AGND}	AGND	Bandgap	1.275	1.301	1.331	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.004	V_{SS} + 0.021	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	2 × Bandgap	2.516	2.595	2.657	V
		V_{AGND}	AGND	Bandgap	1.275	1.301	1.331	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.003	V_{SS} + 0.017	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	2 × Bandgap	2.520	2.595	2.658	V
		V_{AGND}	AGND	Bandgap	1.275	1.300	1.331	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.002	V_{SS} + 0.015	V
0b111	All power settings. Not allowed for 3.3 V.	–	–	–	–	–	–	–

11.3.8 DC Analog PSoC Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 21. DC Analog PSoC Block Specifications

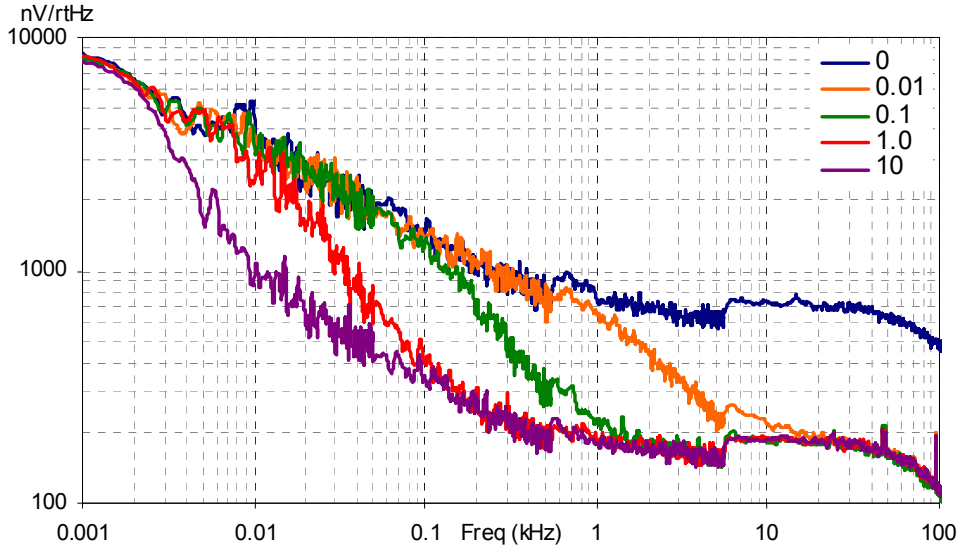
Symbol	Description	Min	Typ	Max	Units	Notes
R_{CT}	Resistor unit value (continuous time)	–	12.2	–	kΩ	
C_{SC}	Capacitor unit value (switched capacitor)	–	80	–	fF	

11.3.9 DC POR and LVD Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V or 3.3 V at 25 °C and are for design guidance only.

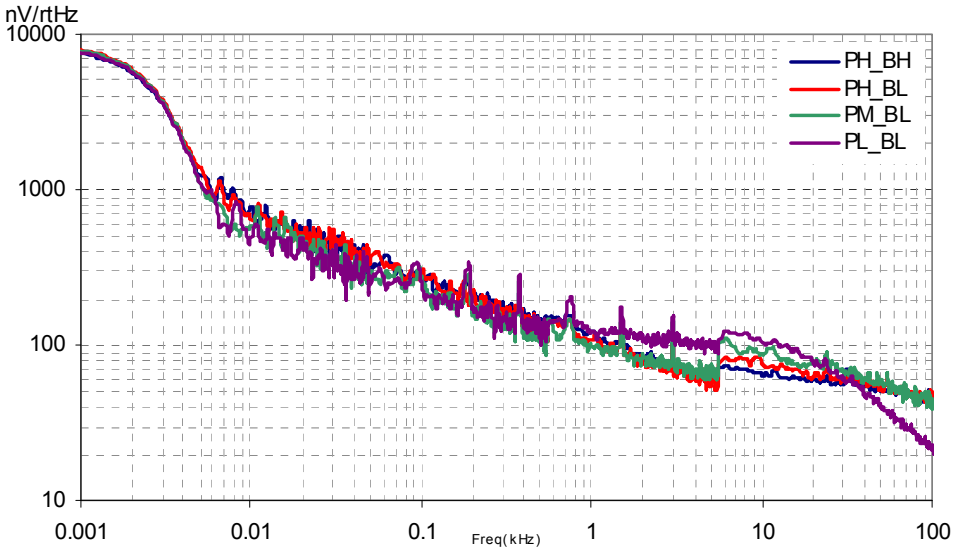
When bypassed by a capacitor on P2[4], the noise of the analog ground signal distributed to each block is reduced by a factor of up to 5 (14 dB). This is at frequencies above the corner frequency defined by the on-chip 8.1 K resistance and the external capacitor.

Figure 13. Typical AGND Noise with P2[4] Bypass



At low frequencies, the opamp noise is proportional to 1/f, power independent, and determined by device geometry. At high frequencies, increased power level reduces the noise spectrum level.

Figure 14. Typical Opamp Noise



11.4.9 AC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 35. AC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{RSCLK}	Rise time of SCLK	1	–	20	ns	
t_{FSCLK}	Fall time of SCLK	1	–	20	ns	
t_{SSCLK}	Data setup time to falling edge of SCLK	40	–	–	ns	
t_{HSCLK}	Data hold time from falling edge of SCLK	40	–	–	ns	
F_{SCLK}	Frequency of SCLK	0	–	8	MHz	
t_{ERASEB}	Flash erase time (block)	–	10	–	ms	
t_{WRITE}	Flash block write time	–	40	–	ms	
t_{DSCLK}	Data out delay from falling edge of SCLK	–	–	45	ns	V_{DD} > 3.6
t_{DSCLK3}	Data out delay from falling edge of SCLK	–	–	50	ns	3.0 ≤ V_{DD} ≤ 3.6
$t_{ERASEALL}$	Flash erase time (bulk)	–	40	–	ms	Erase all blocks and protection fields at once
$t_{PROGRAM\_HOT}$	Flash block erase + flash block write time	–	–	100[34]	ms	0 °C ≤ Tj ≤ 100 °C
$t_{PROGRAM\_COLD}$	Flash block erase + flash block write time	–	–	200[34]	ms	–40 °C ≤ Tj ≤ 0 °C

Note

34. For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. See the Flash APIs application note Design Aids – Reading and Writing PSoC® Flash – AN2015 for more information.

11.5 Thermal Impedance

Table 37. Thermal Impedances per Package

Package	Typical θ_{JA} [36]
56-Pin QFN[37]	12.93 °C/W
68-Pin QFN[37]	13.05 °C/W
100-Ball VFBGA	65 °C/W
100-Pin TQFP	51 °C/W

11.6 Solder Reflow Peak Specifications

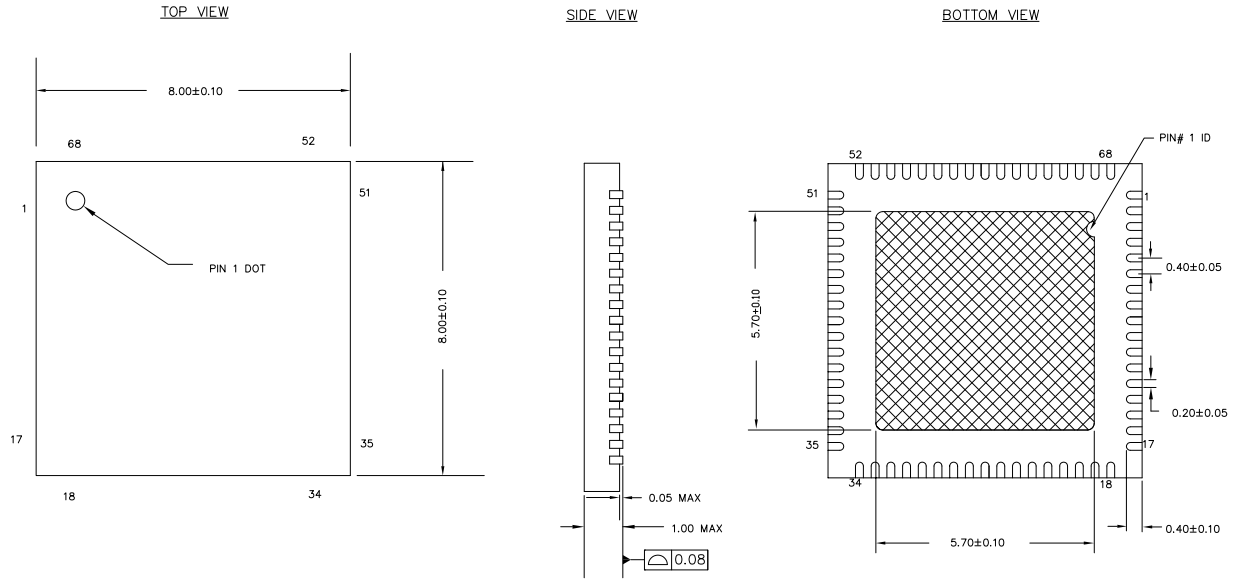
Table 38 shows the solder reflow temperature limits that must not be exceeded.

Table 38. Solder Reflow Specifications

Package	Maximum Peak Temperature (T_C)	Maximum Time above T_C – 5 °C
56-Pin QFN	260 °C	30 seconds
68-Pin QFN	260 °C	30 seconds
100-Ball VFBGA	260 °C	30 seconds
100-Pin TQFP	260 °C	30 seconds

Notes
36. $T_J = T_A + POWER \times \theta_{JA}$.
37. To achieve the thermal impedance specified for the QFN package, see the *Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages* available at http://www.amkor.com.

Figure 19. 68-pin QFN (8 × 8 × 1.0 mm) LT68 5.7 × 5.7 E-Pad (Sawn Type) Package Outline, 001-09618

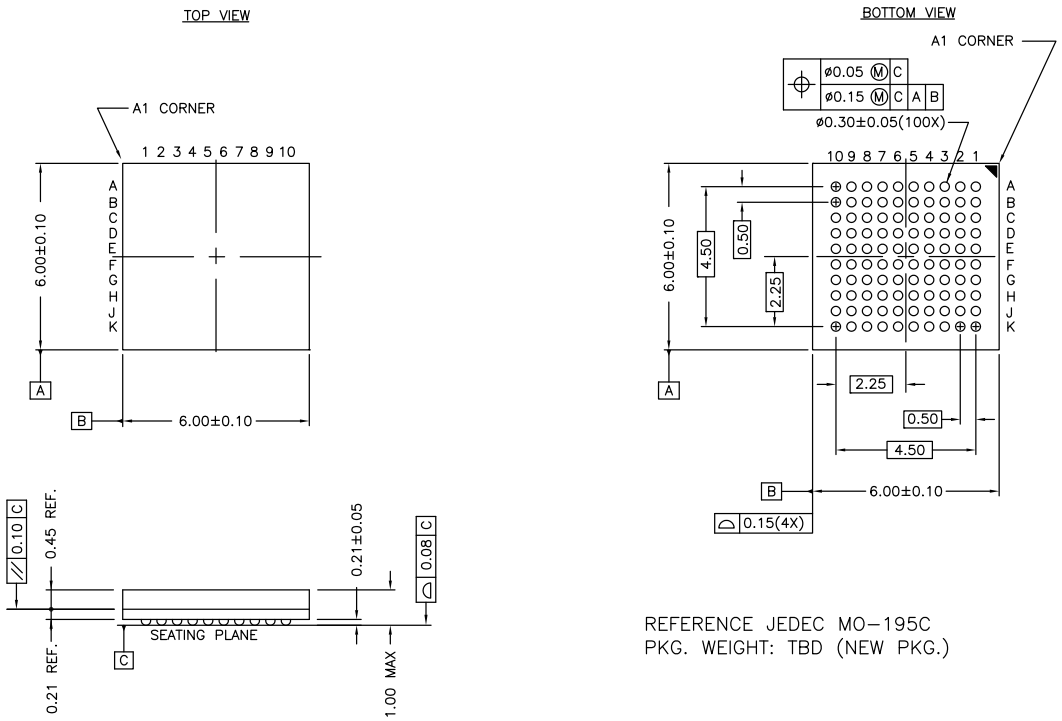


NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO−220
3. PACKAGE WEIGHT: 17 ± 2mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-09618 *E

Figure 20. 100-ball VFBGA (6 × 6 × 1.0 mm) BZ100 Package Outline, 51-85209



17. Glossary *(continued)*

block	1. A functional unit that performs a single function, such as an oscillator. 2. A functional unit that may be configured to perform one of several functions, such as a digital PSoC block or an analog PSoC block.
buffer	1. A storage area for data that is used to compensate for a speed difference, when transferring data from one device to another. Usually refers to an area reserved for IO operations, into which data is read, or from which data is written. 2. A portion of memory set aside to store data, often before it is sent to an external device or as it is received from an external device. 3. An amplifier used to lower the output impedance of a system.
bus	1. A named connection of nets. Bundling nets together in a bus makes it easier to route nets with similar routing patterns. 2. A set of signals performing a common function and carrying similar data. Typically represented using vector notation; for example, address[7:0]. 3. One or more conductors that serve as a common connection for a group of related devices.
clock	The device that generates a periodic signal with a fixed frequency and duty cycle. A clock is sometimes used to synchronize different logic blocks.
comparator	An electronic circuit that produces an output voltage or current whenever two input levels simultaneously satisfy predetermined amplitude requirements.
compiler	A program that translates a high level language, such as C, into machine language.
configuration space	In PSoC devices, the register space accessed when the XIO bit, in the CPU_F register, is set to ‘1’.
crystal oscillator	An oscillator in which the frequency is controlled by a piezoelectric crystal. Typically a piezoelectric crystal is less sensitive to ambient temperature than other circuit components.
cyclic redundancy check (CRC)	A calculation used to detect errors in data communications, typically performed using a linear feedback shift register. Similar calculations may be used for a variety of other purposes such as data compression.
data bus	A bi-directional set of signals used by a computer to convey information from a memory location to the central processing unit and vice versa. More generally, a set of signals used to convey data between digital functions.
debugger	A hardware and software system that allows the user to analyze the operation of the system under development. A debugger usually allows the developer to step through the firmware one step at a time, set break points, and analyze memory.
dead band	A period of time when neither of two or more signals are in their active state or in transition.
digital blocks	The 8-bit logic blocks that can act as a counter, timer, serial receiver, serial transmitter, CRC generator, pseudo-random number generator, or SPI.
digital-to-analog (DAC)	A device that changes a digital signal to an analog signal of corresponding magnitude. The analog-to-digital (ADC) converter performs the reverse operation.
duty cycle	The relationship of a clock period high time to its low time, expressed as a percent.
emulator	Duplicates (provides an emulation of) the functions of one system with a different system, so that the second system appears to behave like the first system.

17. Glossary *(continued)*

external reset (XRES)	An active high signal that is driven into the PSoC device. It causes all operation of the CPU and blocks to stop and return to a pre-defined state.
flash	An electrically programmable and erasable, non-volatile technology that provides users with the programmability and data storage of EPROMs, plus in-system erasability. Non-volatile means that the data is retained when power is off.
Flash block	The smallest amount of Flash ROM space that may be programmed at one time and the smallest amount of Flash space that may be protected. A Flash block holds 64 bytes.
frequency	The number of cycles or events per unit of time, for a periodic function.
gain	The ratio of output current, voltage, or power to input current, voltage, or power, respectively. Gain is usually expressed in dB.
I^2C	A two-wire serial computer bus by Philips Semiconductors (now NXP Semiconductors). I2C is an Inter-Integrated Circuit. It is used to connect low-speed peripherals in an embedded system. The original system was created in the early 1980s as a battery control interface, but it was later used as a simple internal bus system for building control electronics. I2C uses only two bi-directional pins, clock and data, both running at +5V and pulled high with resistors. The bus operates at 100 kbits/second in standard mode and 400 kbits/second in fast mode.
ICE	The in-circuit emulator that allows users to test the project in a hardware environment, while viewing the debugging device activity in a software environment (PSoC Designer).
input/output (I/O)	A device that introduces data into or extracts data from a system.
interrupt	A suspension of a process, such as the execution of a computer program, caused by an event external to that process, and performed in such a way that the process can be resumed.
interrupt service routine (ISR)	A block of code that normal code execution is diverted to when the M8C receives a hardware interrupt. Many interrupt sources may each exist with its own priority and individual ISR code block. Each ISR code block ends with the RETI instruction, returning the device to the point in the program where it left normal program execution.
jitter	1. A misplacement of the timing of a transition from its ideal position. A typical form of corruption that occurs on serial data streams. 2. The abrupt and unwanted variations of one or more signal characteristics, such as the interval between successive pulses, the amplitude of successive cycles, or the frequency or phase of successive cycles.
low-voltage detect (LVD)	A circuit that senses V_{DD} and provides an interrupt to the system when V_{DD} falls lower than a selected threshold.
M8C	An 8-bit Harvard-architecture microprocessor. The microprocessor coordinates all activity inside a PSoC by interfacing to the Flash, SRAM, and register space.
master device	A device that controls the timing for data exchanges between two devices. Or when devices are cascaded in width, the master device is the one that controls the timing for data exchanges between the cascaded devices and an external interface. The controlled device is called the ***slave device.***
microcontroller	An integrated circuit chip that is designed primarily for control systems and products. In addition to a CPU, a microcontroller typically includes memory, timing circuits, and IO circuitry. The reason for this is to permit the realization of a controller with a minimal quantity of chips, thus achieving maximal possible miniaturization. This in turn, reduces the volume and the cost of the controller. The microcontroller is normally not used for general-purpose computation as is a microprocessor.
mixed-signal	The reference to a circuit containing both analog and digital techniques and components.

17. Glossary *(continued)*

SRAM	An acronym for static random access memory. A memory device allowing users to store and retrieve data at a high rate of speed. The term static is used because, after a value has been loaded into an SRAM cell, it remains unchanged until it is explicitly altered or until power is removed from the device.
SROM	An acronym for supervisory read only memory. The SROM holds code that is used to boot the device, calibrate circuitry, and perform Flash operations. The functions of the SROM may be accessed in normal user code, operating from Flash.
stop bit	A signal following a character or block that prepares the receiving device to receive the next character or block.
synchronous	1. A signal whose data is not acknowledged or acted upon until the next active edge of a clock signal. 2. A system whose operation is synchronized by a clock signal.
tristate	A function whose output can adopt three states: 0, 1, and Z (high-impedance). The function does not drive any value in the Z state and, in many respects, may be considered to be disconnected from the rest of the circuit, allowing another output to drive the same net.
UART	A UART or universal asynchronous receiver-transmitter translates between parallel bits of data and serial bits.
user modules	Pre-build, pre-tested hardware/firmware peripheral functions that take care of managing and configuring the lower level Analog and Digital PSoC Blocks. User Modules also provide high level ***API (Application Programming Interface)*** for the peripheral function.
user space	The bank 0 space of the register map. The registers in this bank are more likely to be modified during normal program execution and not just during initialization. Registers in bank 1 are most likely to be modified only during the initialization phase of the program.
V_{DD}	A name for a power net meaning "voltage drain." The most positive power supply signal. Usually 5 V or 3.3 V.
V_{SS}	A name for a power net meaning "voltage source." The most negative power supply signal.
watchdog timer	A timer that must be serviced periodically. If it is not serviced, the CPU resets after a specified period of time.

When Vdd is pulled below ground before power on, an internal Flash reference may deviate from its nominal voltage. The reference deviation tends to result in the first Flash read from that page returning 0xFF. During the first read from each page, the reference is reset resulting in all future reads returning the correct value. A short delay of 5 µs before the first real read provides time for the reference voltage to stabilize.

■ **WORKAROUND**

To prevent an invalid Flash read, a dummy read from each Flash page must occur before use of the pages. A delay of 5 µs must occur after the dummy read and before a real read. The dummy reads occurs as soon as possible and must be located in Flash page 0 before a read from any other Flash page. An example for reading a byte of memory from each Flash page is listed below. Placed it in boot.tpl and boot.asm immediately after the ‘start:’ label.

```
// dummy read from each 8K Flash page
// page 1
mov  A, 0x20        // MSB
mov  X, 0x00        // LSB
romx
// wait at least 5 µs
mov  X, 14
loop1:
dec  X
jnz  loop1
```