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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I²C, LINbus, UART/USART, USB
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	51
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 9x8/12b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f110meafb-30

1.2 Ordering Information

Products with USB

Pin Count	Package	Fields of Application	Orderable Part Number
80 pins	80-pin plastic LFQFP (12 × 12 mm, 0.5 mm pitch)	A	R5F110MEAFB#30, R5F110MFAFB#30, R5F110MGAFB#30, R5F110MHAFB#30, R5F110MJAFB#30 R5F110MEAFB#50, R5F110MFAFB#50, R5F110MGAFB#50, R5F110MHAFB#50, R5F110MJAFB#50
		G	R5F110MEGFB#30, R5F110MFGFB#30, R5F110MGGFB#30, R5F110MHGFB#30, R5F110MJGFB#30 R5F110MEGFB#50, R5F110MFGFB#50, R5F110MGGFB#50, R5F110MHGFB#50, R5F110MJGFB#50
85 pins	85-pin plastic VFLGA (7 × 7 mm, 0.65 mm pitch)	A	R5F110NEALA#U0, R5F110NFALA#U0, R5F110NGALA#U0, R5F110NHALA#U0, R5F110NJALA#U0 R5F110NEALA#W0, R5F110NFALA#W0, R5F110NGALA#W0, R5F110NHALA#W0, R5F110NJALA#W0
		G	R5F110NEGLA#U0, R5F110NFGLA#U0, R5F110NGGLA#U0, R5F110NHGLA#U0, R5F110NJGLA#U0 R5F110NEGLA#W0, R5F110NFGLA#W0, R5F110NGGLA#W0, R5F110NHGLA#W0, R5F110NJGLA#W0
100 pins	100-pin plastic LFQFP (14 × 14 mm, 0.5 mm pitch)	A	R5F110PEAFB#30, R5F110PFAFB#30, R5F110PGAFB#30, R5F110PHAFB#30, R5F110PJAFB#30 R5F110PEAFB#50, R5F110PFAFB#50, R5F110PGAFB#50, R5F110PHAFB#50, R5F110PJAFB#50
		G	R5F110PEGFB#30, R5F110PFGFB#30, R5F110PGGFB#30, R5F110PHGFB#30, R5F110PJGFB#30 R5F110PEGFB#50, R5F110PFGFB#50, R5F110PGGFB#50, R5F110PHGFB#50, R5F110PJGFB#50

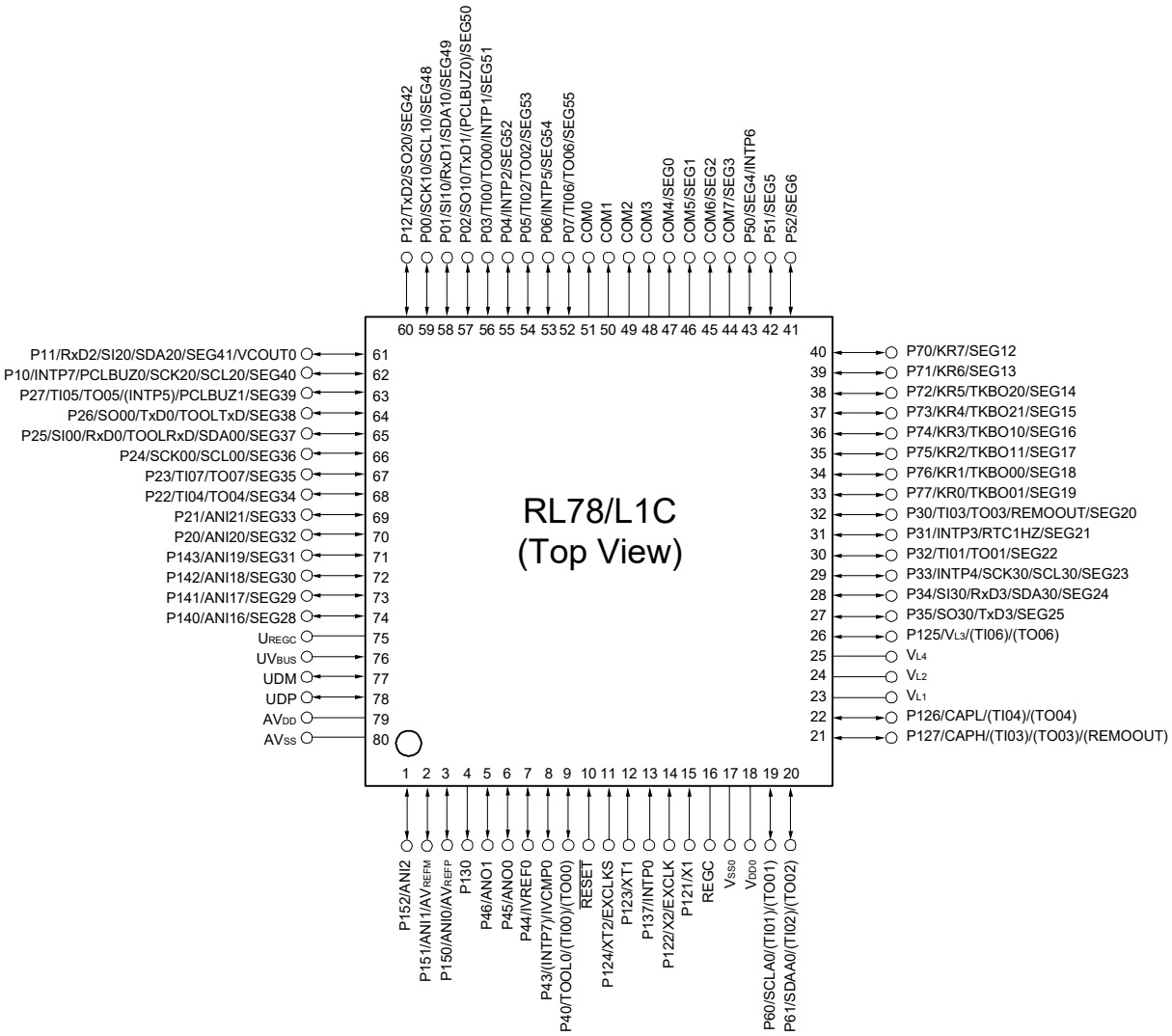
Products without USB

Pin Count	Package	Fields of Application	Orderable Part Number
80 pins	80-pin plastic LFQFP (12 × 12 mm, 0.5 mm pitch)	A	R5F111MEAFB#30, R5F111MFAFB#30, R5F111MGAFB#30, R5F111MHAFB#30, R5F111MJAFB#30 R5F111MEAFB#50, R5F111MFAFB#50, R5F111MGAFB#50, R5F111MHAFB#50, R5F111MJAFB#50
		G	R5F111MEGFB#30, R5F111MFGFB#30, R5F111MGGFB#30, R5F111MHGFB#30, R5F111MJGFB#30 R5F111MEGFB#50, R5F111MFGFB#50, R5F111MGGFB#50, R5F111MHGFB#50, R5F111MJGFB#50
85 pins	85-pin plastic VFLGA (7 × 7 mm, 0.65 mm pitch)	A	R5F111NEALA#U0, R5F111NFALA#U0, R5F111NGALA#U0, R5F111NHALA#U0, R5F111NJALA#U0 R5F111NEALA#W0, R5F111NFALA#W0, R5F111NGALA#W0, R5F111NHALA#W0, R5F111NJALA#W0
		G	R5F111NEGLA#U0, R5F111NFGLA#U0, R5F111NGGLA#U0, R5F111NHGLA#U0, R5F111NJGLA#U0 R5F111NEGLA#W0, R5F111NFGLA#W0, R5F111NGGLA#W0, R5F111NHGLA#W0, R5F111NJGLA#W0
100 pins	100-pin plastic LFQFP (14 × 14 mm, 0.5 mm pitch)	A	R5F111PEAFB#30, R5F111PFAFB#30, R5F111PGAFB#30, R5F111PHAFB#30, R5F111PJAFB#30 R5F111PEAFB#50, R5F111PFAFB#50, R5F111PGAFB#50, R5F111PHAFB#50, R5F111PJAFB#50
		G	R5F111PEGFB#30, R5F111PFGFB#30, R5F111PGGFB#30, R5F111PHGFB#30, R5F111PJGFB#30 R5F111PEGFB#50, R5F111PFGFB#50, R5F111PGGFB#50, R5F111PHGFB#50, R5F111PJGFB#50

1.3 Pin Configuration (Top View)

1.3.1 80-pin products (with USB)

• 80-pin plastic LFQFP (12 × 12 mm, 0.5 mm pitch)



Caution 1. Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 µF).

Caution 2. Connect the UREGC pin to Vss pin via a capacitor (0.33 µF).

Remark 1. For pin identification, see **1.4 Pin Identification**.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

Absolute Maximum Ratings (T_A = 25°C) **(3/3)**

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	I_{OH1}	Per pin	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P46, P50 to P57, P70 to P77, P80 to P83, P125 to P127, P130, P140 to P143	-40	mA
		Total of all pins -170 mA	P40 to P46	-70	mA
			P00 to P07, P10 to P17, P20 to P27, P30 to P37, P50 to P57, P70 to P77, P80 to P83, P125 to P127, P130, P140 to P143	-100	mA
	I_{OH2}	Per pin	P150 to P156	-0.1	mA
		Total of all pins		-0.7	mA
	I_{OH3}	Per pin	UDP, UDM	-3	mA
Output current, low	I_{OL1}	Per pin	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P46, P50 to P57, P60, P61, P70 to P77, P80 to P83, P125 to P127, P130, P140 to P143	40	mA
		Total of all pins 170 mA	P40 to P46	70	mA
			P00 to P07, P10 to P17, P20 to P27, P30 to P37, P50 to P57, P70 to P77, P80 to P83, P125 to P127, P130, P140 to P143	100	mA
	I_{OL2}	Per pin	P150 to P156	0.4	mA
		Total of all pins		2.8	mA
	I_{OL3}	Per pin	UDP, UDM	3	mA
Operating ambient temperature	T_A	In normal operation mode		-40 to +85	°C
		In flash memory programming mode			
Storage temperature	T_{stg}			-65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.3.2 Supply current characteristics

(T_A = -40 to +85°C, 1.6 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V) **(1/2)**

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD1}	Operating mode	HS (high-speed main) mode Note 5	f_{HOCO} = 48 MHz Note 3, f_{IH} = 24 MHz Note 3	Basic operation	V_{DD} = 3.6 V		2.2	2.8	mA
						V_{DD} = 3.0 V		2.2	2.8	
					Normal operation	V_{DD} = 3.6 V		4.4	8.5	
						V_{DD} = 3.0 V		4.4	8.5	
				f_{HOCO} = 24 MHz Note 3, f_{IH} = 24 MHz Note 3	Basic operation	V_{DD} = 3.6 V		2.0	2.6	
						V_{DD} = 3.0 V		2.0	2.6	
					Normal operation	V_{DD} = 3.6 V		4.2	6.8	
						V_{DD} = 3.0 V		4.2	6.8	
				f_{HOCO} = 16 MHz Note 3, f_{IH} = 16 MHz Note 3	Normal operation	V_{DD} = 3.6 V		3.1	4.9	
						V_{DD} = 3.0 V		3.1	4.9	
			LS (low-speed main) mode Note 5	f_{HOCO} = 8 MHz Note 3, f_{IH} = 8 MHz Note 3	Normal operation	V_{DD} = 3.0 V		1.4	2.2	mA
						V_{DD} = 2.0 V		1.4	2.2	
			LV (low-voltage main) mode Note 5	f_{HOCO} = 4 MHz Note 3, f_{IH} = 4 MHz Note 3	Normal operation	V_{DD} = 3.0 V		1.3	1.8	mA
						V_{DD} = 2.0 V		1.3	1.8	
			HS (high-speed main) mode Note 5	f_{MX} = 20 MHz Note 2, V_{DD} = 3.6 V	Normal operation	Square wave input		3.5	5.5	mA
						Resonator connection		3.6	5.7	
				f_{MX} = 20 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		3.5	5.5	
						Resonator connection		3.6	5.7	
				f_{MX} = 16 MHz Note 2, V_{DD} = 3.6 V	Normal operation	Square wave input		2.9	4.5	
						Resonator connection		3.1	4.6	
				f_{MX} = 16 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		2.9	4.5	
						Resonator connection		3.1	4.6	
				f_{MX} = 10 MHz Note 2, V_{DD} = 3.6 V	Normal operation	Square wave input		2.1	3.2	
						Resonator connection		2.2	3.2	
				f_{MX} = 10 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		2.1	3.2	
						Resonator connection		2.2	3.2	
			LS (low-speed main) mode Note 5	f_{MX} = 8 MHz Note 2, V_{DD} = 3.6 V	Normal operation	Square wave input		1.2	2.0	mA
						Resonator connection		1.3	2.0	
				f_{MX} = 8 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		1.2	2.1	
						Resonator connection		1.3	2.2	
			HS (High-speed main) mode (PLL operation)	f_{PLL} = 48 MHz, f_{CLK} = 24 MHz Note 2	Normal operation	V_{DD} = 3.6 V		4.7	7.5	mA
						V_{DD} = 3.0 V		4.7	7.5	
				f_{PLL} = 48 MHz, f_{CLK} = 12 MHz Note 2	Normal operation	V_{DD} = 3.6 V		3.1	5.1	
						V_{DD} = 3.0 V		3.1	5.1	
				f_{PLL} = 48 MHz, f_{CLK} = 6 MHz Note 2	Normal operation	V_{DD} = 3.6 V		2.3	3.9	
						V_{DD} = 3.0 V		2.3	3.9	
			Subsystem clock operation	f_{SUB} = 32.768 kHz Note 4 T_A = -40°C	Normal operation	Square wave input		4.6	6.9	μA
						Resonator connection		4.7	6.9	
				f_{SUB} = 32.768 kHz Note 4 T_A = +25°C	Normal operation	Square wave input		4.9	7.0	
						Resonator connection		5.0	7.2	
				f_{SUB} = 32.768 kHz Note 4 T_A = +50°C	Normal operation	Square wave input		5.2	7.6	
						Resonator connection		5.2	7.7	
				f_{SUB} = 32.768 kHz Note 4 T_A = +70°C	Normal operation	Square wave input		5.5	9.3	
						Resonator connection		5.6	9.4	
				f_{SUB} = 32.768 kHz Note 4 T_A = +85°C	Normal operation	Square wave input		6.2	13.3	
						Resonator connection		6.2	13.4	

(**Notes** and **Remarks** are listed on the next page.)

(6) Communication at different potential (1.8 V, 2.5 V) (UART mode)

(T_A = -40 to +85°C, 1.8 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V) **(1/2)**

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate Notes 1, 2		reception	2.7 V ≤ V_{DD} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V		f_{MCK}/6 Note 1		f_{MCK}/6 Note 1		f_{MCK}/6 Note 1	bps
			Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 4		4.0		1.3		0.6	Mbps
			1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V		f_{MCK}/6 Notes 1, 2, 3		f_{MCK}/6 Notes 1, 2, 3		f_{MCK}/6 Notes 1, 2, 3	bps
			Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 4		4.0		1.3		0.6	Mbps

Note 1. Transfer rate in the SNOOZE mode is 4,800 bps only.

Note 2. Use it with $V_{DD} \geq V_b$.

Note 3. The following conditions are required for low voltage interface.
2.4 V ≤ V_{DD} < 2.7 V: MAX. 2.6 Mbps
1.8 V ≤ V_{DD} < 2.4 V: MAX. 1.3 Mbps
1.6 V ≤ V_{DD} < 1.8 V: MAX. 0.6 Mbps

Note 4. The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:
HS (high-speed main) mode: 24 MHz (2.7 V ≤ V_{DD} ≤ 3.6 V)
16 MHz (2.4 V ≤ V_{DD} ≤ 3.6 V)
LS (low-speed main) mode: 8 MHz (1.8 V ≤ V_{DD} ≤ 3.6 V)
LV (low-voltage main) mode: 4 MHz (1.6 V ≤ V_{DD} ≤ 3.6 V)

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Remark 1. V_b[V]: Communication line voltage

Remark 2. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0 to 3)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

(9) Communication at different potential (1.8 V, 2.5 V) (CSI mode) (slave mode, SCKp... external clock input)

(T_A = -40 to +85°C, 1.8 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time Note 1	t_{KCY2}	2.7 V ≤ V_{DD} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V	20 MHz < f_{MCK} ≤ 24 MHz	16/f_{MCK}		—		—		ns
			16 MHz < f_{MCK} ≤ 20 MHz	14/f_{MCK}		—		—		ns
			8 MHz < f_{MCK} ≤ 16 MHz	12/f_{MCK}		—		—		ns
			4 MHz < f_{MCK} ≤ 8 MHz	8/f_{MCK}		16/f_{MCK}		—		ns
			f_{MCK} ≤ 4 MHz	6/f_{MCK}		10/f_{MCK}		10/f_{MCK}		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2	20 MHz < f_{MCK} ≤ 24 MHz	36/f_{MCK}		—		—		ns
			16 MHz < f_{MCK} ≤ 20 MHz	32/f_{MCK}		—		—		ns
			8 MHz < f_{MCK} ≤ 16 MHz	26/f_{MCK}		—		—		ns
			4 MHz < f_{MCK} ≤ 8 MHz	16/f_{MCK}		16/f_{MCK}		—		ns
			f_{MCK} ≤ 4 MHz	10/f_{MCK}		10/f_{MCK}		10/f_{MCK}		ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	2.7 V ≤ V_{DD} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V		t_{KCY2}/2 - 18		t_{KCY2}/2 - 50		t_{KCY2}/2 - 50		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2		t_{KCY2}/2 - 50		t_{KCY2}/2 - 50		t_{KCY2}/2 - 50		ns
SIp setup time (to SCKp↑) Note 3	t_{SIK2}	2.7 V ≤ V_{DD} ≤ 3.6 V		1/f_{MCK} + 20		1/f_{MCK} + 30		1/f_{MCK} + 30		ns
		1.8 V ≤ V_{DD} < 3.3 V		1/f_{MCK} + 30		1/f_{MCK} + 30		1/f_{MCK} + 30		ns
SIp hold time (from SCKp↑) Note 4	t_{KSI2}			1/f_{MCK} + 31		1/f_{MCK} + 31		1/f_{MCK} + 31		ns
Delay time from SCKp↓ to SOp output Note 5	t_{KSO2}	2.7 V ≤ V_{DD} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V C_b = 30 pF, R_b = 2.7 kΩ			2/f_{MCK} + 214		2/f_{MCK} + 573		2/f_{MCK} + 573	ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2 C_b = 30 pF, R_b = 5.5 kΩ			2/f_{MCK} + 573		2/f_{MCK} + 573		2/f_{MCK} + 573	ns

Note 1. Transfer rate in the SNOOZE mode: MAX. 1 Mbps

Note 2. Use it with V_{DD} ≥ V_b.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 5. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution Select the TTL input buffer for the SIp pin and SCKp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(**Remarks** are listed on the next page.)

(3) I^2C fast mode plus

(T_A = -40 to +85°C, 2.7 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

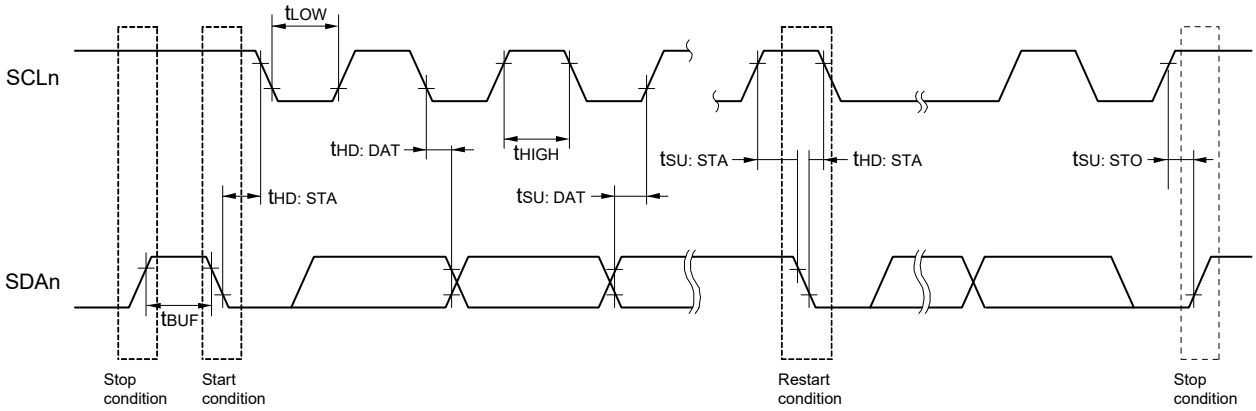
Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Fast mode plus: f_{CLK} ≥ 10 MHz	2.7 V ≤ V_{DD} ≤ 3.6 V	0	1000	—		—		kHz
Setup time of restart condition	$t_{SU: STA}$	2.7 V ≤ V_{DD} ≤ 3.6 V		0.26		—		—		μs
Hold time Note 1	$t_{HD: STA}$	2.7 V ≤ V_{DD} ≤ 3.6 V		0.26		—		—		μs
Hold time when SCLA0 = "L"	t_{LOW}	2.7 V ≤ V_{DD} ≤ 3.6 V		0.5		—		—		μs
Hold time when SCLA0 = "H"	t_{HIGH}	2.7 V ≤ V_{DD} ≤ 3.6 V		0.26		—		—		μs
Data setup time (reception)	$t_{SU: DAT}$	2.7 V ≤ V_{DD} ≤ 3.6 V		50		—		—		ns
Data hold time (transmission) Note 2	$t_{HD: DAT}$	2.7 V ≤ V_{DD} ≤ 3.6 V		0	0.45	—		—		μs
Setup time of stop condition	$t_{SU: STO}$	2.7 V ≤ V_{DD} ≤ 3.6 V		0.26		—		—		μs
Bus-free time	t_{BUF}	2.7 V ≤ V_{DD} ≤ 3.6 V		0.5		—		—		μs

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.

Note 2. The maximum value (MAX.) of $t_{HD: DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.
Fast mode plus: C_b = 120 pF, R_b = 1.1 kΩ

IICA serial transfer timing



(3) BC option standard

(T_A = -40 to +85°C, 4.35 V ≤ UV_{BUS} ≤ 5.25 V, 2.4 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V, HS (High-speed main) mode only)

Parameter			Symbol	Conditions	MIN.	TYP.	MAX.	Unit
UDP/UDM input reference voltage (UV_{BUS} divider ratio) (Function)	VDSELi [3: 0] (i = 0, 1)	0000	V_{DDET0}		27	32	37	%UVBUS
		0001	V_{DDET1}		29	34	39	%UVBUS
		0010	V_{DDET2}		32	37	42	%UVBUS
		0011	V_{DDET3}		35	40	45	%UVBUS
		0100	V_{DDET4}		38	43	48	%UVBUS
		0101	V_{DDET5}		41	46	51	%UVBUS
		0110	V_{DDET6}		44	49	54	%UVBUS
		0111	V_{DDET7}		47	52	57	%UVBUS
		1000	V_{DDET8}		51	56	61	%UVBUS
		1001	V_{DDET9}		55	60	65	%UVBUS
		1010	V_{DDET10}		59	64	69	%UVBUS
		1011	V_{DDET11}		63	68	73	%UVBUS
		1100	V_{DDET12}		67	72	73	%UVBUS
		1101	V_{DDET13}		71	76	81	%UVBUS
		1110	V_{DDET14}		75	80	85	%UVBUS
		1111	V_{DDET15}		79	84	89	%UVBUS

(5) When reference voltage (+) = AV_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (-) = AV_{SS} (ADREFM = 0), conversion target: ANI16 to ANI21, internal reference voltage, temperature sensor output voltage

(T_A = -40 to +85°C, 1.6 V ≤ V_{DD} ≤ 3.6 V, 1.6 V ≤ AV_{DD} = V_{DD} ≤ 3.6 V, V_{SS} = 0 V, AV_{SS} = 0 V, Reference voltage (+) = AV_{DD}, Reference voltage (-) = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES		2.4 V ≤ AV_{DD} ≤ 3.6 V	8		12	bit
			1.8 V ≤ AV_{DD} ≤ 3.6 V	8		10 Note 1	
			1.6 V ≤ AV_{DD} ≤ 3.6 V	8 Note 2			
Overall error Note 3	AINL	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±8.5	LSB
		10-bit resolution	1.8 V ≤ AV_{DD} ≤ 3.6 V			±6.0	
		8-bit resolution	1.6 V ≤ AV_{DD} ≤ 3.6 V			±3.5	
Conversion time	t_{CONV}	ADTYP = 0, 12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V	4.125			µs
		ADTYP = 0, 10-bit resolution Note 1	1.8 V ≤ AV_{DD} ≤ 3.6 V	9.5			
		ADTYP = 0, 8-bit resolution Note 2	1.6 V ≤ AV_{DD} ≤ 3.6 V	57.5			
		ADTYP = 1, 8-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V	3.3125			
			1.8 V ≤ AV_{DD} ≤ 3.6 V	7.875			
			1.6 V ≤ AV_{DD} ≤ 3.6 V	54.25			
Zero-scale error Note 3	E_{ZS}	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±8.0	LSB
		10-bit resolution	1.8 V ≤ AV_{DD} ≤ 3.6 V			±5.5	
		8-bit resolution	1.6 V ≤ AV_{DD} ≤ 3.6 V			±3.0	
Full-scale error Note 3	E_{FS}	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±8.0	LSB
		10-bit resolution	1.8 V ≤ AV_{DD} ≤ 3.6 V			±5.5	
		8-bit resolution	1.6 V ≤ AV_{DD} ≤ 3.6 V			±3.0	
Integral linearity error Note 3	ILE	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±3.5	LSB
		10-bit resolution	1.8 V ≤ AV_{DD} ≤ 3.6 V			±2.5	
		8-bit resolution	1.6 V ≤ AV_{DD} ≤ 3.6 V			±1.5	
Differential linearity error Note 3	DLE	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±2.5	LSB
		10-bit resolution	1.8 V ≤ AV_{DD} ≤ 3.6 V			±2.5	
		8-bit resolution	1.6 V ≤ AV_{DD} ≤ 3.6 V			±2.0	
Analog input voltage	V_{AIN}			0		AV_{DD}	V
		Internal reference voltage (2.4 V ≤ V_{DD} ≤ 3.6 V, HS (high-speed main) mode)		V_{BGR} Note 4			
		Temperature sensor output voltage (2.4 V ≤ V_{DD} ≤ 3.6 V, HS (high-speed main) mode)		V_{TMP25} Note 4			

Note 1. Cannot be used for lower 2 bits of ADCR register

Note 2. Cannot be used for lower 4 bits of ADCR register

Note 3. Excludes quantization error (±1/2 LSB).

Note 4. Refer to **2.6.2 Temperature sensor, internal reference voltage output characteristics**.

Caution Always use AV_{DD} pin with the same potential as the V_{DD} pin.

LVD Detection Voltage of Interrupt & Reset Mode

(T_A = -40 to +85°C, $V_{PDR} \le V_{DD} \le 3.6$ V, V_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Interrupt and reset mode	V_{LVDA0}	V_{POC0}, V_{POC1}, V_{POC2} = 0, 0, 0, falling reset voltage: 1.6 V			1.60	1.63	1.66	V
	V_{LVDA1}	LVIS0, LVIS1 = 1, 0		Rising release reset voltage	1.74	1.77	1.81	V
				Falling interrupt voltage	1.70	1.73	1.77	V
	V_{LVDA2}	LVIS0, LVIS1 = 0, 1		Rising release reset voltage	1.84	1.88	1.91	V
				Falling interrupt voltage	1.80	1.84	1.87	V
	V_{LVDA3}	LVIS0, LVIS1 = 0, 0		Rising release reset voltage	2.86	2.92	2.97	V
				Falling interrupt voltage	2.80	2.86	2.91	V
	V_{LVDB0}	V_{POC0}, V_{POC1}, V_{POC2} = 0, 0, 1, falling reset voltage: 1.8 V			1.80	1.84	1.87	V
	V_{LVDB1}	LVIS0, LVIS1 = 1, 0		Rising release reset voltage	1.94	1.98	2.02	V
				Falling interrupt voltage	1.90	1.94	1.98	V
	V_{LVDB2}	LVIS0, LVIS1 = 0, 1		Rising release reset voltage	2.05	2.09	2.13	V
				Falling interrupt voltage	2.00	2.04	2.08	V
	V_{LVDB3}	LVIS0, LVIS1 = 0, 0		Rising release reset voltage	3.07	3.13	3.19	V
				Falling interrupt voltage	3.00	3.06	3.12	V
	V_{LVDC0}	V_{POC0}, V_{POC1}, V_{POC2} = 0, 1, 0, falling reset voltage: 2.4 V			2.40	2.45	2.50	V
	V_{LVDC1}	LVIS0, LVIS1 = 1, 0		Rising release reset voltage	2.56	2.61	2.66	V
				Falling interrupt voltage	2.50	2.55	2.60	V
	V_{LVDC2}	LVIS0, LVIS1 = 0, 1		Rising release reset voltage	2.66	2.71	2.76	V
				Falling interrupt voltage	2.60	2.65	2.70	V
	V_{LVDD0}	V_{POC0}, V_{POC1}, V_{POC2} = 0, 1, 1, falling reset voltage: 2.7 V			2.70	2.75	2.81	V
	V_{LVDD1}	LVIS0, LVIS1 = 1, 0		Rising release reset voltage	2.86	2.92	2.97	V
				Falling interrupt voltage	2.80	2.86	2.91	V
	V_{LVDD2}	LVIS0, LVIS1 = 0, 1		Rising release reset voltage	2.96	3.02	3.08	V
				Falling interrupt voltage	2.90	2.96	3.02	V

2.7 Power supply voltage rising slope characteristics

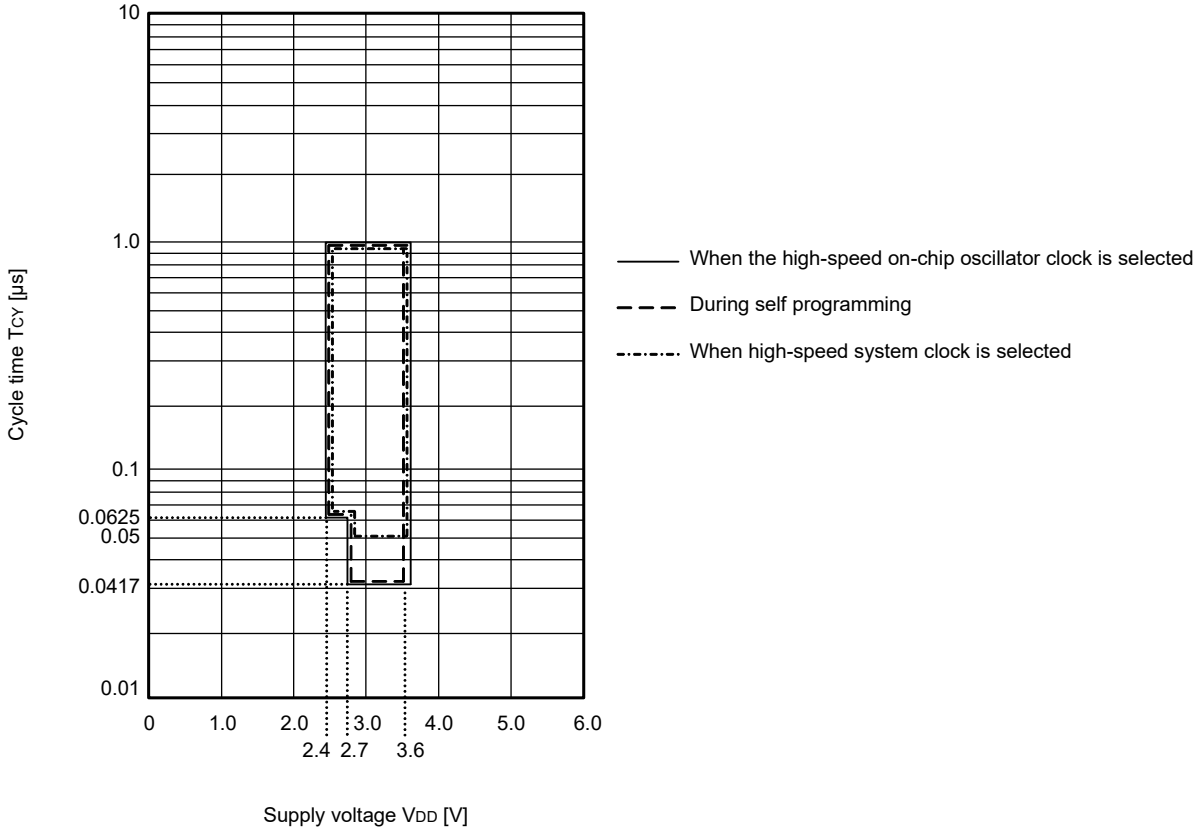
(T_A = -40 to +85°C, V_{SS} = 0 V)

Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	SV_{DD}			54	V/ms

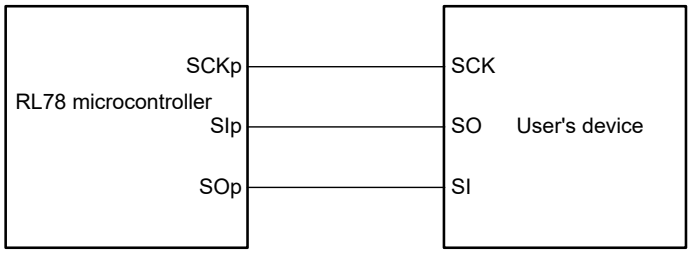
Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until V_{DD} reaches the operating voltage range shown in 2.4 AC Characteristics.

Minimum Instruction Execution Time during Main System Clock Operation

TCY vs VDD (HS (high-speed main) mode)



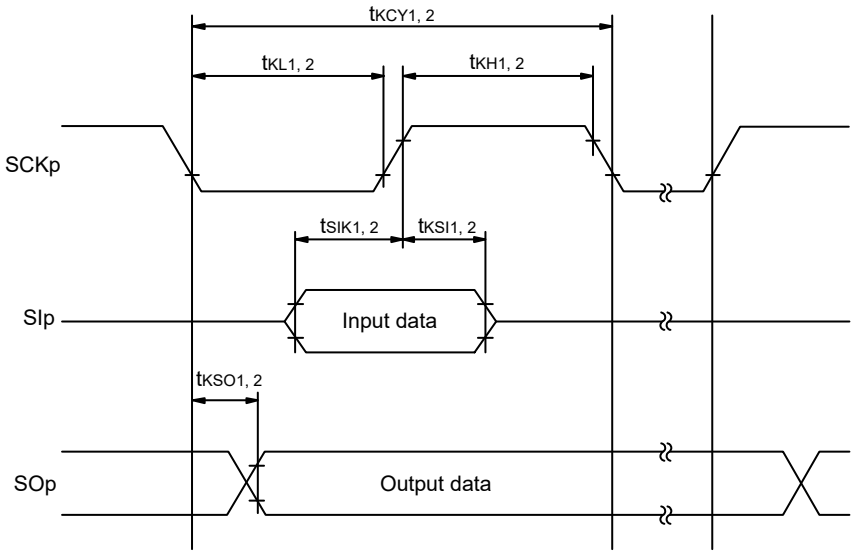
CSI mode connection diagram (during communication at same potential)



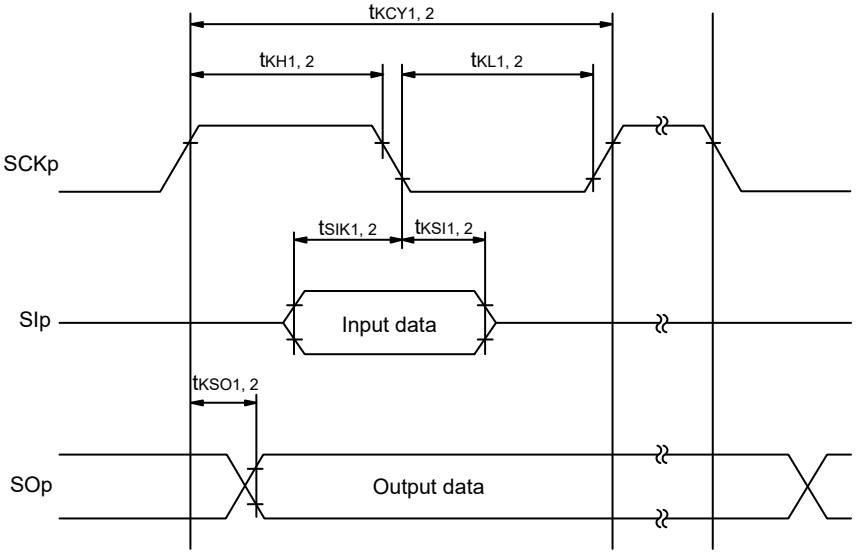
Remark 1. p: CSI number (p = 00, 10, 20, 30)

Remark 2. m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark 1. p: CSI number (p = 00, 10, 20, 30)
Remark 2. m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

(5) Communication at different potential (1.8 V, 2.5V) (UART mode)

(T_A = -40 to +105°C, 2.4 ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V) (2/2)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
Transfer rate Note 2		Transmission	2.7 V ≤ V_{DD} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V		Note 1	bps
			Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 2.7 kΩ, V_b = 2.3 V		1.2 Note 2	Mbps
			1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V		Notes 3, 4	bps
			Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 5.5 kΩ, V_b = 1.6 V		0.43 Note 5	Mbps

Note 1. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 2.7 V ≤ V_{DD} < 3.6 V and 2.3 V ≤ V_b ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

Note 2. This value as an example is calculated when the conditions described in the “Conditions” column are met.
Refer to Note 1 above to calculate the maximum transfer rate under conditions of the customer.

Note 3. Use it with $V_{DD} \geq V_b$.

Note 4. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 2.4 V ≤ V_{DD} < 3.3 V and 1.6 V ≤ V_b ≤ 2.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

Note 5. This value as an example is calculated when the conditions described in the “Conditions” column are met.
Refer to Note 4 above to calculate the maximum transfer rate under conditions of the customer.

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

3.5.3 USB

(1) Electrical specifications

(T_A = -40 to +105°C, 2.4 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
UREGC	UREGC output voltage characteristic	UREGC	UVBUS = 4.0 to 5.5 V, PXXCON = VDDUSBE = 1	3.0	3.3	3.6	V
UVBUS	UVBUS input voltage characteristic	UVBUS	Function	4.35 (4.02 Note)	5.00	5.25	V

Note Value of instantaneous voltage

(T_A = -40 to +105°C, 4.35 V ≤ UVBUS ≤ 5.25 V, 2.4 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

Parameter			Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input characteristic (FS/LS receiver)	Input voltage		VIH		2.0			V
			VIL				0.8	V
	Difference input sensitivity		VDI	| UDP voltage - UDM voltage |	0.2			V
	Difference common mode range		VCM		0.8		2.5	V
Output characteristic (FS driver)	Output voltage		VOH	IOH = -200 μA	2.8		3.6	V
			VOL	IOL = 2 mA	0		0.3	V
	Transition time	Rising	tFR	Rising: From 10% to 90% of amplitude, Falling: From 90% to 10% of amplitude, CL = 50 pF	4		20	ns
		Falling	tFF		4		20	ns
	Matching (TFR/TFF)		VFRFM		90		111.1	%
	Crossover voltage		VFCRS		1.3		2.0	V
	Output Impedance		ZDRV		28		44	Ω
Output characteristic (LS driver)	Output voltage		VOH		2.8		3.6	V
			VOL		0		0.3	V
	Transition time	Rising	tLR	Rising: From 10% to 90% of amplitude, Falling: From 90% to 10% of amplitude, CL = 250 pF to 750 pF The UDP and UDM pins are individually pulled down via 15 kΩ	75		300	ns
		Falling	tLF		75		300	ns
	Matching (TFR/TFF) Note		VLTFM		80		125	%
	Crossover voltage Note		VLCRS		1.3		2.0	V
Pull-up, Pull-down	Pull-down resistor		RPD		14.25		24.80	kΩ
	Pull-up resistor	Idle	RPUI		0.9		1.575	kΩ
		Reception	RPUA		1.425		3.09	kΩ
UVBUS	UVBUS pull-down resistor		RVBUS	UVBUS voltage = 5.5 V		1000		kΩ
	UVBUS input voltage		VIH		3.20			V
			VIL				0.8	V

Note Excludes the first signal transition from the idle state.

LVD Detection Voltage of Interrupt & Reset Mode

(T_A = -40 to +105°C, $V_{PDR} \leq V_{DD} \leq$ 3.6 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Interrupt and reset mode	V_{LVDD0}	V_{POC0}, V_{POC1}, V_{POC2} = 0, 1, 1, falling reset voltage: 2.7 V			2.64	2.75	2.86	V
	V_{LVDD1}		LVIS0, LVIS1 = 1, 0	Rising release reset voltage	2.81	2.92	3.03	V
				Falling interrupt voltage	2.75	2.86	2.97	V
	V_{LVDD2}		LVIS0, LVIS1 = 0, 1	Rising release reset voltage	2.90	3.02	3.14	V
				Falling interrupt voltage	2.85	2.96	3.07	V

3.7 Power supply voltage rising slope characteristics

(T_A = -40 to +105°C, V_{SS} = 0 V)

Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	SV_{DD}			54	V/ms

Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until V_{DD} reaches the operating voltage range shown in 3.4 AC Characteristics.

3.8.2 Internal voltage boosting method

(1) 1/3 bias method

(T_A = -40 to +105°C, 2.4 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
LCD output voltage variation range	V_{L1}	C1 to C4 Note 1 = 0.47 μF Note 2	VLCD = 04H	0.90	1.00	1.08	V
			VLCD = 05H	0.95	1.05	1.13	V
			VLCD = 06H	1.00	1.10	1.18	V
			VLCD = 07H	1.05	1.15	1.23	V
			VLCD = 08H	1.10	1.20	1.28	V
			VLCD = 09H	1.15	1.25	1.33	V
			VLCD = 0AH	1.20	1.30	1.38	V
			VLCD = 0BH	1.25	1.35	1.43	V
			VLCD = 0CH	1.30	1.40	1.48	V
			VLCD = 0DH	1.35	1.45	1.53	V
			VLCD = 0EH	1.40	1.50	1.58	V
			VLCD = 0FH	1.45	1.55	1.63	V
			VLCD = 10H	1.50	1.60	1.68	V
			VLCD = 11H	1.55	1.65	1.73	V
			VLCD = 12H	1.60	1.70	1.78	V
			VLCD = 13H	1.65	1.75	1.83	V
Doubler output voltage	V_{L2}	C1 to C4 Note 1 = 0.47 μF		2 V_{L1} - 0.1	2 V_{L1}	2 V_{L1}	V
Tripler output voltage	V_{L3}	C1 to C4 Note 1 = 0.47 μF		3 V_{L1} - 0.15	3 V_{L1}	3 V_{L1}	V
Reference voltage setup time Note 2	t_{VWAIT1}			5			ms
Voltage boost wait time Note 3	t_{VWAIT2}	C1 to C4 Note 1 = 0.47μF		500			ms

Note 1. This is a capacitor that is connected between voltage pins used to drive the LCD.
C1: A capacitor connected between CAPH and CAPL
C2: A capacitor connected between V_{L1} and GND
C3: A capacitor connected between V_{L2} and GND
C4: A capacitor connected between V_{L4} and GND
C1 = C2 = C3 = C4 = 0.47 μF±30%

Note 2. This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected (by setting the MDSET1 and MDSET0 bits of the LCDM0 register to 01B) if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).

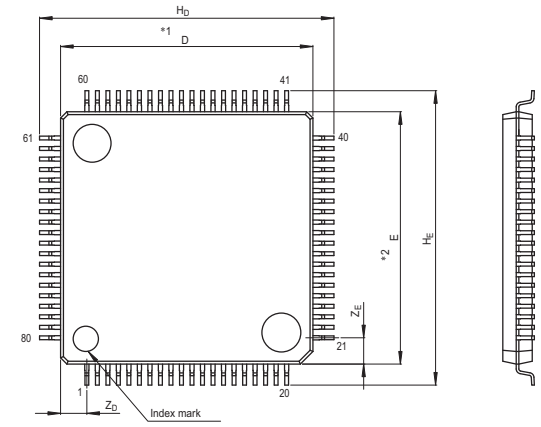
Note 3. This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

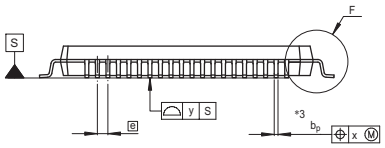
4. PACKAGE DRAWINGS

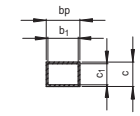
4.1 80-pin products

R5F110MEAFB, R5F110MFAFB, R5F110MGAFB, R5F110MHAFB, R5F110MJAFB
R5F111MEAFB, R5F111MFAFB, R5F111MGAFB, R5F111MHAFB, R5F111MJAFB
R5F110MEGFB, R5F110MFGFB, R5F110MGGFB, R5F110MHGFB, R5F110MJGFB
R5F111MEGFB, R5F111MFGFB, R5F111MGGFB, R5F111MHGFB, R5F111MJGFB

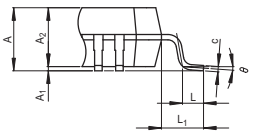
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP80-12x12-0.50	PLQP0080KB-A	80P6Q-A	0.5g







Terminal cross section



Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	11.9	12.0	12.1
E	11.9	12.0	12.1
A_2	—	1.4	—
H_D	13.8	14.0	14.2
H_E	13.8	14.0	14.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	10°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.3	0.5	0.7
L_1	—	1.0	—

REVISION HISTORY	RL78/L1C Datasheet

Rev.	Date	Description	
		Page	Summary
0.01	Oct 15, 2012	—	First Edition issued
1.00	Nov 18, 2013	1, 2	Modification of 1.1 Features
		3, 4	Modification of 1.2 Ordering Information
		5 to 8	Modification of package type in 1.3 Pin Configuration (Top View)
		14 to 17	Modification of vectored interrupt sources in 1.6 Outline of Functions
		14 to 17	Modification of operating ambient temperature in 1.6 Outline of Functions
		19 to 21	Modification of description in tables in 2.1 Absolute Maximum Ratings
		22, 23	Modification of description in 2.2 Oscillator Characteristics
		25	Modification of low-level output current in 2.3.1 Pin characteristics
		26	Modification of error of high-level input voltage conditions in 2.3.1 Pin characteristics
		26	Modification of error of low-level input voltage conditions in 2.3.1 Pin characteristics
		27	Modification of low-level output voltage in 2.3.1 Pin characteristics
		28	Modification of error of internal pull-up resistor conditions in 2.3.1 Pin characteristics
		29 to 34	Modification of 2.3.2 Supply current characteristics
		35, 36	Modification of 2.4 AC Characteristics
		37, 38	Addition of minimum instruction execution time during main system clock operation
		41 to 63	Addition of LS mode and LV mode characteristics in 2.5.1 Serial array unit
		64 to 66	Addition of LS mode and LV mode characteristics in 2.5.2 Serial interface IICA
		67, 68	Modification of conditions in 2.5.3 USB
		69	Addition of (3) BC option standard in 2.5.3 USB
		70 to 75	Addition of characteristics about conversion of internal reference voltage and temperature sensor in 2.6.1 A/D converter characteristics
		76	Addition of characteristic in 2.6.4 Comparator
		76	Deletion of detection delay in 2.6.5 POR circuit characteristics
		78	Modification of 2.7 Power supply voltage rising slope characteristics
		79 to 82	Modification of 2.8 LCD Characteristics
		83	Modification of 2.9 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics
		83	Modification of 2.10 Flash Memory Programming Characteristics
		84	Addition of 2.12 Timing Specs for Switching Modes
		85 to 144	Addition of 3. ELECTRICAL SPECIFICATIONS (G: T_A = -40 to +105°C)
2.00	Feb 21, 2014	All	Addition of 85-pin product information
		All	Modification from 80-pin to 80/85-pin
		All	Modification from x = M, P to x = M, N, P
		All	Modification from high-accuracy real-time clock to real-time clock 2
		All	Modification from RTC to RTC2
		1	Modification of 1.1 Features
		3	Modification of 1.2 Ordering Information

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