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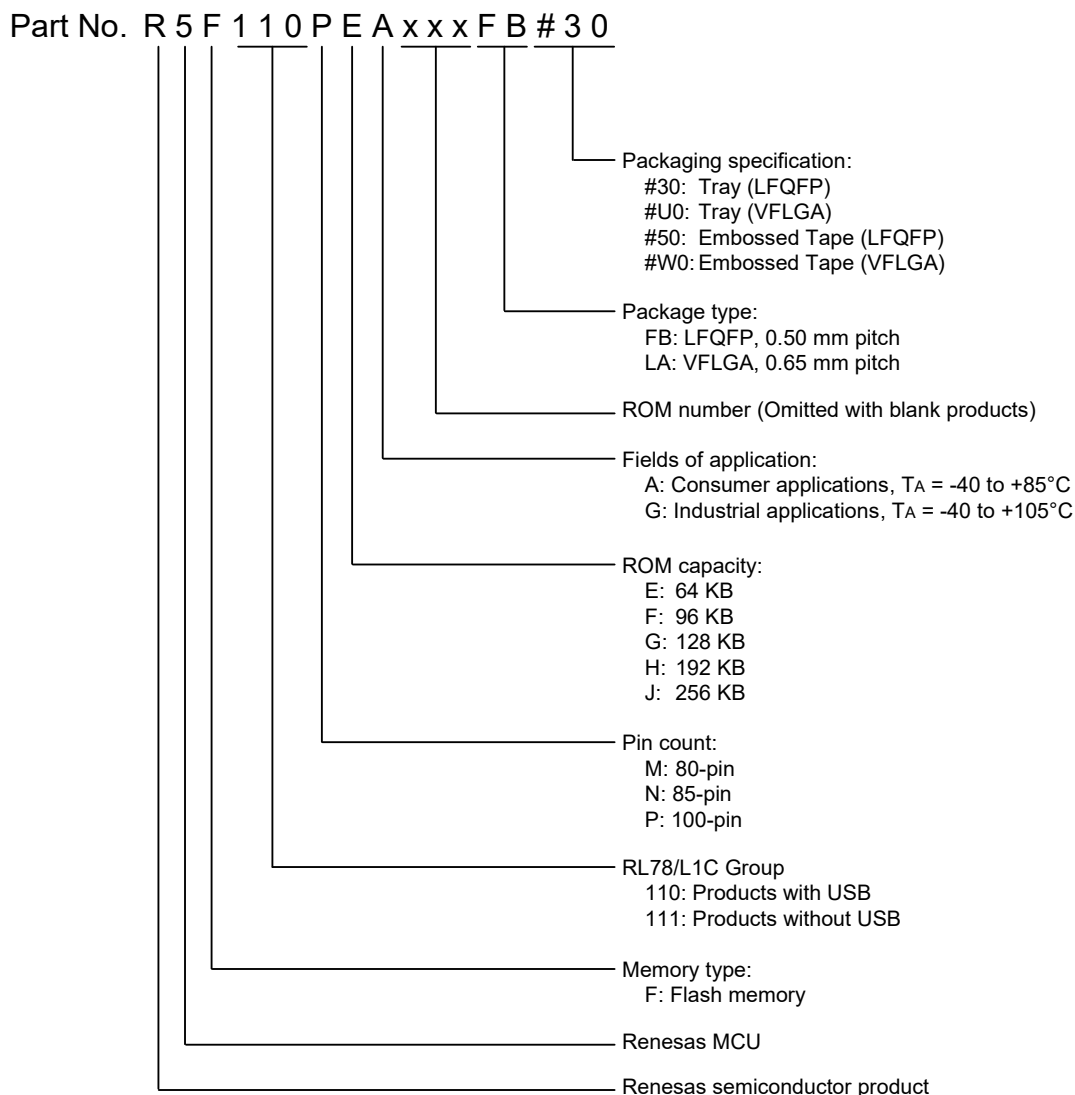
"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I ² C, LINbus, UART/USART
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	55
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 11x8/12b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f111meafb-30

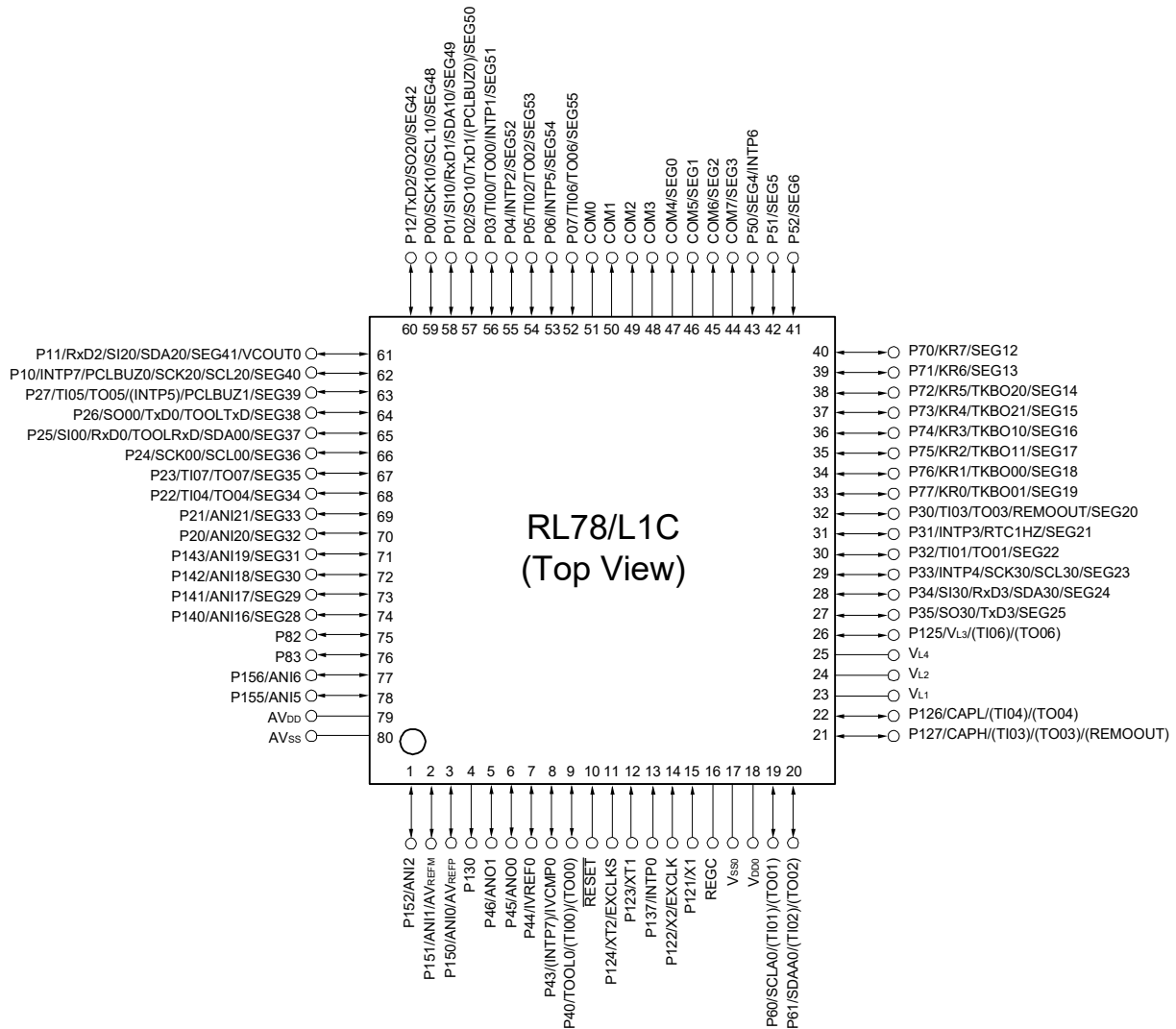
Figure 1 - 1 Part Number, Memory Size, and Package of RL78/L1C



Caution Orderable part numbers are current as of when this manual was published.
Please make sure to refer to the relevant product page on the Renesas website for the latest part numbers.

1.3.2 80-pin products (without USB)

- 80-pin plastic LQFP (fine pitch) (12 × 12 mm, 0.5 mm pitch)



Caution Connect the REGC pin to V_{SS} pin via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.4 Pin Identification

ANI0 to ANI6,	: Analog Input	SCL00, SCL10, SCL20, SCL30	: Serial Clock Output
ANI16 to ANI21		SDAA0, SDA00, SDA10,	: Serial Data Input/Output
ANO0, ANO1	: Analog Output	SDA20, SDA30	
AVDD	: Analog Power Supply	SEG0 to SEG55	: LCD Segment Output
AVREFM	: Analog Reference Voltage Minus	SI00, SI10, SI20, SI30	: Serial Data Input
AVREFP	: Analog Reference Voltage Plus	SO00, SO10, SO20, SO30	: Serial Data Output
AVss	: Analog Ground	TI00 to TI07	: Timer Input
CAPH, CAPL	: Capacitor for LCD	TO00 to TO07	: Timer Output
COM0 to COM7	: LCD Common Output	TKBO00, TKBO01, TKBO10,	
EXCLK	: External Clock Input (Main System Clock)	TKBO11, TKBO20, TKBO21	
EXCLKS	: External Clock Input (Subsystem Clock)	TOOL0	: Data Input/Output for Tool
INTP0 to INTP7	: External Interrupt Input	TOOLRxD, TOOLTxD	: Data Input/Output for External Device
IVCMP0, IVCMP1	: Comparator Input	UDM, UDP	: USB Input/Output
IVREF0, IVREF1	: Comparator Reference Input	UREGC	: USB Regulator Capacitance
KR0 to KR7	: Key Return	UVBUS	: USB Input/USB Power Supply
P00 to P07	: Port 0	TxD0 to TxD3	: Transmit Data
P10 to P17	: Port 1	VCOUT0, VCOUT1	: Comparator Output
P20 to P27	: Port 2	VDD0, VDD1	: Power Supply
P30 to P37	: Port 3	VL1 to VL4	: LCD Power Supply
P40 to P46	: Port 4	VSS0, VSS1	: Ground
P50 to P57	: Port 5	X1, X2	: Crystal Oscillator (Main System Clock)
P60 to P62	: Port 6	XT1, XT2	: Crystal Oscillator (Subsystem Clock)
P70 to P77	: Port 7		
P80 to P83	: Port 8		
P121 to P127	: Port 12		
P130, P137	: Port 13		
P140 to P143	: Port 14		
P150 to P156	: Port 15		
PCLBUZ0, PCLBUZ1	: Programmable Clock Output/ Buzzer Output		
REGC	: Regulator Capacitance		
REMOOUT	: Remote Control Output		
$\overline{\text{RESET}}$: Reset		
RTC1HZ	: Real-time Clock Correction Clock (1 Hz) Output		
RxD0 to RxD3	: Receive Data		
SCK00, SCK10, SCK20, SCK30	: Serial Clock Input/Output		
SCLA0	: Serial Clock Input/Output		

1.6 Outline of Functions

[80/85-pin, 100-pin products (with USB)]

(1/2)

Item		80/85-pin	100-pin
		R5F110Mx/R5F110Nx (x = E to H, J)	R5F110Px (x = E to H, J)
Code flash memory (KB)		64 to 256	64 to 256
Data flash memory (KB)		8	8
RAM (KB)		8 to 16 ^{Note 1}	8 to 16 ^{Note 1}
Memory space		1 MB	
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) 1 to 20 MHz: V _{DD} = 2.7 to 3.6 V, 1 to 8 MHz: V _{DD} = 1.8 to 2.7 V, 1 to 4 MHz: V _{DD} = 1.6 to 1.8 V	
	High-speed on-chip oscillator clock	HS (high-speed main) operation mode: 1 to 24 MHz (V _{DD} = 2.7 to 3.6 V), HS (high-speed main) operation mode: 1 to 16 MHz (V _{DD} = 2.4 to 3.6 V), LS (low-speed main) operation mode: 1 to 8 MHz (V _{DD} = 1.8 to 3.6 V), LV (low-voltage main) operation mode: 1 to 4 MHz (V _{DD} = 1.6 to 3.6 V)	
	PLL clock	6, 12, 24 MHz ^{Note 2} : V _{DD} = 2.4 to 3.6 V	
Subsystem clock		XT1 (crystal) oscillation, external subsystem clock input (EXCLKS) 32.768 kHz (TYP.): V _{DD} = 1.6 to 3.6 V	
Low-speed on-chip oscillator clock		15 kHz (TYP.): V _{DD} = 1.6 to 3.6 V	
General-purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)	
Minimum instruction execution time		0.04167 μs (High-speed on-chip oscillator clock: f _{HOCO} = f _{IH} = 24 MHz operation)	
		0.04167 μs (PLL clock: f _{PLL} = 48 MHz/f _{IH} = 24 MHz ^{Note 2} operation)	
		0.05 μs (High-speed system clock: f _{MX} = 20 MHz operation)	
		30.5 μs (Subsystem clock: f _{SUB} = 32.768 kHz operation)	
Instruction set		<ul style="list-style-type: none"> • Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits, 16 bits × 16 bits), Division (16 bits ÷ 16 bits, 32 bits ÷ 32 bits) • Multiplication and Accumulation (16 bits × 16 bits + 32 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc. 	
I/O port	Total	59	77
	CMOS I/O	51	69
	CMOS input	5	5
	CMOS output	1	1
	N-ch open-drain I/O (6 V tolerance)	2	2
Timer	16-bit timer TAU	8 channels (with 1 channel remote control output function) (Timer outputs: 8, PWM outputs: 7 ^{Note 3})	
	16-bit timer KB2	3 channels (PWM outputs: 6)	
	Watchdog timer	1 channel	
	12-bit interval timer	1 channel	
	Real-time clock 2	1 channel	
	RTC output	1 1 Hz (subsystem clock: f _{SUB} = 32.768 kHz)	

Note 1. In the case of the 16 KB, this is about 15 KB when the self-programming function and data flash function are used (For details, see **CHAPTER 3** in the RL78/L1C User's Manual).

Note 2. In the PLL clock 48 MHz operation, the system clock is 2/4/8 dividing ratio.

Note 3. The number of outputs varies, depending on the setting of channels in use and the number of the master.

2.2 Oscillator Characteristics

2.2.1 X1 and XT1 oscillator characteristics

(TA = -40 to +85°C, 1.6 V ≤ VDD ≤ 3.6 V, VSS = 0 V)

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (fx) Note	Ceramic resonator/crystal resonator	2.7 V ≤ VDD ≤ 3.6 V	1.0		20.0	MHz
		2.4 V ≤ VDD < 2.7 V	1.0		16.0	
		1.8 V ≤ VDD < 2.4 V	1.0		8.0	
		1.6 V ≤ VDD < 1.8 V	1.0		4.0	
XT1 clock oscillation frequency (fxT) Note	Crystal resonator		32	32.768	35	kHz

Note Indicates only permissible oscillator frequency ranges. Refer to **AC Characteristics** for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

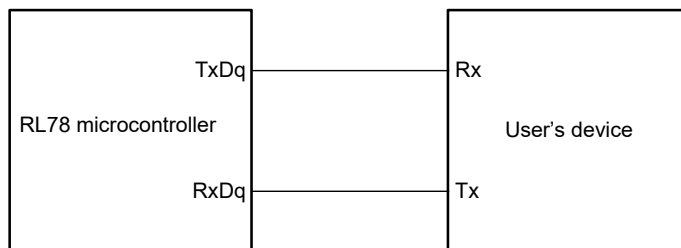
Remark When using the X1 and XT1 oscillator, refer to **5.4 System Clock Oscillator** in the RL78/L1C User's Manual.

(TA = -40 to +85°C, 1.6 V ≤ AVDD = VDD ≤ 3.6 V, VSS = 0 V)

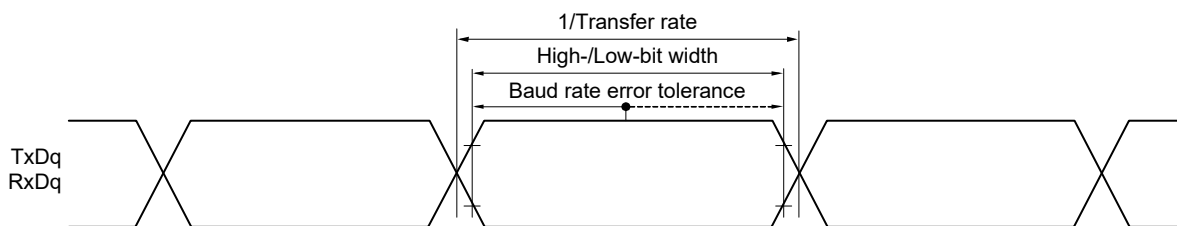
Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit		
Input leakage current, high	LIH1	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P46, P50 to P57, P60, P61, P70 to P77, P80 to P83, P125 to P127, P137, P140 to P143, $\overline{\text{RESET}}$	Vi = VDD		1	μA		
	LIH2	P20, P21, P140 to P143	Vi = VDD		1	μA		
	LIH3	P121 to P124 (X1, X2, EXCLK, XT1, XT2, EXCLKS)	Vi = VDD	In input port or external clock input		1	μA	
				In resonator connection		10	μA	
LIH4	P150 to P156	Vi = AVDD		1	μA			
Input leakage current, low	LIIL1	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P46, P50 to P57, P60, P61, P70 to P77, P80 to P83, P125 to P127, P137, P140 to P143, $\overline{\text{RESET}}$	Vi = VSS		-1	μA		
	LIIL2	P20, P21, P140 to P143	Vi = VSS		-1	μA		
	LIIL3	P121 to P124 (X1, X2, EXCLK, XT1, XT2, EXCLKS)	Vi = VSS	In input port or external clock input		-1	μA	
				In resonator connection		-10	μA	
LIIL4	P150 to P156	Vi = AVSS		-1	μA			
On-chip pull-up resistance	RU1	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P50 to P57, P70 to P77, P140 to P143, P125 to P127	Vi = VSS	2.4 V ≤ VDD ≤ 3.6 V	10	20	100	kΩ
				1.6 V ≤ VDD ≤ 2.4 V	10	30	100	
	RU2	P40 to P46, P80 to P83	Vi = VSS		10	20	100	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)



Remark 1. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0 to 3)

Remark 2. fMCK: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only)**(TA = -40 to +85°C, 2.7 V ≤ VDD ≤ 3.6 V, VSS = 0 V)**

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t _{KCY1}	t _{KCY1} ≥ f _{CLK/2}	2.7 V ≤ V _{DD} ≤ 3.6 V	167		250		500		ns
SCKp high-/low-level width	t _{KL1}	2.7 V ≤ V _{DD} ≤ 3.6 V		t _{KCY1/2} - 10		t _{KCY1/2} - 50		t _{KCY1/2} - 50		ns
Slp setup time (to SCKp↑) ^{Note 1}	t _{SIK1}	2.7 V ≤ V _{DD} ≤ 3.6 V		33		110		110		ns
Slp hold time (from SCKp↑) ^{Note 2}	t _{SI1}	2.7 V ≤ V _{DD} ≤ 3.6 V		10		10		10		ns
Delay time from SCKp↓ to SOp output ^{Note 3}	t _{KSO1}	C = 20 pF ^{Note 4}			10		10		10	ns

Note 1. When DAP_{mn} = 0 and CKP_{mn} = 0, or DAP_{mn} = 1 and CKP_{mn} = 1. The Slp setup time becomes “to SCKp↓” when DAP_{mn} = 0 and CKP_{mn} = 1, or DAP_{mn} = 1 and CKP_{mn} = 0.

Note 2. When DAP_{mn} = 0 and CKP_{mn} = 0, or DAP_{mn} = 1 and CKP_{mn} = 1. The Slp hold time becomes “from SCKp↓” when DAP_{mn} = 0 and CKP_{mn} = 1, or DAP_{mn} = 1 and CKP_{mn} = 0.

Note 3. When DAP_{mn} = 0 and CKP_{mn} = 0, or DAP_{mn} = 1 and CKP_{mn} = 1. The delay time to SOp output becomes “from SCKp↑” when DAP_{mn} = 0 and CKP_{mn} = 1, or DAP_{mn} = 1 and CKP_{mn} = 0.

Note 4. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM number (g = 2)

Remark 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKS_{mn} bit of serial mode register mn (SMR_{mn}). m: Unit number, n: Channel number (mn = 00))

(8) Communication at different potential (1.8 V, 2.5 V) (CSI mode) (master mode, SCKp... internal clock output)**(TA = -40 to +85°C, 1.8 V ≤ VDD ≤ 3.6 V, VSS = 0 V)****(2/2)**

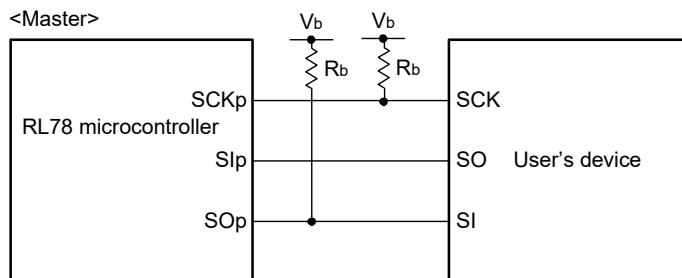
Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Slp setup time (to SCKp↑) Note 1	tSIK1	2.7 V ≤ VDD ≤ 3.6 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	177		479		479		ns
		1.8 V ≤ VDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 3, Cb = 30 pF, Rb = 5.5 kΩ	479		479		479		ns
Slp hold time (from SCKp↑) Note 1	tKS11	2.7 V ≤ VDD ≤ 3.6 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	19		19		19		ns
		1.8 V ≤ VDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 3, Cb = 30 pF, Rb = 5.5 kΩ	19		19		19		ns
Delay time from SCKp↓ to SOp output Note 1	tKSO1	2.7 V ≤ VDD ≤ 3.6 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ		195		195		195	ns
		1.8 V ≤ VDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 3, Cb = 30 pF, Rb = 5.5 kΩ		483		483		483	ns
Slp setup time (to SCKp↓) Note 2	tSIK1	2.7 V ≤ VDD ≤ 3.6 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	44		110		110		ns
		1.8 V ≤ VDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 3, Cb = 30 pF, Rb = 5.5 kΩ	110		110		110		ns
Slp hold time (from SCKp↓) Note 2	tKS11	2.7 V ≤ VDD ≤ 3.6 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	19		19		19		ns
		1.8 V ≤ VDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 3, Cb = 30 pF, Rb = 5.5 kΩ	19		19		19		ns
Delay time from SCKp↑ to SOp output Note 2	tKSO1	2.7 V ≤ VDD ≤ 3.6 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ		25		25		25	ns
		1.8 V ≤ VDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 3, Cb = 30 pF, Rb = 5.5 kΩ		25		25		25	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.**Note 2.** When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.**Note 3.** Use it with VDD ≥ Vb.

Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (VDD tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

CSI mode connection diagram (during communication at different potential)



- Remark 1.** Rb[Ω]: Communication line (SCKp, SOp) pull-up resistance, Cb[F]: Communication line (SCKp, SOp) load capacitance, Vb[V]: Communication line voltage
- Remark 2.** p: CSI number (p = 00, 10, 20, 30), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0 to 3)
- Remark 3.** fMCK: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))

(3) BC option standard**(TA = -40 to +85°C, 4.35 V ≤ UVBus ≤ 5.25 V, 2.4 V ≤ VDD ≤ 3.6 V, VSS = 0 V, HS (High-speed main) mode only)**

Parameter			Symbol	Conditions	MIN.	TYP.	MAX.	Unit
UDP/UDM input reference voltage (UVBus divider ratio) (Function)	VDSELi [3: 0] (i = 0, 1)	0000	VDDDET0		27	32	37	%UVBUS
		0001	VDDDET1		29	34	39	%UVBUS
		0010	VDDDET2		32	37	42	%UVBUS
		0011	VDDDET3		35	40	45	%UVBUS
		0100	VDDDET4		38	43	48	%UVBUS
		0101	VDDDET5		41	46	51	%UVBUS
		0110	VDDDET6		44	49	54	%UVBUS
		0111	VDDDET7		47	52	57	%UVBUS
		1000	VDDDET8		51	56	61	%UVBUS
		1001	VDDDET9		55	60	65	%UVBUS
		1010	VDDDET10		59	64	69	%UVBUS
		1011	VDDDET11		63	68	73	%UVBUS
		1100	VDDDET12		67	72	73	%UVBUS
		1101	VDDDET13		71	76	81	%UVBUS
		1110	VDDDET14		75	80	85	%UVBUS
1111	VDDDET15		79	84	89	%UVBUS		

(5) When reference voltage (+) = AVDD (ADREFP1 = 0, ADREFP0 = 0), reference voltage (-) = AVSS (ADREFM = 0), conversion target: ANI16 to ANI21, internal reference voltage, temperature sensor output voltage

(TA = -40 to +85°C, 1.6 V ≤ VDD ≤ 3.6 V, 1.6 V ≤ AVDD = VDD ≤ 3.6 V, VSS = 0 V, AVSS = 0 V, Reference voltage (+) = AVDD, Reference voltage (-) = AVSS = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES		2.4 V ≤ AVDD ≤ 3.6 V	8		12	bit
			1.8 V ≤ AVDD ≤ 3.6 V	8		10 Note 1	
			1.6 V ≤ AVDD ≤ 3.6 V	8 Note 2			
Overall error Note 3	AINL	12-bit resolution	2.4 V ≤ AVDD ≤ 3.6 V			±8.5	LSB
		10-bit resolution	1.8 V ≤ AVDD ≤ 3.6 V			±6.0	
		8-bit resolution	1.6 V ≤ AVDD ≤ 3.6 V			±3.5	
Conversion time	tCONV	ADTYP = 0, 12-bit resolution	2.4 V ≤ AVDD ≤ 3.6 V	4.125			μs
		ADTYP = 0, 10-bit resolution Note 1	1.8 V ≤ AVDD ≤ 3.6 V	9.5			
		ADTYP = 0, 8-bit resolution Note 2	1.6 V ≤ AVDD ≤ 3.6 V	57.5			
		ADTYP = 1, 8-bit resolution	2.4 V ≤ AVDD ≤ 3.6 V	3.3125			
			1.8 V ≤ AVDD ≤ 3.6 V	7.875			
Zero-scale error Note 3	Ezs	12-bit resolution	2.4 V ≤ AVDD ≤ 3.6 V			±8.0	LSB
		10-bit resolution	1.8 V ≤ AVDD ≤ 3.6 V			±5.5	
		8-bit resolution	1.6 V ≤ AVDD ≤ 3.6 V			±3.0	
Full-scale error Note 3	EFS	12-bit resolution	2.4 V ≤ AVDD ≤ 3.6 V			±8.0	LSB
		10-bit resolution	1.8 V ≤ AVDD ≤ 3.6 V			±5.5	
		8-bit resolution	1.6 V ≤ AVDD ≤ 3.6 V			±3.0	
Integral linearity error Note 3	ILE	12-bit resolution	2.4 V ≤ AVDD ≤ 3.6 V			±3.5	LSB
		10-bit resolution	1.8 V ≤ AVDD ≤ 3.6 V			±2.5	
		8-bit resolution	1.6 V ≤ AVDD ≤ 3.6 V			±1.5	
Differential linearity error Note 3	DLE	12-bit resolution	2.4 V ≤ AVDD ≤ 3.6 V			±2.5	LSB
		10-bit resolution	1.8 V ≤ AVDD ≤ 3.6 V			±2.5	
		8-bit resolution	1.6 V ≤ AVDD ≤ 3.6 V			±2.0	
Analog input voltage	VAIN			0		AVDD	V
		Internal reference voltage (2.4 V ≤ VDD ≤ 3.6 V, HS (high-speed main) mode)		VBGR Note 4			
		Temperature sensor output voltage (2.4 V ≤ VDD ≤ 3.6 V, HS (high-speed main) mode)		VTMP25 Note 4			

Note 1. Cannot be used for lower 2 bits of ADCR register

Note 2. Cannot be used for lower 4 bits of ADCR register

Note 3. Excludes quantization error (±1/2 LSB).

Note 4. Refer to 2.6.2 Temperature sensor, internal reference voltage output characteristics.

Caution Always use AVDD pin with the same potential as the VDD pin.

2.6.6 LVD circuit characteristics

(TA = -40 to +85°C, VPDR ≤ VDD ≤ 3.6 V ≤ VSS = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	VLVD2	Power supply rise time	3.07	3.13	3.19	V
			Power supply fall time	3.00	3.06	3.12	V
		VLVD3	Power supply rise time	2.96	3.02	3.08	V
			Power supply fall time	2.90	2.96	3.02	V
		VLVD4	Power supply rise time	2.86	2.92	2.97	V
			Power supply fall time	2.80	2.86	2.91	V
		VLVD5	Power supply rise time	2.76	2.81	2.87	V
			Power supply fall time	2.70	2.75	2.81	V
		VLVD6	Power supply rise time	2.66	2.71	2.76	V
			Power supply fall time	2.60	2.65	2.70	V
		VLVD7	Power supply rise time	2.56	2.61	2.66	V
			Power supply fall time	2.50	2.55	2.60	V
		VLVD8	Power supply rise time	2.45	2.50	2.55	V
			Power supply fall time	2.40	2.45	2.50	V
		VLVD9	Power supply rise time	2.05	2.09	2.13	V
			Power supply fall time	2.00	2.04	2.08	V
		VLVD10	Power supply rise time	1.94	1.98	2.02	V
			Power supply fall time	1.90	1.94	1.98	V
		VLVD11	Power supply rise time	1.84	1.88	1.91	V
			Power supply fall time	1.80	1.84	1.87	V
		VLVD12	Power supply rise time	1.74	1.77	1.81	V
			Power supply fall time	1.70	1.73	1.77	V
		VLVD13	Power supply rise time	1.64	1.67	1.70	V
			Power supply fall time	1.60	1.63	1.66	V
Minimum pulse width	tLW		300			μs	
Detection delay time					300	μs	

Caution Set the detection voltage (VLVD) to be within the operating voltage range. The operating voltage range depends on the setting of the user option byte (000C2H/010C2H). The following shows the operating voltage range.

HS (high-speed main) mode: VDD = 2.7 to 3.6 V at 1 MHz to 24 MHz

VDD = 2.4 to 3.6 V at 1 MHz to 16 MHz

LS (low-speed main) mode: VDD = 1.8 to 3.6 V at 1 MHz to 8 MHz

LV (low-voltage main) mode: VDD = 1.6 to 3.6 V at 1 MHz to 4 MHz

2.8.2 Internal voltage boosting method

(1) 1/3 bias method

(TA = -40 to +85°C, 1.8 V ≤ VDD ≤ 3.6 V, VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
LCD output voltage variation range	VL1	C1 to C4 ^{Note 1} = 0.47 μF ^{Note 2}	VLCD = 04H	0.90	1.00	1.08	V
			VLCD = 05H	0.95	1.05	1.13	V
			VLCD = 06H	1.00	1.10	1.18	V
			VLCD = 07H	1.05	1.15	1.23	V
			VLCD = 08H	1.10	1.20	1.28	V
			VLCD = 09H	1.15	1.25	1.33	V
			VLCD = 0AH	1.20	1.30	1.38	V
			VLCD = 0BH	1.25	1.35	1.43	V
			VLCD = 0CH	1.30	1.40	1.48	V
			VLCD = 0DH	1.35	1.45	1.53	V
			VLCD = 0EH	1.40	1.50	1.58	V
			VLCD = 0FH	1.45	1.55	1.63	V
			VLCD = 10H	1.50	1.60	1.68	V
			VLCD = 11H	1.55	1.65	1.73	V
VLCD = 12H	1.60	1.70	1.78	V			
VLCD = 13H	1.65	1.75	1.83	V			
Doubler output voltage	VL2	C1 to C4 ^{Note 1} = 0.47 μF	2 VL1 - 0.1	2 VL1	2 VL1	V	
Tripler output voltage	VL3	C1 to C4 ^{Note 1} = 0.47 μF	3 VL1 - 0.15	3 VL1	3 VL1	V	
Reference voltage setup time ^{Note 2}	tVWAIT1		5			ms	
Voltage boost wait time ^{Note 3}	tVWAIT2	C1 to C4 ^{Note 1} = 0.47 μF	500			ms	

Note 1. This is a capacitor that is connected between voltage pins used to drive the LCD.

C1: A capacitor connected between CAPH and CAPL

C2: A capacitor connected between VL1 and GND

C3: A capacitor connected between VL2 and GND

C4: A capacitor connected between VL4 and GND

C1 = C2 = C3 = C4 = 0.47 μF ± 30%

Note 2. This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected (by setting the MDSET1 and MDSET0 bits of the LCDM0 register to 01B) if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).

Note 3. This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

(TA = -40 to +105°C, 2.4 V ≤ AVDD = VDD ≤ 3.6 V, VSS = 0 V)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Output voltage, high	VOH1	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P46, P50 to P57, P70 to P77, P80 to P83, P125 to P127, P130, P140 to P143	2.7 V ≤ VDD ≤ 3.6 V, IOH1 = -2.0 mA	VDD - 0.6			V
			2.4 V ≤ VDD ≤ 3.6 V, IOH1 = -1.5 mA	VDD - 0.5			V
	VOH2	P150 to P156	2.4 V ≤ VDD ≤ 3.6 V, IOH2 = -100 μA	AVDD - 0.5			V
Output voltage, low	VOL1	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P46, P50 to P57, P70 to P77, P80 to P83, P125 to P127, P130, P140 to P143	2.7 V ≤ VDD ≤ 3.6 V, IOL1 = 3.0 mA			0.6	V
			2.4 V ≤ VDD ≤ 3.6 V, IOL1 = 1.5 mA			0.4	V
			2.4 V ≤ VDD ≤ 3.6 V, IOL1 = 0.6 mA			0.4	V
	VOL2	P150 to P156	2.4 V ≤ VDD ≤ 3.6 V, IOL2 = 400 μA			0.4	V
	VOL3	P60, P61	2.7 V ≤ VDD ≤ 3.6 V, IOL3 = 3.0 mA			0.4	V
			2.4 V ≤ VDD ≤ 3.6 V, IOL3 = 2.0 mA			0.4	V

Caution P00 to P02, P10 to P12, P24 to P26, P33 to P35, and P42 to P44 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(TA = -40 to +105°C, 2.4 V ≤ VDD ≤ 3.6 V, VSS = 0 V)

(2/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit			
Supply current Note 1	IDD2 Note 2	HALT mode	HS (high-speed main) mode Note 7	fHOCO = 48 MHz Note 4, fIH = 24 MHz Note 4	VDD = 3.6 V		0.77	3.4	mA	
					VDD = 3.0 V		0.77	3.4		
				fHOCO = 24 MHz Note 4, fIH = 24 MHz Note 4	VDD = 3.6 V		0.55	2.7		
					VDD = 3.0 V		0.55	2.7		
				fHOCO = 16 MHz Note 4, fIH = 16 MHz Note 4	VDD = 3.6 V		0.48	1.9		
					VDD = 3.0 V		0.47	1.9		
			HS (high-speed main) mode Note 7	fMX = 20 MHz Note 3, VDD = 3.6 V	Square wave input		0.35	2.10	mA	
					Resonator connection		0.51	2.20		
				fMX = 20 MHz Note 3, VDD = 3.0 V	Square wave input		0.34	2.10		
					Resonator connection		0.51	2.20		
				fMX = 16 MHz Note 3, VDD = 3.6 V	Square wave input		0.30	1.25		
					Resonator connection		0.45	1.41		
		fMX = 16 MHz Note 3, VDD = 3.0 V		Square wave input		0.29	1.23			
				Resonator connection		0.45	1.41			
		fMX = 10 MHz Note 3, VDD = 3.6 V		Square wave input		0.23	1.10			
				Resonator connection		0.30	1.20			
		fMX = 10 MHz Note 3, VDD = 3.0 V		Square wave input		0.22	1.10			
				Resonator connection		0.30	1.20			
		HS (High-speed main) mode (PLL operation)	fMX = 48 MHz, fCLK = 24 MHz Note 3	VDD = 3.6 V		0.99	2.93	mA		
				VDD = 3.0 V		0.99	2.92			
			fMX = 48 MHz, fCLK = 12 MHz Note 3	VDD = 3.6 V		0.89	2.51			
				VDD = 3.0 V		0.89	2.50			
			fMX = 48 MHz, fCLK = 6 MHz Note 3	VDD = 3.6 V		0.84	2.30			
				VDD = 3.0 V		0.84	2.29			
			Subsystem clock operation	fsUB = 32.768 kHz Note 5 TA = -40°C	Square wave input		0.32		0.61	μA
					Resonator connection		0.51		0.80	
		fsUB = 32.768 kHz Note 5 TA = +25°C		Square wave input		0.41	0.74			
Resonator connection				0.62	0.91					
fsUB = 32.768 kHz Note 5 TA = +50°C	Square wave input			0.52	2.30					
	Resonator connection			0.75	2.49					
fsUB = 32.768 kHz Note 5 TA = +70°C	Square wave input			0.82	4.03					
	Resonator connection			1.08	4.22					
fsUB = 32.768 kHz Note 5 TA = +85°C	Square wave input			1.38	8.04					
	Resonator connection			1.62	8.23					
fsUB = 32.768 kHz Note 5 TA = +105°C	Square wave input			3.29	41.00					
	Resonator connection			3.63	41.00					
IDD3 Note 6	STOP mode Note 8	TA = -40°C			0.18	0.52	μA			
		TA = +25°C			0.25	0.52				
		TA = +50°C			0.34	2.21				
		TA = +70°C			0.64	3.94				
		TA = +85°C			1.18	7.95				
		TA = +105°C			2.92	40.00				

(Notes and Remarks are listed on the next page.)

3.5.2 Serial interface IICA

(TA = -40 to +105°C, 2.4 V ≤ VDD ≤ 3.6 V, VSS = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode				Unit
			Standard mode		Fast mode		
			MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	fSCL	Fast mode: fCLK ≥ 3.5 MHz	—	—	0	400	kHz
		Standard mode: fCLK ≥ 1 MHz	0	100	—	—	kHz
Setup time of restart condition	tSU: STA		4.7		0.6		μs
Hold time Note 1	tHD: STA		4.0		0.6		μs
Hold time when SCLA0 = "L"	tLOW		4.7		1.3		μs
Hold time when SCLA0 = "H"	tHIGH		4.0		0.6		μs
Data setup time (reception)	tSU: DAT		250		100		ns
Data hold time (transmission) Note 2	tHD: DAT		0	3.45	0	0.9	μs
Setup time of stop condition	tSU: STO		4.0		0.6		μs
Bus-free time	tBUF		4.7		1.3		μs

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.

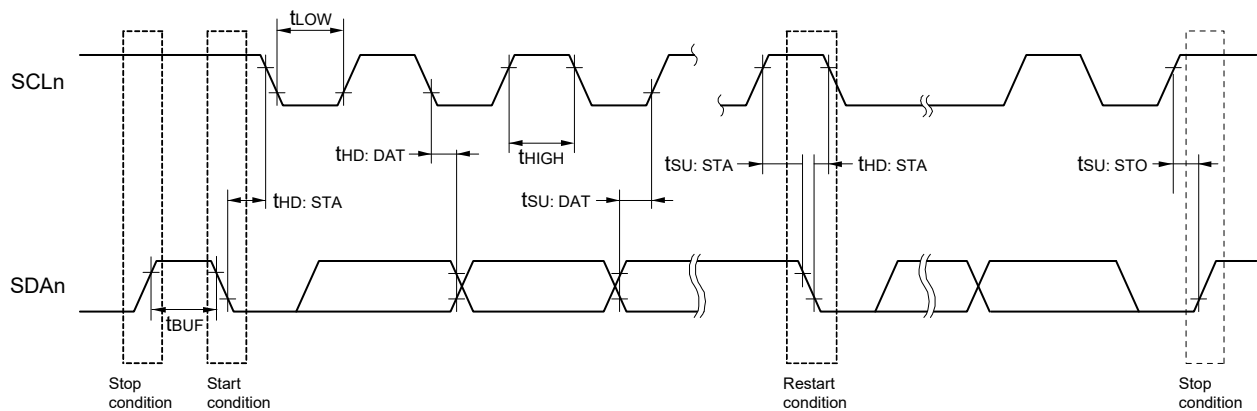
Note 2. The maximum value (MAX.) of tHD:DAT is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Remark The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: Cb = 400 pF, Rb = 2.7 kΩ

Fast mode: Cb = 320 pF, Rb = 1.1 kΩ

IICA serial transfer timing



(5) When reference voltage (+) = Internal reference voltage (1.45 V) (ADREFP1 = 1, ADREFP0 = 0), reference voltage (-) = AVss (ADREFM = 0), conversion target: ANI0 to ANI6, ANI16 to ANI21

(TA = -40 to +105°C, 2.4 V ≤ VDD ≤ 3.6 V, 2.4 V ≤ VDD, 2.4 V ≤ AVDD = VDD, VSS = 0 V, AVSS = 0 V,

Reference voltage (+) = internal reference voltage, Reference voltage (-) = AVSS = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES		8			bit
Conversion time	tCONV	8-bit resolution	16.0			μs
Zero-scale error ^{Note}	EZS	8-bit resolution			±4.0	LSB
Integral linearity error ^{Note}	ILE	8-bit resolution			±2.0	LSB
Differential linearity error ^{Note}	DLE	8-bit resolution			±2.5	LSB
Reference voltage (+)	AVREF(+)	= Internal reference voltage (VBGR)	1.38	1.45	1.5	V
Analog input voltage	VAIN		0		VBGR	V

Note Excludes quantization error (±1/2 LSB).

Caution Always use AVDD pin with the same potential as the VDD pin.

3.6.2 Temperature sensor, internal reference voltage output characteristics

(TA = -40 to +105°C, 2.4 V ≤ VDD ≤ 3.6 V, VSS = 0 V (HS (high-speed main) mode))

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	VTMPS25	Setting ADS register = 80H, TA = +25°C		1.05		V
Internal reference voltage	VBGR	Setting ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	FVTMPS	Temperature sensor output voltage that depends on the temperature		-3.6		mV/°C
Operation stabilization wait time	tAMP		10			μs

3.6.3 D/A converter characteristics

(TA = -40 to +105°C, 2.4 V ≤ VDD ≤ 3.6 V, VSS = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES					8	bit
Overall error	AINL	Rload = 4 MΩ	2.4 V ≤ VDD ≤ 3.6 V			±2.5	LSB
		Rload = 8 MΩ	2.4 V ≤ VDD ≤ 3.6 V			±2.5	LSB
Settling time	tSET	Cload = 20 pF	2.7 V ≤ VDD ≤ 3.6 V			3	μs
			2.4 V ≤ VDD < 2.7 V			6	μs

3.6.4 Comparator

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage range	Ivref		0		$V_{DD} - 1.4$	V
	Ivcmp		-0.3		$V_{DD} + 0.3$	V
Output delay	td	$V_{DD} = 3.0\text{ V}$ Input slew rate $> 50\text{ mV}/\mu\text{s}$	High-speed comparator mode, standard mode		1.2	μs
			High-speed comparator mode, window mode		2.0	μs
			Low-speed comparator mode, standard mode		3	5.0
High-electric-potential judgment voltage	VTW+	High-speed comparator mode, window mode		$0.76 V_{DD}$		V
Low-electric-potential judgment voltage	VTW-	High-speed comparator mode, window mode		$0.24 V_{DD}$		V
Operation stabilization wait time	tCMP		100			μs
Internal reference voltage <small>Note</small>	VBGR	$2.4\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, HS (high-speed main) mode	1.38	1.45	1.50	V

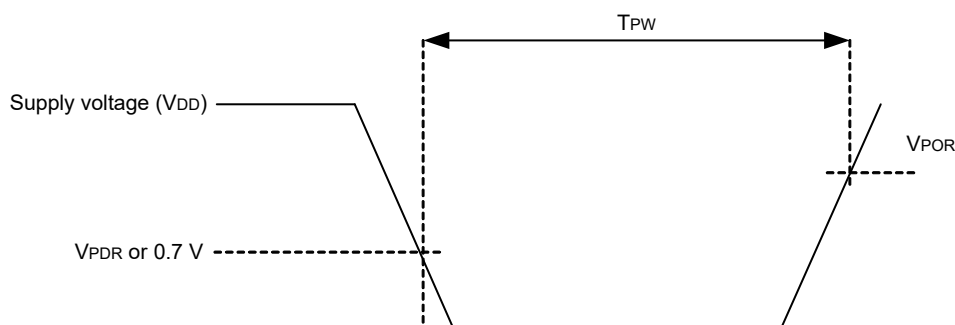
Note Not usable in sub-clock operation or STOP mode.

3.6.5 POR circuit characteristics

($T_A = -40$ to $+105^\circ\text{C}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	VPOR	Power supply rise time	1.45	1.51	1.57	V
	VPDR	Power supply fall time <small>Note</small>	1.44	1.50	1.56	V
Minimum pulse width	TPW		300			μs

Note Minimum time required for a POR reset when V_{DD} exceeds below V_{PDR} . This is also the minimum time required for a POR reset from when V_{DD} exceeds below 0.7 V to when V_{DD} exceeds V_{POR} while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



3.8 LCD Characteristics

3.8.1 Resistance division method

(1) Static display mode

(TA = -40 to +105°C, VL4 (MIN.) ≤ VDD ≤ 3.6 V, VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	VL4		2.0		VDD	V

(2) 1/2 bias method, 1/4 bias method

(TA = -40 to +105°C, VL4 (MIN.) ≤ VDD ≤ 3.6 V, VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	VL4		2.7		VDD	V

(3) 1/3 bias method

(TA = -40 to +105°C, VL4 (MIN.) ≤ VDD ≤ 3.6 V, VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	VL4		2.5		VDD	V