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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

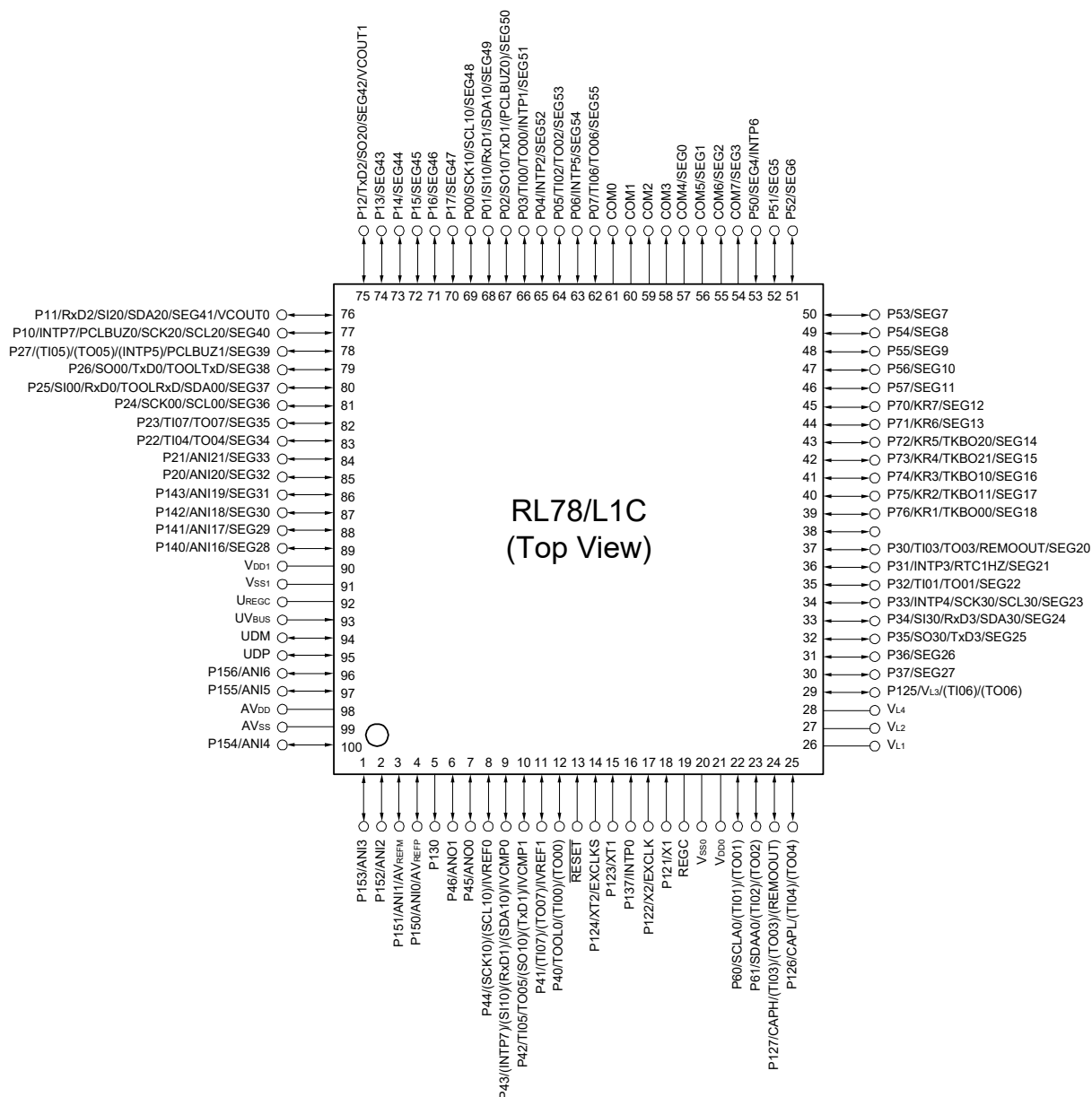
Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I ² C, LINbus, UART/USART
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	55
Program Memory Size	192KB (192K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 11x8/12b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f111mhafb-30

1.3.5 100-pin products (with USB)

- 100-pin plastic LFQFP (fine pitch) (14 × 14 mm, 0.5 mm pitch)



Caution 1. Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).

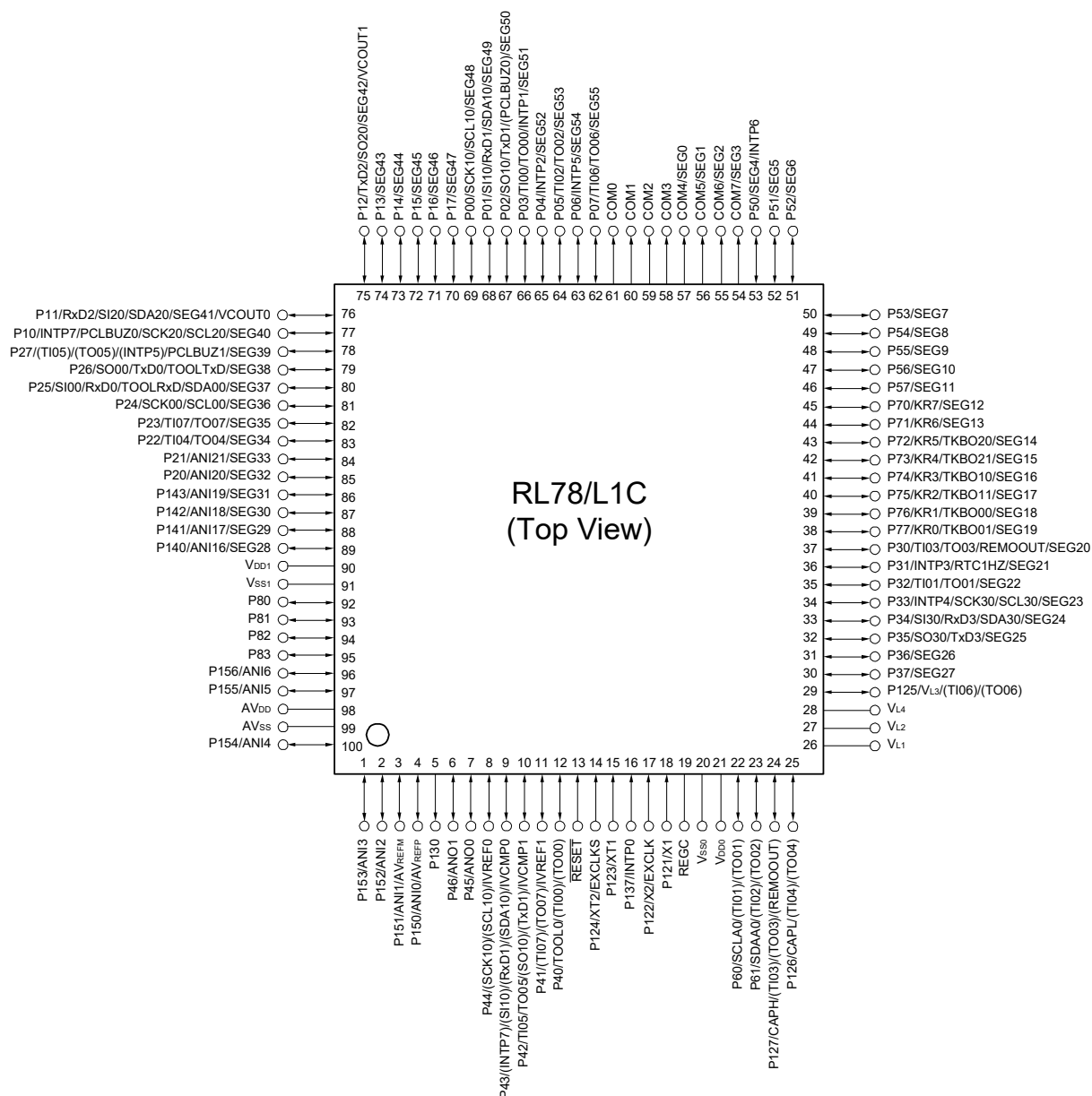
Caution 2. Connect the UREGC pin to Vss pin via a capacitor (0.33 μF).

Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.3.6 100-pin products (without USB)

- 100-pin plastic LFQFP (fine pitch) (14 × 14 mm, 0.5 mm pitch)



Caution Connect the REGC pin to V_{ss} pin via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

(2/2)

Item		80/85-pin	100-pin
		R5F110Mx/R5F110Nx (x = E to H, J)	R5F110Px (x = E to H, J)
Clock output/buzzer output		2	2
		2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f_{MAIN} = 20 MHz operation) 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: f_{SUB} = 32.768 kHz operation)	
8/12-bit resolution A/D converter		9 channels	13 channels
D/A converter		2 channels	2 channels
Comparator		1 channel	2 channels
Serial interface		- CSI: 1 channel/UART (UART supporting LIN-bus): 1 channel/simplified I²C: 1 channel - CSI: 1 channel/UART: 1 channel/simplified I²C: 1 channel - CSI: 1 channel/UART: 1 channel/simplified I²C: 1 channel - CSI: 1 channel/UART: 1 channel/simplified I²C: 1 channel	
	I ² C bus	1 channel	1 channel
USB	Function	1 channel	
LCD controller/driver		Internal voltage boosting method, capacitor split method, and external resistance division method are switchable.	
	Segment signal output	44 (40) ^{Note 1}	56 (52) ^{Note 1}
	Common signal output	4 (8) ^{Note 1}	
Data transfer controller (DTC)		32 sources	33 sources
Event link controller (ELC)		Event input: 30, Event trigger output: 22	Event input: 31, Event trigger output: 22
Vectored interrupt sources	Internal	36	37
	External	9	9
Key interrupt		8	8
Reset		- Reset by $\overline{\text{RESET}}$ pin - Internal reset by watchdog timer - Internal reset by power-on-reset - Internal reset by voltage detector - Internal reset by illegal instruction execution ^{Note 2} - Internal reset by RAM parity error - Internal reset by illegal-memory access	
Power-on-reset circuit		- Power-on-reset: 1.51 ± 0.03 V - Power-down-reset: 1.50 ± 0.03 V	
Voltage detector		- Rising edge: 1.67 V to 3.13 V (12 stages) - Falling edge: 1.63 V to 3.06 V (12 stages)	
On-chip debug function		Provided	
Power supply voltage		V _{DD} = 1.6 to 3.6 V (TA = -40 to +85°C) V _{DD} = 2.4 to 3.6 V (TA = -40 to +105°C)	
Operating ambient temperature		TA = -40 to +85°C (A: Consumer applications), TA = -40 to +105°C (G: Industrial applications)	

Note 1. The number in parentheses indicates the number of signal outputs when 8 coms are used.

Note 2. The illegal instruction is generated when instruction code FFH is executed.

Reset by the illegal instruction execution not is issued by emulation with the in-circuit emulator or on-chip debug emulator.

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2.4 AC Characteristics

2.4.1 Basic operation

(T_A = -40 to +85°C, 1.6 V ≤ AV_{DD} = V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

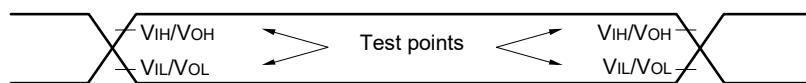
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Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T _{CY}	Main system clock (f _{MAIN}) operation	HS (high-speed main) mode	2.7 V ≤ V _{DD} ≤ 3.6 V	0.0417		1	μs
				2.4 V ≤ V _{DD} < 2.7 V	0.0625		1	μs
			LS (low-speed main) mode	1.8 V ≤ V _{DD} ≤ 3.6 V	0.125		1	μs
			LV (low-voltage main) mode	1.6 V ≤ V _{DD} ≤ 3.6 V	0.25		1	μs
		Subsystem clock (f _{SUB}) operation			28.5	30.5	31.3	μs
		In the self- programming mode	HS (high-speed main) mode	2.7 V ≤ V _{DD} ≤ 3.6 V	0.0417		1	μs
				2.4 V ≤ V _{DD} < 2.7 V	0.0625		1	μs
			LS (low-speed main) mode	1.8 V ≤ V _{DD} ≤ 3.6 V	0.125		1	μs
			LV (low-voltage main) mode	1.8 V ≤ V _{DD} ≤ 3.6 V	0.25		1	μs
External main system clock frequency	f _{EX}	2.7 V ≤ V _{DD} ≤ 3.6 V			1.0		20.0	MHz
		2.4 V ≤ V _{DD} < 2.7 V			1.0		16.0	MHz
		1.8 V ≤ V _{DD} < 2.4 V			1.0		8.0	MHz
		1.6 V ≤ V _{DD} < 1.8 V			1.0		4.0	MHz
	f _{EXT}				32		35	kHz
External main system clock input high-level width, low-level width	t _{EXH} , t _{EXL}	2.7 V ≤ V _{DD} ≤ 3.6 V			24			ns
		2.4 V ≤ V _{DD} < 2.7 V			30			ns
		1.8 V ≤ V _{DD} < 2.4 V			60			ns
		1.6 V ≤ V _{DD} < 1.8 V			120			ns
	t _{EXHS} , t _{EXLS}				13.7			μs
Ti00 to Ti07 input high-level width, low-level width	t _{TIH} , t _{TIL}				1/f _{MCK} + 10			ns

Remark f_{MCK}: Timer array unit operation clock frequency
 (Operation clock to be set by the CKSmn bit of timer mode register mn (TMRmn). m: Unit number (m = 0),
 n: Channel number (n = 0 to 7))

2.5 Peripheral Functions Characteristics

AC Timing Test Points



2.5.1 Serial array unit

(1) During communication at same potential (UART mode)

(T_A = -40 to +85°C, 1.6 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate Note 1		2.7 V ≤ V _{DD} ≤ 3.6 V		f _{MCK} /6 Note 2		f _{MCK} /6		f _{MCK} /6	bps
		Theoretical value of the maximum transfer rate f _{MCK} = f _{CLK} Note 3		4.0		1.3		0.6	Mbps
		2.4 V ≤ V _{DD} ≤ 3.6 V		f _{MCK} /6 Note 2		f _{MCK} /6		f _{MCK} /6	bps
		Theoretical value of the maximum transfer rate f _{MCK} = f _{CLK} Note 3		2.6		1.3		0.6	Mbps
		1.8 V ≤ V _{DD} ≤ 3.6 V	—			f _{MCK} /6 Note 2		f _{MCK} /6	bps
		Theoretical value of the maximum transfer rate f _{MCK} = f _{CLK} Note 3	—			1.3		0.6	Mbps
		1.6 V ≤ V _{DD} ≤ 3.6 V	—		—			f _{MCK} /6	bps
		Theoretical value of the maximum transfer rate f _{MCK} = f _{CLK} Note 3	—		—			0.6	Mbps

Note 1. Transfer rate in the SNOOZE mode is 4800 bps only.

Note 2. The following conditions are required for low voltage interface.

2.4 V ≤ V_{DD} < 2.7 V: MAX. 2.6 Mbps

1.8 V ≤ V_{DD} < 2.4 V: MAX. 1.3 Mbps

1.6 V ≤ V_{DD} < 1.8 V: MAX. 0.6 Mbps

Note 3. The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:

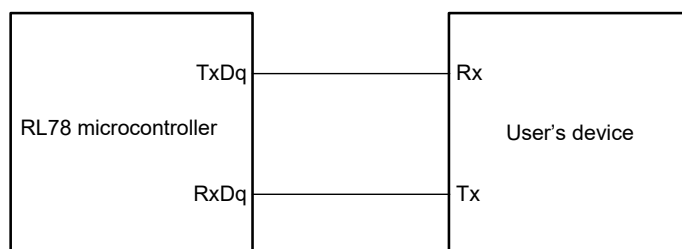
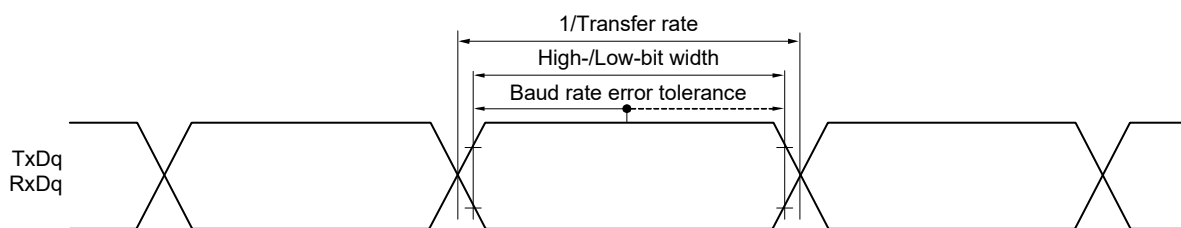
HS (high-speed main) mode: 24 MHz (2.7 V ≤ V_{DD} ≤ 3.6 V)

16 MHz (2.4 V ≤ V_{DD} ≤ 3.6 V)

LS (low-speed main) mode: 8 MHz (1.8 V ≤ V_{DD} ≤ 3.6 V)

LV (low-voltage main) mode: 4 MHz (1.6 V ≤ V_{DD} ≤ 3.6 V)

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

UART mode connection diagram (during communication at same potential)**UART mode bit width (during communication at same potential) (reference)**

Remark 1. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0 to 3)

Remark 2. f_{MCK}: Serial array unit operation clock frequency

(Operation clock to be set by the CKSMn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00 to 03, 10 to 13))

(2) I²C fast mode**(TA = -40 to +85°C, 1.8 V ≤ VDD ≤ 3.6 V, VSS = 0 V)**

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	fSCL	Fast mode: fCLK ≥ 3.5 MHz	2.7 V ≤ VDD ≤ 3.6 V	0	400	0	400	0	400	kHz
			1.8 V ≤ VDD ≤ 3.6 V	0	400	0	400	0	400	kHz
Setup time of restart condition	tSU: STA	2.7 V ≤ VDD ≤ 3.6 V		0.6		0.6		0.6		μs
		1.8 V ≤ VDD ≤ 3.6 V		0.6		0.6		0.6		μs
Hold time ^{Note 1}	tHD: STA	2.7 V ≤ VDD ≤ 3.6 V		0.6		0.6		0.6		μs
		1.8 V ≤ VDD ≤ 3.6 V		0.6		0.6		0.6		μs
Hold time when SCLA0 = "L"	tLOW	2.7 V ≤ VDD ≤ 3.6 V		1.3		1.3		1.3		μs
		1.8 V ≤ VDD ≤ 3.6 V		1.3		1.3		1.3		μs
Hold time when SCLA0 = "H"	tHIGH	2.7 V ≤ VDD ≤ 3.6 V		0.6		0.6		0.6		μs
		1.8 V ≤ VDD ≤ 3.6 V		0.6		0.6		0.6		μs
Data setup time (reception)	tSU: DAT	2.7 V ≤ VDD ≤ 3.6 V		100		100		100		ns
		1.8 V ≤ VDD ≤ 3.6 V		100		100		100		ns
Data hold time (transmission) ^{Note 2}	tHD: DAT	2.7 V ≤ VDD ≤ 3.6 V		0	0.9	0	0.9	0	0.9	μs
		1.8 V ≤ VDD ≤ 3.6 V		0	0.9	0	0.9	0	0.9	μs
Setup time of stop condition	tSU: STO	2.7 V ≤ VDD ≤ 3.6 V		0.6		0.6		0.6		μs
		1.8 V ≤ VDD ≤ 3.6 V		0.6		0.6		0.6		μs
Bus-free time	tBUF	2.7 V ≤ VDD ≤ 3.6 V		1.3		1.3		1.3		μs
		1.8 V ≤ VDD ≤ 3.6 V		1.3		1.3		1.3		μs

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.

Note 2. The maximum value (MAX.) of tHD: DAT is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.
Fast mode: C_b = 320 pF, R_b = 1.1 kΩ

(6) When reference voltage (+) = Internal reference voltage (1.45 V) (ADREFP1 = 1, ADREFP0 = 0), reference voltage (-) = AVss (ADREFM = 0), conversion target: ANI0 to ANI6, ANI16 to ANI21

(TA = -40 to +85°C, 2.4 V ≤ VDD ≤ 3.6 V, 1.6 V ≤ VDD, 1.6 V ≤ AVDD = VDD, Vss = 0 V, AVss = 0 V, Reference voltage (+) = internal reference voltage, Reference voltage (-) = AVss = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES		8			bit
Conversion time	tCONV	8-bit resolution	16			μs
Zero-scale error ^{Note}	EZS	8-bit resolution			±4.0	LSB
Integral linearity error ^{Note}	ILE	8-bit resolution			±2.0	LSB
Differential linearity error ^{Note}	DLE	8-bit resolution			±2.5	LSB
Reference voltage (+)	AVREF(+)	= Internal reference voltage (VBGR)	1.38	1.45	1.5	V
Analog input voltage	VAIN		0		VBGR	V

Note Excludes quantization error (±1/2 LSB).

Caution Always use AVDD pin with the same potential as the VDD pin.

2.6.2 Temperature sensor, internal reference voltage output characteristics

(TA = -40 to +85°C, 2.4 V ≤ VDD ≤ 3.6 V, Vss = 0 V (HS (high-speed main) mode))

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	VTMPS25	Setting ADS register = 80H, TA = +25°C		1.05		V
Internal reference voltage	VBGR	Setting ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	FVTMPS	Temperature sensor output voltage that depends on the temperature		-3.6		mV/°C
Operation stabilization wait time	tAMP		10			μs

2.6.3 D/A converter characteristics

(TA = -40 to +85°C, 1.6 V ≤ VDD ≤ 3.6 V, Vss = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES					8	bit
Overall error	AINL	Rload = 4 MΩ	1.8 V ≤ VDD ≤ 3.6 V			±2.5	LSB
		Rload = 8 MΩ	1.8 V ≤ VDD ≤ 3.6 V			±2.5	LSB
Settling time	tSET	Cload = 20 pF	2.7 V ≤ VDD ≤ 3.6 V			3	μs
			1.6 V ≤ VDD < 2.7 V			6	μs

2.6.6 LVD circuit characteristics

(TA = -40 to +85°C, VPDR ≤ VDD ≤ 3.6 V ≤ VSS = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	VLVD2	Power supply rise time	3.07	3.13	3.19	V
			Power supply fall time	3.00	3.06	3.12	V
		VLVD3	Power supply rise time	2.96	3.02	3.08	V
			Power supply fall time	2.90	2.96	3.02	V
		VLVD4	Power supply rise time	2.86	2.92	2.97	V
			Power supply fall time	2.80	2.86	2.91	V
		VLVD5	Power supply rise time	2.76	2.81	2.87	V
			Power supply fall time	2.70	2.75	2.81	V
		VLVD6	Power supply rise time	2.66	2.71	2.76	V
			Power supply fall time	2.60	2.65	2.70	V
		VLVD7	Power supply rise time	2.56	2.61	2.66	V
			Power supply fall time	2.50	2.55	2.60	V
		VLVD8	Power supply rise time	2.45	2.50	2.55	V
			Power supply fall time	2.40	2.45	2.50	V
		VLVD9	Power supply rise time	2.05	2.09	2.13	V
			Power supply fall time	2.00	2.04	2.08	V
		VLVD10	Power supply rise time	1.94	1.98	2.02	V
			Power supply fall time	1.90	1.94	1.98	V
		VLVD11	Power supply rise time	1.84	1.88	1.91	V
			Power supply fall time	1.80	1.84	1.87	V
		VLVD12	Power supply rise time	1.74	1.77	1.81	V
			Power supply fall time	1.70	1.73	1.77	V
		VLVD13	Power supply rise time	1.64	1.67	1.70	V
			Power supply fall time	1.60	1.63	1.66	V
Minimum pulse width		tLW		300			μs
Detection delay time						300	μs

Caution Set the detection voltage (VLVD) to be within the operating voltage range. The operating voltage range depends on the setting of the user option byte (000C2H/010C2H). The following shows the operating voltage range.

HS (high-speed main) mode: VDD = 2.7 to 3.6 V at 1 MHz to 24 MHz

VDD = 2.4 to 3.6 V at 1 MHz to 16 MHz

LS (low-speed main) mode: VDD = 1.8 to 3.6 V at 1 MHz to 8 MHz

LV (low-voltage main) mode: VDD = 1.6 to 3.6 V at 1 MHz to 4 MHz

Absolute Maximum Ratings (TA = 25°C)**(2/3)**

Parameter	Symbols	Conditions		Ratings	Unit
LCD voltage	VL11	VL1 input voltage ^{Note 1}		-0.3 to +2.8	V
	VL12	VL2 input voltage ^{Note 1}		-0.3 to +6.5	V
	VL13	VL3 input voltage ^{Note 1}		-0.3 to +6.5	V
	VL14	VL4 input voltage ^{Note 1}		-0.3 to +6.5	V
	VL15	CAPL, CAPH input voltage ^{Note 1}		-0.3 to +6.5	V
	VLO1	VL1 output voltage		-0.3 to +2.8	V
	VLO2	VL2 output voltage		-0.3 to +6.5	V
	VLO3	VL3 output voltage		-0.3 to +6.5	V
	VLO4	VL4 output voltage		-0.3 to +6.5	V
	VLO5	CAPL, CAPH output voltage		-0.3 to +6.5	V
	VLO6	COM0 to COM7 SEG0 to SEG55 output voltage	External resistance division method	-0.3 to V _{DD} + 0.3 ^{Note 2}	V
			Capacitor split method	-0.3 to V _{DD} + 0.3 ^{Note 2}	V
			Internal voltage boosting method	-0.3 to VL14 + 0.3 ^{Note 2}	V

Note 1. This value only indicates the absolute maximum ratings when applying voltage to the VL1, VL2, VL3, and VL4 pins; it does not mean that applying voltage to these pins is recommended. When using the internal voltage boosting method or capacitance split method, connect these pins to VSS via a capacitor (0.47 ± 30%) and connect a capacitor (0.47 ± 30%) between the CAPL and CAPH pins.

Note 2. Must be 6.5 V or lower.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Absolute Maximum Ratings (TA = 25°C)**(3/3)**

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	IOH1	Per pin	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P46, P50 to P57, P70 to P77, P80 to P83, P125 to P127, P130, P140 to P143	-40	mA
		Total of all pins	P40 to P46	-70	mA
		-170 mA	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P50 to P57, P70 to P77, P80 to P83, P125 to P127, P130, P140 to P143	-100	mA
	IOH2	Per pin	P150 to P156	-0.1	mA
		Total of all pins		-0.7	mA
	IOH3	Per pin	UDP, UDM	-3	mA
Output current, low	IOL1	Per pin	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P46, P50 to P57, P60, P61, P70 to P77, P80 to P83, P125 to P127, P130, P140 to P143	40	mA
		Total of all pins	P40 to P46	70	mA
		170 mA	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P50 to P57, P70 to P77, P80 to P83, P125 to P127, P130, P140 to P143	100	mA
	IOL2	Per pin	P150 to P156	0.4	mA
		Total of all pins		2.8	mA
	IOL3	Per pin	UDP, UDM	3	mA
Operating ambient temperature	TA	In normal operation mode		-40 to +105	°C
		In flash memory programming mode		-40 to +105	
Storage temperature	Tstg			-65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

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(T_A = -40 to +105°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Input leakage current, high	ILI _{H1}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P46, P50 to P57, P60, P61, P70 to P77, P80 to P83, P125 to P127, P137, P140 to P143, <u>RESET</u>	V _I = V _{DD}				1	μA
	ILI _{H2}	P20, P21, P140 to P143	V _I = V _{DD}				1	μA
	ILI _{H3}	P121 to P124 (X1, X2, EXCLK, XT1, XT2, EXCLKS)	V _I = V _{DD}	In input port or external clock input			1	μA
				In resonator connection			10	μA
	ILI _{H4}	P150 to P156	V _I = AV _{DD}				1	μA
Input leakage current, low	ILI _{L1}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P46, P50 to P57, P60, P61, P70 to P77, P80 to P83, P125 to P127, P137, P140 to P143, <u>RESET</u>	V _I = V _{SS}				-1	μA
	ILI _{L2}	P20, P21, P140 to P143	V _I = V _{SS}				-1	μA
	ILI _{L3}	P121 to P124 (X1, X2, EXCLK, XT1, XT2, EXCLKS)	V _I = V _{SS}	In input port or external clock input			-1	μA
				In resonator connection			-10	μA
	ILI _{L4}	P150 to P156	V _I = AV _{SS}				-1	μA
On-chip pull-up resistance	RU ₁	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P50 to P57, P70 to P77, P140 to P143, P125 to P127	V _I = V _{SS}	2.4 V ≤ V _{DD} ≤ 3.6 V	10	20	100	kΩ
	RU ₂	P40 to P46, P80 to P83	V _I = V _{SS}		10	20	100	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

3.3.2 Supply current characteristics

(TA = -40 to +105°C, 2.4 V ≤ VDD ≤ 3.6 V, VSS = 0 V)

(1/2)

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit	
Supply current Note 1	IDD1	Operating mode	HS (high-speed main) mode Note 5	fHOCO = 48 MHz Note 3 , fIH = 24 MHz Note 3	Basic operation	VDD = 3.6 V		2.2	2.9	mA	
						VDD = 3.0 V		2.2	2.9		
					Normal operation	VDD = 3.6 V		4.4	9.2		
						VDD = 3.0 V		4.4	9.2		
				fHOCO = 24 MHz Note 3 , fIH = 24 MHz Note 3	Basic operation	VDD = 3.6 V		2.0	2.6		
						VDD = 3.0 V		2.0	2.6		
					Normal operation	VDD = 3.6 V		4.2	7.0		
						VDD = 3.0 V		4.2	7.0		
				fHOCO = 16 MHz Note 3 , fIH = 16 MHz Note 3	Normal operation	VDD = 3.6 V		3.1	5.0		
						VDD = 3.0 V		3.1	5.0		
			HS (high-speed main) mode Note 5	fMX = 20 MHz Note 2 , VDD = 3.6 V	Normal operation	Square wave input		3.5	5.9	mA	
						Resonator connection		3.6	6.0		
				fMX = 20 MHz Note 2 , VDD = 3.0 V	Normal operation	Square wave input		3.5	5.9		
						Resonator connection		3.6	6.0		
				fMX = 16 MHz Note 2 , VDD = 3.6 V	Normal operation	Square wave input		2.9	4.5		
						Resonator connection		3.1	4.6		
				fMX = 16 MHz Note 2 , VDD = 3.0 V	Normal operation	Square wave input		2.9	4.5		
						Resonator connection		3.1	4.6		
				fMX = 10 MHz Note 2 , VDD = 3.6 V	Normal operation	Square wave input		2.1	3.5		
						Resonator connection		2.2	3.5		
				fMX = 10 MHz Note 2 , VDD = 3.0 V	Normal operation	Square wave input		2.1	3.5		
						Resonator connection		2.2	3.5		
		HS (High-speed main) mode (PLL operation)	fPLL = 48 MHz, fCLK = 24 MHz Note 2	Normal operation	VDD = 3.6 V		4.7	7.6	mA		
					VDD = 3.0 V		4.7	7.6			
			fPLL = 48 MHz, fCLK = 12 MHz Note 2	Normal operation	VDD = 3.6 V		3.1	5.2			
					VDD = 3.0 V		3.1	5.1			
			fPLL = 48 MHz, fCLK = 6 MHz Note 2	Normal operation	VDD = 3.6 V		2.3	3.9			
					VDD = 3.0 V		2.3	3.9			
			Subsystem clock operation	fSUB = 32.768 kHz Note 4 TA = -40°C	Normal operation	Square wave input		4.6		6.9	μA
						Resonator connection		4.7		6.9	
		fSUB = 32.768 kHz Note 4 TA = +25°C		Normal operation	Square wave input		4.9	7.0			
					Resonator connection		5.0	7.2			
		fSUB = 32.768 kHz Note 4 TA = +50°C		Normal operation	Square wave input		5.2	7.6			
					Resonator connection		5.2	7.7			
		fSUB = 32.768 kHz Note 4 TA = +70°C		Normal operation	Square wave input		5.5	9.3			
					Resonator connection		5.6	9.4			
		fSUB = 32.768 kHz Note 4 TA = +85°C		Normal operation	Square wave input		6.2	13.3			
					Resonator connection		6.2	13.4			
		fSUB = 32.768 kHz Note 4 TA = +105°C	Normal operation	Square wave input		8.3	46.0				
				Resonator connection		8.4	46.0				

(Notes and Remarks are listed on the next page.)

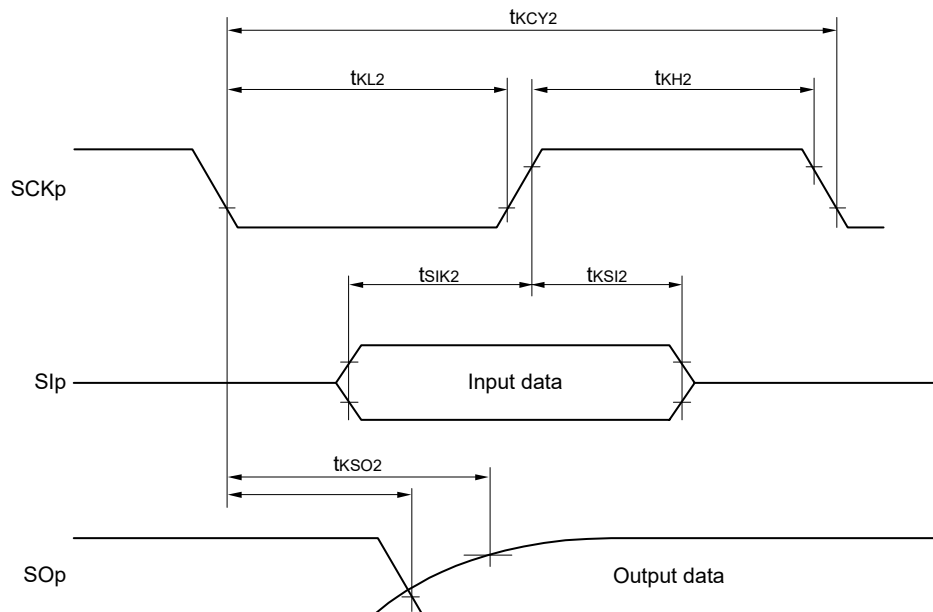
- Note 1.** Total current flowing into VDD, including the input leakage current flowing when the level of the input pin is fixed to VDD or VSS. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the LCD controller/driver, A/D converter, D/A converter, comparator, LVD circuit, USB 2.0 function module, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
- Note 2.** During HALT instruction execution by flash memory.
- Note 3.** When high-speed on-chip oscillator and subsystem clock are stopped.
- Note 4.** When high-speed system clock and subsystem clock are stopped.
- Note 5.** When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the real-time clock 2 is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.
- Note 6.** Not including the current flowing into the real-time clock 2, 12-bit interval timer, and watchdog timer.
- Note 7.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
 HS (high-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}@1\text{ MHz to }24\text{ MHz}$
 $2.4\text{ V} \leq V_{DD} \leq 3.6\text{ V}@1\text{ MHz to }16\text{ MHz}$
- Note 8.** Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.
- Remark 1.** fMX: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
- Remark 2.** fHOCO: High-speed on-chip oscillator clock frequency (48 MHz max.)
- Remark 3.** fIH: Main system clock source frequency when the high-speed on-chip oscillator clock divided 1, 2, 4, or 8, or the PLL clock divided by 2, 4, or 8 is selected (24 MHz max.)
- Remark 4.** fSUB: Subsystem clock frequency (XT1 clock oscillation frequency)
- Remark 5.** Except subsystem clock operation, temperature condition of the TYP. value is TA = 25°C

(TA = -40 to +105°C, 2.4 V ≤ VDD ≤ 3.6 V, VSS = 0 V)

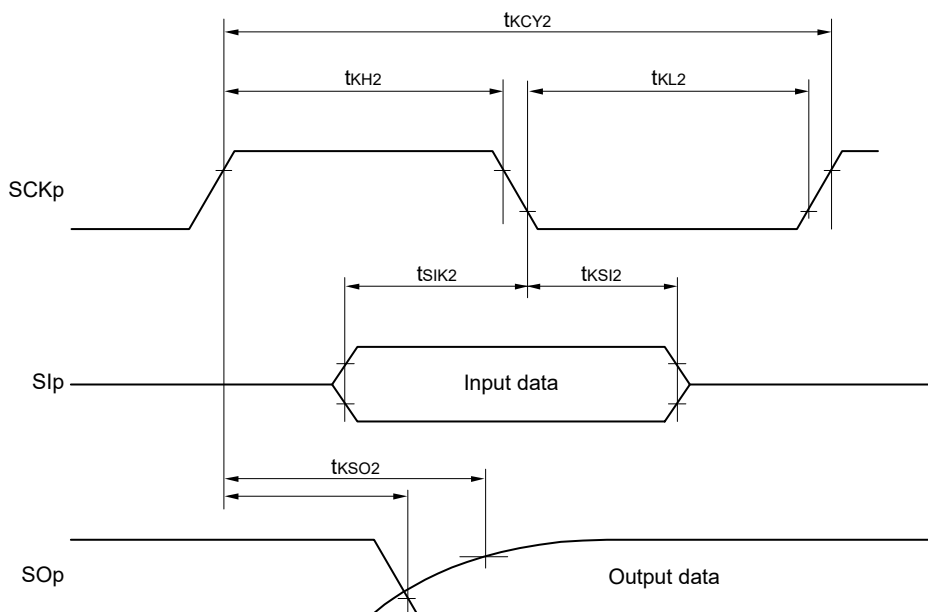
Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Low-speed on-chip oscillator operating current	IFIL Note 1						0.20		μA
RTC2 operating current	IRTC Notes 1, 3						0.02		μA
12-bit interval timer operating current	ITMKA Notes 1, 2, 4						0.02		μA
Watchdog timer operating current	IWDTC Notes 1, 2, 5	fIL = 15 kHz					0.22		μA
A/D converter operating current	IADC Notes 6, 7	AVDD = 3.0 V, when conversion at maximum speed					422	720	μA
AVREF (+) current	IAVREF Note 8	AVDD = 3.0 V, ADREFP1 = 0, ADREFP0 = 0 Note 7					14.0	25.0	μA
		AVREFP = 3.0 V, ADREFP1 = 0, ADREFP0 = 1 Note 10					14.0	25.0	
		ADREFP1 = 1, ADREFP0 = 0 Note 1					14.0	25.0	
A/D converter reference voltage current	IADREF Notes 1, 9	VDD = 3.0 V					75.0		μA
Temperature sensor operating current	ITMPS Note 1						78		μA
D/A converter operating current	IDAC Notes 1, 11	Per D/A converter channel					0.53	1.5	mA
Comparator operating current	ICMP Notes 1, 12	VDD = 3.6 V, Regulator output voltage = 2.1 V	Window mode				12.5		μA
			Comparator high-speed mode				4.5		μA
			Comparator low-speed mode				1.2		μA
LVD operating current	ILVD Notes 1, 13						0.06		μA
Self-programming operating current	IFSP Notes 1, 14						2.50	12.20	mA
BGO operating current	IBGO Notes 1, 15						1.68	12.20	mA
SNOOZE operating current	ISNOZ Note 1	ADC operation	The mode is performed Note 16				0.34	1.10	mA
			The A/D conversion operations are performed, Low voltage mode, AVREFP = VDD = 3.0 V				0.53	2.04	
		CSI/UART operation					0.70	1.54	mA
LCD operating current	ILCD1 Notes 17, 18	External resistance division method	fLCD = fSUB LCD clock = 128 Hz	1/3 bias 4-time slice	VDD = 3.6 V, LV4 = 3.6 V		0.14		μA
	ILCD2 Note 17	Internal voltage boosting method	fLCD = fSUB LCD clock = 128 Hz	1/3 bias 4-time slice	VDD = 3.0 V, LV4 = 3.0 V (VLCD = 04H)		0.61		μA
	ILCD3 Note 17	Capacitor split method	fLCD = fSUB LCD clock = 128 Hz	1/3 bias 4-time slice	VDD = 3.0 V, LV4 = 3.0 V		0.12		μA
USB current Note 19	IUSB Note 20	Operating current during USB communication					4.88		mA
	IUSB Note 21	Operating current in the USB suspended state					0.04		mA

(Notes and Remarks are listed on the next page.)

CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark p: CSI number (p = 00, 10, 20, 30), m: Unit number (m = 0, 1),
n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0 to 3)

3.5.2 Serial interface IICA

($T_A = -40$ to $+105^{\circ}\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	HS (high-speed main) Mode				Unit
			Standard mode		Fast mode		
			MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	fSCL	Fast mode: fCLK ≥ 3.5 MHz	—	—	0	400	kHz
		Standard mode: fCLK ≥ 1 MHz	0	100	—	—	kHz
Setup time of restart condition	tSU: STA		4.7		0.6		μs
Hold time ^{Note 1}	tHD: STA		4.0		0.6		μs
Hold time when SCLA0 = “L”	tLOW		4.7		1.3		μs
Hold time when SCLA0 = “H”	tHIGH		4.0		0.6		μs
Data setup time (reception)	tSU: DAT		250		100		ns
Data hold time (transmission) ^{Note 2}	tHD: DAT		0	3.45	0	0.9	μs
Setup time of stop condition	tSU: STO		4.0		0.6		μs
Bus-free time	tBUF		4.7		1.3		μs

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.

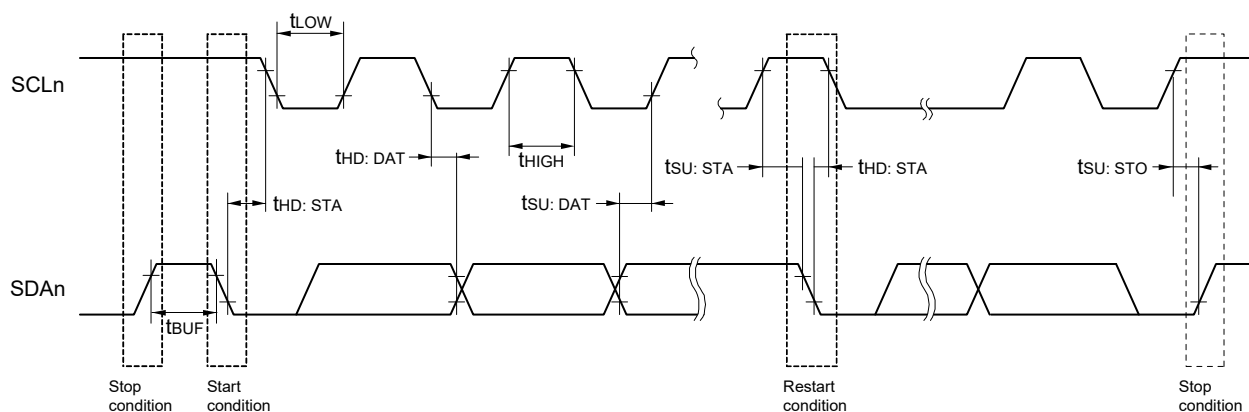
Note 2. The maximum value (MAX.) of tHD:DAT is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: $C_b = 400\text{ pF}$, $R_b = 2.7\text{ k}\Omega$

Fast mode: $C_b = 320\text{ pF}$, $R_b = 1.1\text{ k}\Omega$

IICA serial transfer timing



(3) BC option standard**($T_A = -40$ to $+105^\circ\text{C}$, $4.35\text{ V} \leq \text{UVBUS} \leq 5.25\text{ V}$, $2.4\text{ V} \leq \text{VDD} \leq 3.6$, $\text{VSS} = 0\text{ V}$)**

Parameter			Symbol	Conditions	MIN.	TYP.	MAX.	Unit
UDP/UDM input reference voltage (UVBUS divider ratio) (Function)	VDSELi [3: 0] (i = 0, 1)	0000	VDDDET0		27	32	37	%UVBUS
		0001	VDDDET1		29	34	39	%UVBUS
		0010	VDDDET2		32	37	42	%UVBUS
		0011	VDDDET3		35	40	45	%UVBUS
		0100	VDDDET4		38	43	48	%UVBUS
		0101	VDDDET5		41	46	51	%UVBUS
		0110	VDDDET6		44	49	54	%UVBUS
		0111	VDDDET7		47	52	57	%UVBUS
		1000	VDDDET8		51	56	61	%UVBUS
		1001	VDDDET9		55	60	65	%UVBUS
		1010	VDDDET10		59	64	69	%UVBUS
		1011	VDDDET11		63	68	73	%UVBUS
		1100	VDDDET12		67	72	73	%UVBUS
		1101	VDDDET13		71	76	81	%UVBUS
		1110	VDDDET14		75	80	85	%UVBUS
		1111	VDDDET15		79	84	89	%UVBUS

- (5) When reference voltage (+) = Internal reference voltage (1.45 V) (ADREFP1 = 1, ADREFP0 = 0), reference voltage (-) = AVss (ADREFM = 0), conversion target: ANI0 to ANI6, ANI16 to ANI21

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $2.4\text{ V} \leq V_{DD}$, $2.4\text{ V} \leq AV_{DD} = V_{DD}$, $V_{SS} = 0\text{ V}$, $AV_{SS} = 0\text{ V}$,

Reference voltage (+) = internal reference voltage, Reference voltage (-) = AVss = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES		8			bit
Conversion time	tCONV	8-bit resolution	16.0			μs
Zero-scale error ^{Note}	EZS	8-bit resolution			± 4.0	LSB
Integral linearity error ^{Note}	ILE	8-bit resolution			± 2.0	LSB
Differential linearity error ^{Note}	DLE	8-bit resolution			± 2.5	LSB
Reference voltage (+)	AVREF(+)	= Internal reference voltage (VBGR)	1.38	1.45	1.5	V
Analog input voltage	VAIN		0		VBGR	V

Note Excludes quantization error ($\pm 1/2$ LSB).

Caution Always use AVDD pin with the same potential as the VDD pin.

3.6.2 Temperature sensor, internal reference voltage output characteristics

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $V_{SS} = 0\text{ V}$ (HS (high-speed main) mode))

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	VTMPS25	Setting ADS register = 80H, $T_A = +25^\circ\text{C}$		1.05		V
Internal reference voltage	VBGR	Setting ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	FVTMPS	Temperature sensor output voltage that depends on the temperature		-3.6		$\text{mV}/^\circ\text{C}$
Operation stabilization wait time	tAMP		10			μs

3.6.3 D/A converter characteristics

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES					8	bit
Overall error	AINL	Rload = 4 M Ω	$2.4\text{ V} \leq V_{DD} \leq 3.6\text{ V}$			± 2.5	LSB
		Rload = 8 M Ω	$2.4\text{ V} \leq V_{DD} \leq 3.6\text{ V}$			± 2.5	LSB
Settling time	tSET	Cload = 20 pF	$2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$			3	μs
			$2.4\text{ V} \leq V_{DD} < 2.7\text{ V}$			6	μs

REVISION HISTORY	RL78/L1C Datasheet
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Rev.	Date	Description	
		Page	Summary
0.01	Oct 15, 2012	—	First Edition issued
1.00	Nov 18, 2013	1, 2	Modification of 1.1 Features
		3, 4	Modification of 1.2 Ordering Information
		5 to 8	Modification of package type in 1.3 Pin Configuration (Top View)
		14 to 17	Modification of vectored interrupt sources in 1.6 Outline of Functions
		14 to 17	Modification of operating ambient temperature in 1.6 Outline of Functions
		19 to 21	Modification of description in tables in 2.1 Absolute Maximum Ratings
		22, 23	Modification of description in 2.2 Oscillator Characteristics
		25	Modification of low-level output current in 2.3.1 Pin characteristics
		26	Modification of error of high-level input voltage conditions in 2.3.1 Pin characteristics
		26	Modification of error of low-level input voltage conditions in 2.3.1 Pin characteristics
		27	Modification of low-level output voltage in 2.3.1 Pin characteristics
		28	Modification of error of internal pull-up resistor conditions in 2.3.1 Pin characteristics
		29 to 34	Modification of 2.3.2 Supply current characteristics
		35, 36	Modification of 2.4 AC Characteristics
		37, 38	Addition of minimum instruction execution time during main system clock operation
		41 to 63	Addition of LS mode and LV mode characteristics in 2.5.1 Serial array unit
		64 to 66	Addition of LS mode and LV mode characteristics in 2.5.2 Serial interface IICA
		67, 68	Modification of conditions in 2.5.3 USB
		69	Addition of (3) BC option standard in 2.5.3 USB
		70 to 75	Addition of characteristics about conversion of internal reference voltage and temperature sensor in 2.6.1 A/D converter characteristics
		76	Addition of characteristic in 2.6.4 Comparator
		76	Deletion of detection delay in 2.6.5 POR circuit characteristics
		78	Modification of 2.7 Power supply voltage rising slope characteristics
		79 to 82	Modification of 2.8 LCD Characteristics
		83	Modification of 2.9 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics
		83	Modification of 2.10 Flash Memory Programming Characteristics
		84	Addition of 2.12 Timing Specs for Switching Modes
		85 to 144	Addition of 3. ELECTRICAL SPECIFICATIONS (G: TA = -40 to +105°C)
2.00	Feb 21, 2014	All	Addition of 85-pin product information
		All	Modification from 80-pin to 80/85-pin
		All	Modification from x = M, P to x = M, N, P
		All	Modification from high-accuracy real-time clock to real-time clock 2
		All	Modification from RTC to RTC2
		1	Modification of 1.1 Features
		3	Modification of 1.2 Ordering Information