Renesas Electronics America Inc - R5F111NJALA#U0 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	55
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 11x8/12b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	85-VFLGA
Supplier Device Package	85-VFLGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f111njala-u0

1.2 Ordering Information

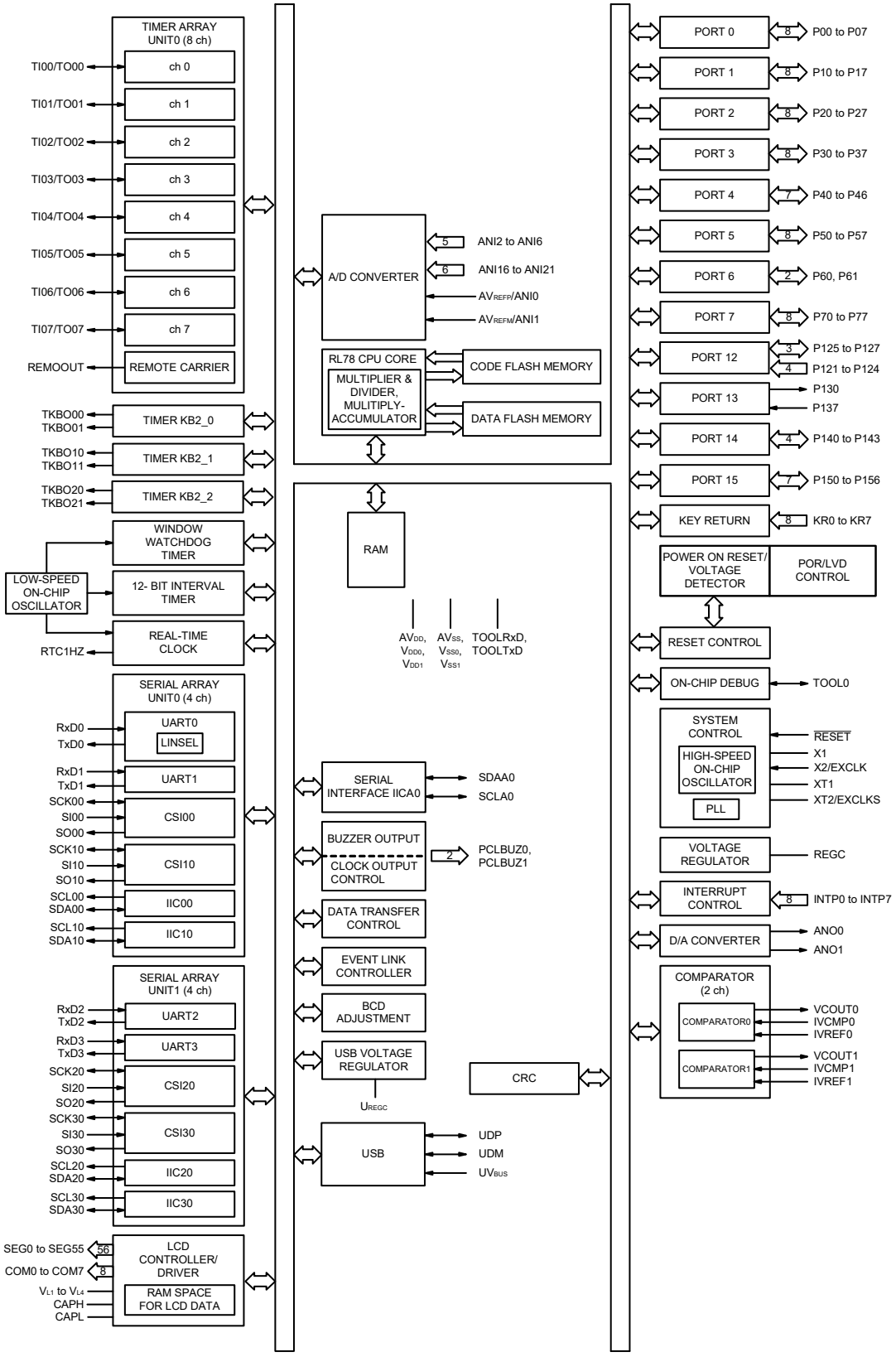
Products with USB

Pin Count	Package	Fields of Application	Orderable Part Number
80 pins	80-pin plastic LFQFP (12 × 12 mm, 0.5 mm pitch)	A	R5F110MEAFB#30, R5F110MFAFB#30, R5F110MGAFB#30, R5F110MHAFB#30, R5F110MJAFB#30 R5F110MEAFB#50, R5F110MFAFB#50, R5F110MGAFB#50, R5F110MHAFB#50, R5F110MJAFB#50
		G	R5F110MEGFB#30, R5F110MFGFB#30, R5F110MGGFB#30, R5F110MHGFB#30, R5F110MJGFB#30 R5F110MEGFB#50, R5F110MFGFB#50, R5F110MGGFB#50, R5F110MHGFB#50, R5F110MJGFB#50
85 pins	85-pin plastic VFLGA (7 × 7 mm, 0.65 mm pitch)	A	R5F110NEALA#U0, R5F110NFALA#U0, R5F110NGALA#U0, R5F110NHALA#U0, R5F110NJALA#U0 R5F110NEALA#W0, R5F110NFALA#W0, R5F110NGALA#W0, R5F110NHALA#W0, R5F110NJALA#W0
		G	R5F110NEGLA#U0, R5F110NFGLA#U0, R5F110NGGLA#U0, R5F110NHGLA#U0, R5F110NJGLA#U0 R5F110NEGLA#W0, R5F110NFGLA#W0, R5F110NGGLA#W0, R5F110NHGLA#W0, R5F110NJGLA#W0
100 pins	100-pin plastic LFQFP (14 × 14 mm, 0.5 mm pitch)	A	R5F110PEAFB#30, R5F110PFAFB#30, R5F110PGAFB#30, R5F110PHAFB#30, R5F110PJAFB#30 R5F110PEAFB#50, R5F110PFAFB#50, R5F110PGAFB#50, R5F110PHAFB#50, R5F110PJAFB#50
		G	R5F110PEGFB#30, R5F110PFGFB#30, R5F110PGGFB#30, R5F110PHGFB#30, R5F110PJGFB#30 R5F110PEGFB#50, R5F110PFGFB#50, R5F110PGGFB#50, R5F110PHGFB#50, R5F110PJGFB#50

Products without USB

Pin Count	Package	Fields of Application	Orderable Part Number
80 pins	80-pin plastic LFQFP (12 × 12 mm, 0.5 mm pitch)	A	R5F111MEAFB#30, R5F111MFAFB#30, R5F111MGAFB#30, R5F111MHAFB#30, R5F111MJAFB#30 R5F111MEAFB#50, R5F111MFAFB#50, R5F111MGAFB#50, R5F111MHAFB#50, R5F111MJAFB#50
		G	R5F111MEGFB#30, R5F111MFGFB#30, R5F111MGGFB#30, R5F111MHGFB#30, R5F111MJGFB#30 R5F111MEGFB#50, R5F111MFGFB#50, R5F111MGGFB#50, R5F111MHGFB#50, R5F111MJGFB#50
85 pins	85-pin plastic VFLGA (7 × 7 mm, 0.65 mm pitch)	A	R5F111NEALA#U0, R5F111NFALA#U0, R5F111NGALA#U0, R5F111NHALA#U0, R5F111NJALA#U0 R5F111NEALA#W0, R5F111NFALA#W0, R5F111NGALA#W0, R5F111NHALA#W0, R5F111NJALA#W0
		G	R5F111NEGLA#U0, R5F111NFGLA#U0, R5F111NGGLA#U0, R5F111NHGLA#U0, R5F111NJGLA#U0 R5F111NEGLA#W0, R5F111NFGLA#W0, R5F111NGGLA#W0, R5F111NHGLA#W0, R5F111NJGLA#W0
100 pins	100-pin plastic LFQFP (14 × 14 mm, 0.5 mm pitch)	A	R5F111PEAFB#30, R5F111PFAFB#30, R5F111PGAFB#30, R5F111PHAFB#30, R5F111PJAFB#30 R5F111PEAFB#50, R5F111PFAFB#50, R5F111PGAFB#50, R5F111PHAFB#50, R5F111PJAFB#50
		G	R5F111PEGFB#30, R5F111PFGFB#30, R5F111PGGFB#30, R5F111PHGFB#30, R5F111PJGFB#30 R5F111PEGFB#50, R5F111PFGFB#50, R5F111PGGFB#50, R5F111PHGFB#50, R5F111PJGFB#50

1.5.3 100-pin products (with USB)



2.3.2 Supply current characteristics

(T_A = -40 to +85°C, 1.6 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V) **(1/2)**

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD1}	Operating mode	HS (high-speed main) mode Note 5	f_{HOCO} = 48 MHz Note 3, f_{IH} = 24 MHz Note 3	Basic operation	V_{DD} = 3.6 V		2.2	2.8	mA
						V_{DD} = 3.0 V		2.2	2.8	
					Normal operation	V_{DD} = 3.6 V		4.4	8.5	
						V_{DD} = 3.0 V		4.4	8.5	
				f_{HOCO} = 24 MHz Note 3, f_{IH} = 24 MHz Note 3	Basic operation	V_{DD} = 3.6 V		2.0	2.6	
						V_{DD} = 3.0 V		2.0	2.6	
					Normal operation	V_{DD} = 3.6 V		4.2	6.8	
						V_{DD} = 3.0 V		4.2	6.8	
				f_{HOCO} = 16 MHz Note 3, f_{IH} = 16 MHz Note 3	Normal operation	V_{DD} = 3.6 V		3.1	4.9	
						V_{DD} = 3.0 V		3.1	4.9	
			LS (low-speed main) mode Note 5	f_{HOCO} = 8 MHz Note 3, f_{IH} = 8 MHz Note 3	Normal operation	V_{DD} = 3.0 V		1.4	2.2	mA
						V_{DD} = 2.0 V		1.4	2.2	
			LV (low-voltage main) mode Note 5	f_{HOCO} = 4 MHz Note 3, f_{IH} = 4 MHz Note 3	Normal operation	V_{DD} = 3.0 V		1.3	1.8	mA
						V_{DD} = 2.0 V		1.3	1.8	
			HS (high-speed main) mode Note 5	f_{MX} = 20 MHz Note 2, V_{DD} = 3.6 V	Normal operation	Square wave input		3.5	5.5	mA
						Resonator connection		3.6	5.7	
				f_{MX} = 20 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		3.5	5.5	
						Resonator connection		3.6	5.7	
				f_{MX} = 16 MHz Note 2, V_{DD} = 3.6 V	Normal operation	Square wave input		2.9	4.5	
						Resonator connection		3.1	4.6	
				f_{MX} = 16 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		2.9	4.5	
						Resonator connection		3.1	4.6	
				f_{MX} = 10 MHz Note 2, V_{DD} = 3.6 V	Normal operation	Square wave input		2.1	3.2	
						Resonator connection		2.2	3.2	
				f_{MX} = 10 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		2.1	3.2	
						Resonator connection		2.2	3.2	
			LS (low-speed main) mode Note 5	f_{MX} = 8 MHz Note 2, V_{DD} = 3.6 V	Normal operation	Square wave input		1.2	2.0	mA
						Resonator connection		1.3	2.0	
				f_{MX} = 8 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		1.2	2.1	
						Resonator connection		1.3	2.2	
			HS (High-speed main) mode (PLL operation)	f_{PLL} = 48 MHz, f_{CLK} = 24 MHz Note 2	Normal operation	V_{DD} = 3.6 V		4.7	7.5	mA
						V_{DD} = 3.0 V		4.7	7.5	
				f_{PLL} = 48 MHz, f_{CLK} = 12 MHz Note 2	Normal operation	V_{DD} = 3.6 V		3.1	5.1	
						V_{DD} = 3.0 V		3.1	5.1	
				f_{PLL} = 48 MHz, f_{CLK} = 6 MHz Note 2	Normal operation	V_{DD} = 3.6 V		2.3	3.9	
						V_{DD} = 3.0 V		2.3	3.9	
			Subsystem clock operation	f_{SUB} = 32.768 kHz Note 4 T_A = -40°C	Normal operation	Square wave input		4.6	6.9	μA
						Resonator connection		4.7	6.9	
				f_{SUB} = 32.768 kHz Note 4 T_A = +25°C	Normal operation	Square wave input		4.9	7.0	
						Resonator connection		5.0	7.2	
				f_{SUB} = 32.768 kHz Note 4 T_A = +50°C	Normal operation	Square wave input		5.2	7.6	
						Resonator connection		5.2	7.7	
				f_{SUB} = 32.768 kHz Note 4 T_A = +70°C	Normal operation	Square wave input		5.5	9.3	
						Resonator connection		5.6	9.4	
				f_{SUB} = 32.768 kHz Note 4 T_A = +85°C	Normal operation	Square wave input		6.2	13.3	
						Resonator connection		6.2	13.4	

(**Notes** and **Remarks** are listed on the next page.)

(3) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)

(T_A = -40 to +85°C, 1.6 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq f_{CLK}/4$	2.7 V ≤ V_{DD} ≤ 3.6 V	167		500		1000		ns
			2.4 V ≤ V_{DD} ≤ 3.6 V	250		500		1000		ns
			1.8 V ≤ V_{DD} ≤ 3.6 V	—		500		1000		ns
			1.6 V ≤ V_{DD} ≤ 3.6 V	—		—		1000		ns
SCKp high-/low-level width	t_{KH1}, t_{KL1}	2.7 V ≤ V_{DD} ≤ 3.6 V		t_{KCY1}/2 - 18		t_{KCY1}/2 - 50		t_{KCY1}/2 - 50		ns
		2.4 V ≤ V_{DD} ≤ 3.6 V		t_{KCY1}/2 - 38		t_{KCY1}/2 - 50		t_{KCY1}/2 - 50		ns
		1.8 V ≤ V_{DD} ≤ 3.6 V		—		t_{KCY1}/2 - 50		t_{KCY1}/2 - 50		ns
		1.6 V ≤ V_{DD} ≤ 3.6 V		—		—		t_{KCY1}/2 - 100		ns
SIp setup time (to SCKp↑) Note 1	t_{SIK1}	2.7 V ≤ V_{DD} ≤ 3.6 V		44		110		110		ns
		2.4 V ≤ V_{DD} ≤ 3.6 V		75		110		110		ns
		1.8 V ≤ V_{DD} ≤ 3.6 V		—		110		110		ns
		1.6 V ≤ V_{DD} ≤ 3.6 V		—		—		220		ns
SIp hold time (from SCKp↑) Note 2	t_{KSI1}	2.4 V ≤ V_{DD} ≤ 3.6 V		19		19		19		ns
		1.8 V ≤ V_{DD} ≤ 3.6 V		—		19		19		ns
		1.6 V ≤ V_{DD} ≤ 3.6 V		—		—		19		ns
Delay time from SCKp↓ to SOp output Note 3	t_{KSO1}	C = 30 pF Note 4	2.7 V ≤ V_{DD} ≤ 3.6 V		25		50		50	ns
			2.4 V ≤ V_{DD} ≤ 3.6 V		25		50		50	ns
			1.8 V ≤ V_{DD} ≤ 3.6 V		—		50		50	ns
			1.6 V ≤ V_{DD} ≤ 3.6 V		—		—		50	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

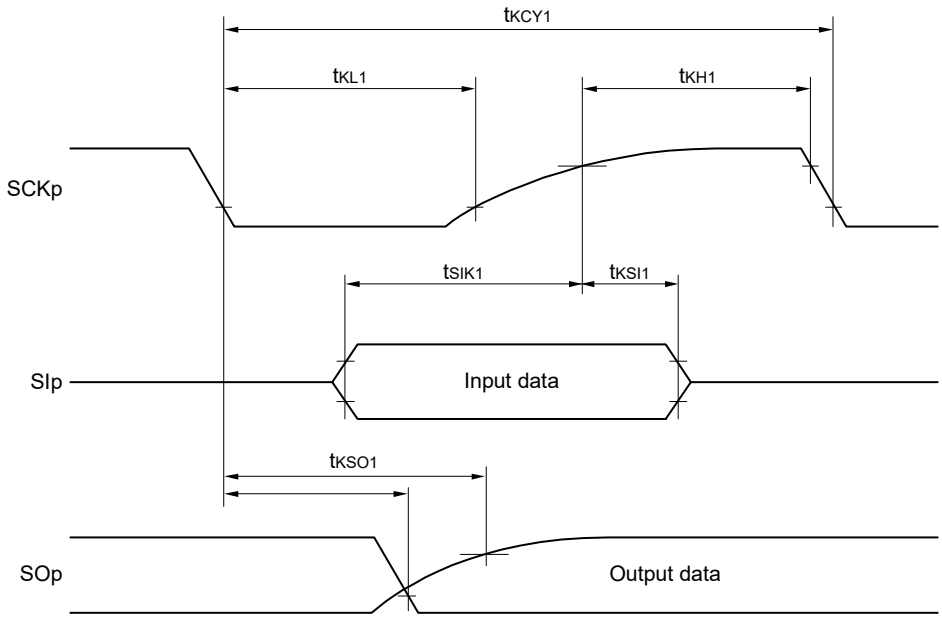
Note 4. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

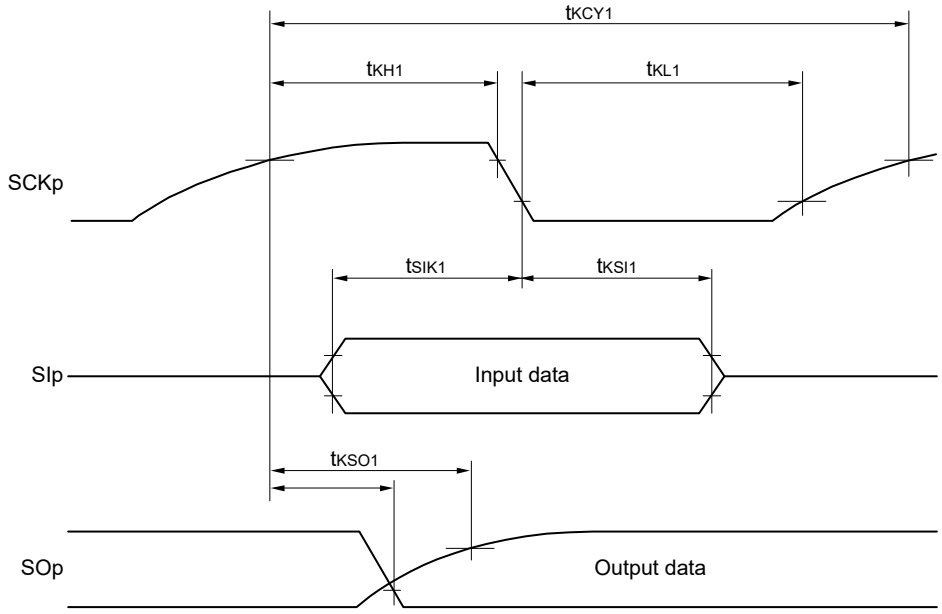
Remark 1. p: CSI number (p = 00, 10, 20, 30), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM number (g = 0 to 3)

Remark 2. f_{MCK}: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark p: CSI number (p = 00, 10, 20, 30), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),
g: PIM and POM number (g = 0 to 3)

(2) I^2C fast mode

(T_A = -40 to +85°C, 1.8 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Fast mode: f_{CLK} ≥ 3.5 MHz	2.7 V ≤ V_{DD} ≤ 3.6 V	0	400	0	400	0	400	kHz
			1.8 V ≤ V_{DD} ≤ 3.6 V	0	400	0	400	0	400	kHz
Setup time of restart condition	$t_{SU: STA}$	2.7 V ≤ V_{DD} ≤ 3.6 V		0.6		0.6		0.6		μs
		1.8 V ≤ V_{DD} ≤ 3.6 V		0.6		0.6		0.6		μs
Hold time Note 1	$t_{HD: STA}$	2.7 V ≤ V_{DD} ≤ 3.6 V		0.6		0.6		0.6		μs
		1.8 V ≤ V_{DD} ≤ 3.6 V		0.6		0.6		0.6		μs
Hold time when SCLA0 = "L"	t_{LOW}	2.7 V ≤ V_{DD} ≤ 3.6 V		1.3		1.3		1.3		μs
		1.8 V ≤ V_{DD} ≤ 3.6 V		1.3		1.3		1.3		μs
Hold time when SCLA0 = "H"	t_{HIGH}	2.7 V ≤ V_{DD} ≤ 3.6 V		0.6		0.6		0.6		μs
		1.8 V ≤ V_{DD} ≤ 3.6 V		0.6		0.6		0.6		μs
Data setup time (reception)	$t_{SU: DAT}$	2.7 V ≤ V_{DD} ≤ 3.6 V		100		100		100		ns
		1.8 V ≤ V_{DD} ≤ 3.6 V		100		100		100		ns
Data hold time (transmission) Note 2	$t_{HD: DAT}$	2.7 V ≤ V_{DD} ≤ 3.6 V		0	0.9	0	0.9	0	0.9	μs
		1.8 V ≤ V_{DD} ≤ 3.6 V		0	0.9	0	0.9	0	0.9	μs
Setup time of stop condition	$t_{SU: STO}$	2.7 V ≤ V_{DD} ≤ 3.6 V		0.6		0.6		0.6		μs
		1.8 V ≤ V_{DD} ≤ 3.6 V		0.6		0.6		0.6		μs
Bus-free time	t_{BUF}	2.7 V ≤ V_{DD} ≤ 3.6 V		1.3		1.3		1.3		μs
		1.8 V ≤ V_{DD} ≤ 3.6 V		1.3		1.3		1.3		μs

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.

Note 2. The maximum value (MAX.) of $t_{HD: DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.
Fast mode: C_b = 320 pF, R_b = 1.1 kΩ

2.6 Analog Characteristics

2.6.1 A/D converter characteristics

Classification of A/D converter characteristics

Reference Voltage / Input Channel	Reference voltage (+) = AV_{REFP} Reference voltage (-) = AV_{REFM}	Reference voltage (+) = AV_{DD} Reference voltage (-) = AV_{SS}	Reference voltage (+) = Internal reference voltage Reference voltage (-) = AV_{SS}
High-accuracy channel; ANI0 to ANI6 (input buffer power supply: AV_{DD})	Refer to **2.6.1 (1)**. Refer to **2.6.1 (2)**.	Refer to **2.6.1 (3)**.	Refer to **2.6.1 (6)**.
Standard channel; ANI16 to ANI21 (input buffer power supply: V_{DD})	Refer to **2.6.1 (4)**.	Refer to **2.6.1 (5)**.	
Internal reference voltage, Temperature sensor output voltage	Refer to **2.6.1 (4)**.	Refer to **2.6.1 (5)**.	—

(1) When reference voltage (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AV_{REFM}/ANI1 (ADREFM = 1), target for conversion: ANI2 to ANI6

(T_A = -40 to +85°C, 2.4 V ≤ AV_{REFP} ≤ AV_{DD} = V_{DD} ≤ 3.6 V, V_{SS} = 0 V, AV_{SS} = 0 V, reference voltage (+) = AV_{REFP}, reference voltage (-) = AV_{REFM} = 0 V, HALT mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES				12	bit
Overall error Notes 1, 2, 3	AINL	12-bit resolution		±1.7	±3.3	LSB
Conversion time	tCONV	ADTYP = 0, 12-bit resolution	3.375			μs
Zero-scale error Notes 1, 2, 3	EZS	12-bit resolution		±1.3	±3.2	LSB
Full-scale error Notes 1, 2, 3	EFS	12-bit resolution		±0.7	±2.9	LSB
Integral linearity error Notes 1, 2, 3	ILE	12-bit resolution		±1.0	±1.4	LSB
Differential linearity error Notes 1, 2, 3	DLE	12-bit resolution		±0.9	±1.2	LSB
Analog input voltage	VAIN		0		AV_{REFP}	V

Note 1. TYP. Value is the average value at AV_{DD} = AV_{REFP} = 3 V and T_A = 25°C. MAX. value is the average value ±3σ at normalized distribution.

Note 2. These values are the results of characteristic evaluation and are not checked for shipment.

Note 3. Excludes quantization error (±1/2 LSB).

Caution 1. Route the wiring so that noise will not be superimposed on each power line and ground line, and insert a capacitor to suppress noise.
In addition, separate the reference voltage line of AV_{REFP} from the other power lines to keep it free from the influences of noise.

Caution 2. During A/D conversion, keep a pulse, such as a digital signal, that abruptly changes its level from being input to or output from the pins adjacent to the converter pins and P150 to P156.

3.2 Oscillator Characteristics

3.2.1 X1 and XT1 oscillator characteristics

(T_A = -40 to +105°C, 2.4 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f_X) Note	Ceramic resonator/crystal resonator	2.7 V ≤ V_{DD} ≤ 3.6 V	1.0		20.0	MHz
		2.4 V ≤ V_{DD} < 2.7 V	1.0		16.0	
XT1 clock oscillation frequency (f_{XT}) Note	Crystal resonator		32	32.768	35	kHz

Note Indicates only permissible oscillator frequency ranges. Refer to **AC Characteristics** for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution **Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.**

Remark When using the X1 and XT1 oscillator, refer to **5.4 System Clock Oscillator** in the RL78/L1C User's Manual.

3.2.2 On-chip oscillator characteristics

(TA = -40 to +105°C, 2.4 V ≤ VDD ≤ 3.6 V, VSS = 0 V)

Oscillators	Parameters	Conditions	MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency Notes 1, 2	fHOCO		1		24	MHz
High-speed on-chip oscillator clock frequency accuracy		-20 to +85°C	-1.0		+1.0	%
		-40 to -20°C	-1.5		+1.5	%
		+85 to +105°C	-2.0		+2.0	%
Low-speed on-chip oscillator clock frequency	fIL			15		kHz
Low-speed on-chip oscillator clock frequency accuracy			-15		+15	%

Note 1. High-speed on-chip oscillator frequency is selected with bits 0 to 4 of the option byte (000C2H) and bits 0 to 2 of the HOCODIV register.

Note 2. This only indicates the oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

3.2.3 PLL oscillator characteristics

(TA = -40 to +105°C, 2.4 V ≤ VDD ≤ 3.6 V, VSS = 0 V)

Oscillators	Parameters	Conditions	MIN.	TYP.	MAX.	Unit
PLL input frequency Note	fPLLIN	High-speed system clock	6.00		16.00	MHz
PLL output frequency Note	fPLL			48.00		MHz

Note Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

Note 1. Current flowing to V_{DD}.

Note 2. When high speed on-chip oscillator and high-speed system clock are stopped.

Note 3. Current flowing only to the real-time clock 2 (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2}, and I_{RTC}, when the real-time clock 2 operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added. I_{DD2} subsystem clock operation includes the operational current of the real-time clock 2.

Note 4. Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2}, and I_{TMKA}, when the 12-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added. I_{DD2} subsystem clock operation includes the operational current of the 12-bit interval timer.

Note 5. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The current value of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{WDT} when the watchdog timer operates in STOP mode.

Note 6. Current flowing only to the A/D converter. The supply current of the RL78 microcontrollers is the sum of I_{DD1} or I_{DD2} and I_{ADC}, I_{AVREF}, I_{ADREF} when the A/D converter operates in an operation mode or the HALT mode.

Note 7. Current flowing to the AV_{DD}.

Note 8. Current flowing from the reference voltage source of A/D converter.

Note 9. Operation current flowing to the internal reference voltage.

Note 10. Current flowing to the AV_{REFP}.

Note 11. Current flowing only to the D/A converter. The current value of the RL78 microcontrollers is the sum of I_{DD1} or I_{DD2} and I_{DA} when the D/A converter operates in an operation mode or the HALT mode.

Note 12. Current flowing only to the comparator circuit. The current value of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{CMP} when the comparator circuit operates in the Operating, HALT or STOP mode.

Note 13. Current flowing only to the LVD circuit. The current value of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{LVI} when the LVD circuit operates in the Operating, HALT or STOP mode.

Note 14. Current flowing only during self-programming.

Note 15. Current flowing only during data flash rewrite.

Note 16. For shift time to the SNOOZE mode, see **23.3.3 SNOOZE mode** in the RL78/L1C User's Manual..

Note 17. Current flowing only to the LCD controller/driver (V_{DD} pin). The current value of the RL78 microcontrollers is the sum of the LCD operating current (I_{LCD1}, I_{LCD2} or I_{LCD3}) to the supply current (I_{DD1}, or I_{DD2}) when the LCD controller/driver operates in an operation mode or HALT mode. Not including the current that flows through the LCD panel.

Note 18. Not including the current that flows through the external divider resistor divider resistor.

Note 19. Current flowing to the UV_{BUS}.

Note 20. Including the operating current when f_{PLL} = 48 MHz.

Note 21. Including the current supplied from the pull-up resistor of the UDP pin to the pull-down resistor of the host device, in addition to the current consumed by this MCU during the suspended state.

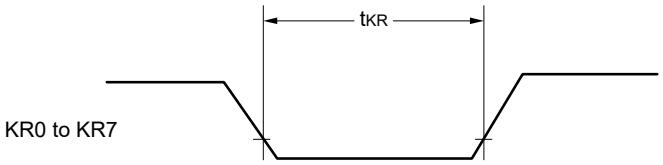
Remark 1. f_{IL}: Low-speed on-chip oscillator clock frequency

Remark 2. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

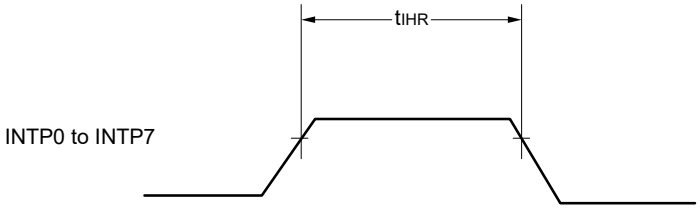
Remark 3. f_{CLK}: CPU/peripheral hardware clock frequency

Remark 4. Temperature condition of the TYP. value is T_A = 25°C

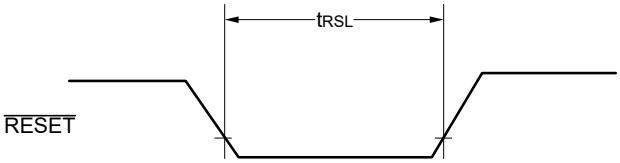
Key Interrupt Input Timing



Timer KB2 Input Timing



$\overline{\text{RESET}}$ Input Timing



(5) Communication at different potential (1.8 V, 2.5 V) (UART mode)

(T_A = -40 to +105°C, 2.4 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V) **(1/2)**

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
Transfer rate Notes 1, 2		Reception	2.7 V ≤ V_{DD} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V		f_{MCK}/12 Note 1	bps
			Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 4		2.0	Mbps
			1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V		f_{MCK}/12 Notes 1, 2, 3	bps
			Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 4		1.3	Mbps

Note 1. Transfer rate in the SNOOZE mode is 4,800 bps only.

Note 2. Use it with V_{DD} ≥ V_b.

Note 3. The following conditions are required for low voltage interface.
2.4 V ≤ V_{DD} < 2.7 V: MAX. 2.6 Mbps

Note 4. The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:
HS (high-speed main) mode: 24 MHz (2.7 V ≤ V_{DD} ≤ 3.6 V)
16 MHz (2.4 V ≤ V_{DD} ≤ 3.6 V)

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Remark 1. V_b[V]: Communication line voltage

Remark 2. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0 to 3)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

(6) Communication at different potential (1.8 V, 2.5 V) (CSI mode) (master mode, SCKp... internal clock output)

(T_A = -40 to +105°C, 2.4 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V) (2/2)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SIp setup time (to SCKp↑) Note 1	t_{SIK1}	2.7 V ≤ V_{DD} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	354		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3, C_b = 30 pF, R_b = 5.5 kΩ	958		ns
SIp hold time (from SCKp↑) Note 1	t_{KSI1}	2.7 V ≤ V_{DD} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	38		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3, C_b = 30 pF, R_b = 5.5 kΩ	38		ns
Delay time from SCKp↓ to SOp output Note 1	t_{KSO1}	2.7 V ≤ V_{DD} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		390	ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3, C_b = 30 pF, R_b = 5.5 kΩ		966	ns
SIp setup time (to SCKp↓) Note 2	t_{SIK1}	2.7 V ≤ V_{DD} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	88		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3, C_b = 30 pF, R_b = 5.5 kΩ	220		ns
SIp hold time (from SCKp↓) Note 2	t_{KSI1}	2.7 V ≤ V_{DD} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	38		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3, C_b = 30 pF, R_b = 5.5 kΩ	38		ns
Delay time from SCKp↑ to SOp output Note 2	t_{KSO1}	2.7 V ≤ V_{DD} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		50	ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3, C_b = 30 pF, R_b = 5.5 kΩ		50	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

Note 2. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. Use it with V_{DD} ≥ V_b.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(**Remarks** are listed on the next page.)

(8) Communication at different potential (1.8 V, 2.5 V) (simplified I^2C mode)

(T_A = -40 to +105°C, 2.4 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SCLr clock frequency	f_{SCL}	2.7 V ≤ V_{DD} ≤ 3.6 V, 2.3 V ≤ V_b < 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ		400 Note 1	kHz
		2.7 V ≤ V_{DD} ≤ 3.6 V, 2.3 V ≤ V_b < 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ		100 Note 1	kHz
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 100 pF, R_b = 5.5 kΩ		100 Note 1	kHz
Hold time when SCLr = "L"	t_{LOW}	2.7 V ≤ V_{DD} ≤ 3.6 V, 2.3 V ≤ V_b < 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	1200		ns
		2.7 V ≤ V_{DD} ≤ 3.6 V, 2.3 V ≤ V_b <2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	4600		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 100 pF, R_b = 5.5 kΩ	4650		ns
Hold time when SCLr = "H"	t_{HIGH}	2.7 V ≤ V_{DD} ≤ 3.6 V, 2.3 V ≤ V_b < 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	500		ns
		2.7 V ≤ V_{DD} ≤ 3.6 V, 2.3 V ≤ V_b < 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	2400		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 100 pF, R_b = 5.5 kΩ	1830		ns
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ V_{DD} ≤ 3.6 V, 2.3 V ≤ V_b < 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	1/f_{MCK} + 340 Note 3		ns
		2.7 V ≤ V_{DD} ≤ 3.6 V, 2.3 V ≤ V_b < 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	1/f_{MCK} + 760 Note 3		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 100 pF, R_b = 5.5 kΩ	1/f_{MCK} + 570 Note 3		ns
Data hold time (transmission)	$t_{HD:DAT}$	2.7 V ≤ V_{DD} ≤ 3.6 V, 2.3 V ≤ V_b < 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	0	770	ns
		2.7 V ≤ V_{DD} ≤ 3.6 V, 2.3 V ≤ V_b < 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	0	1420	ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 100 pF, R_b = 5.5 kΩ	0	1215	ns

Note 1. The value must be equal to or less than f_{MCK}/4.

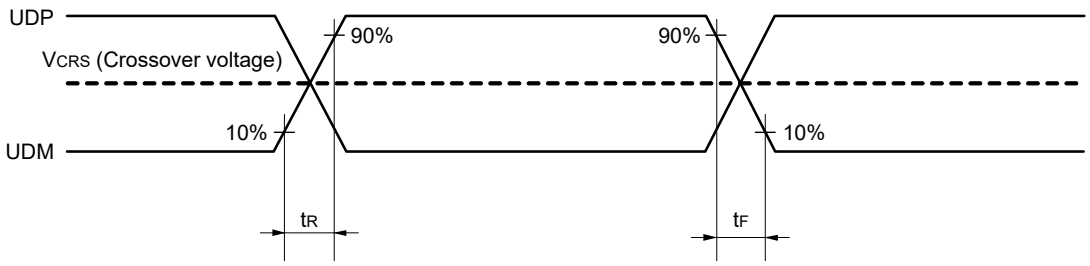
Note 2. Use it with V_{DD} ≥ V_b.

Note 3. Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance) mode for the SDAr pin and the N-ch open drain output (V_{DD} tolerance) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(**Remarks** are listed on the next page.)

Timing of UDP and UDM



(2) BC standard

(TA = -40 to +105°C, 4.35 V ≤ UVBUS ≤ 5.25 V, 2.4 V ≤ VDD ≤ 3.6 V, VSS = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
USB standard BC1.2	UDP sink current	IDP_SINK		25	100	175	μA
	UDM sink current	IDM_SINK		25	100	175	μA
	DCD source current	IDP_SRC		7	10	13	μA
	Data detection voltage	VDAT_REF		0.25	0.325	0.4	V
	UDP source voltage	VDP_SRC	Output current 250 μA	0.5	0.6	0.7	V
	UDM source voltage	VDM_SRC	Output current 250 μA	0.5	0.6	0.7	V

(4) When reference voltage (+) = AV_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (-) = AV_{SS} (ADREFM = 0), conversion target: ANI16 to ANI21, internal reference voltage, temperature sensor output voltage

(T_A = -40 to +105°C, 2.4 V ≤ V_{DD} ≤ 3.6 V, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 3.6 V, V_{SS} = 0 V, AV_{SS} = 0 V, Reference voltage (+) = AV_{DD}, Reference voltage (-) = AV_{SS} = 0)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES		2.4 V ≤ AV_{DD} ≤ 3.6 V	8		12	bit
Overall error Note 1	AINL	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±8.5	LSB
Conversion time	tCONV	ADTYP = 0, 12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V	4.125			µs
Zero-scale error Note 1	EZS	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±8.0	LSB
Full-scale error Note 1	EFS	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±8.0	LSB
Integral linearity error Note 1	ILE	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±3.5	LSB
Differential linearity error Note 1	DLE	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±2.5	LSB
Analog input voltage	VAIN			0		AV_{DD}	V
		Internal reference voltage (2.4 V ≤ V_{DD} ≤ 3.6 V, HS (high-speed main) mode)		V_{BGR} Note 2			
		Temperature sensor output voltage (2.4 V ≤ V_{DD} ≤ 3.6 V, HS (high-speed main) mode)		V_{TMP25} Note 2			

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. Refer to **3.6.2 Temperature sensor, internal reference voltage output characteristics**.

Caution Always use AV_{DD} pin with the same potential as the V_{DD} pin.

(5) When reference voltage (+) = Internal reference voltage (1.45 V) (ADREFP1 = 1, ADREFP0 = 0), reference voltage (-) = AVSS (ADREFM = 0), conversion target: ANI0 to ANI6, ANI16 to ANI21

(T_A = -40 to +105°C, 2.4 V ≤ V_{DD} ≤ 3.6 V, 2.4 V ≤ V_{DD}, 2.4 V ≤ AV_{DD} = V_{DD}, V_{SS} = 0 V, AV_{SS} = 0 V, Reference voltage (+) = internal reference voltage, Reference voltage (-) = AV_{SS} = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES			8		bit
Conversion time	tCONV	8-bit resolution	16.0			µs
Zero-scale error Note	EZS	8-bit resolution			±4.0	LSB
Integral linearity error Note	ILE	8-bit resolution			±2.0	LSB
Differential linearity error Note	DLE	8-bit resolution			±2.5	LSB
Reference voltage (+)	$AV_{REF(+)}$	= Internal reference voltage (V_{BGR})	1.38	1.45	1.5	V
Analog input voltage	VAIN		0		V_{BGR}	V

Note Excludes quantization error (±1/2 LSB).

Caution Always use AV_{DD} pin with the same potential as the V_{DD} pin.

3.6.2 Temperature sensor, internal reference voltage output characteristics

(T_A = -40 to +105°C, 2.4 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V (HS (high-speed main) mode))

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V_{TMPS25}	Setting ADS register = 80H, T_A = +25°C		1.05		V
Internal reference voltage	V_{BGR}	Setting ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	F_{VTMPS}	Temperature sensor output voltage that depends on the temperature		-3.6		mV/°C
Operation stabilization wait time	tAMP		10			µs

3.6.3 D/A converter characteristics

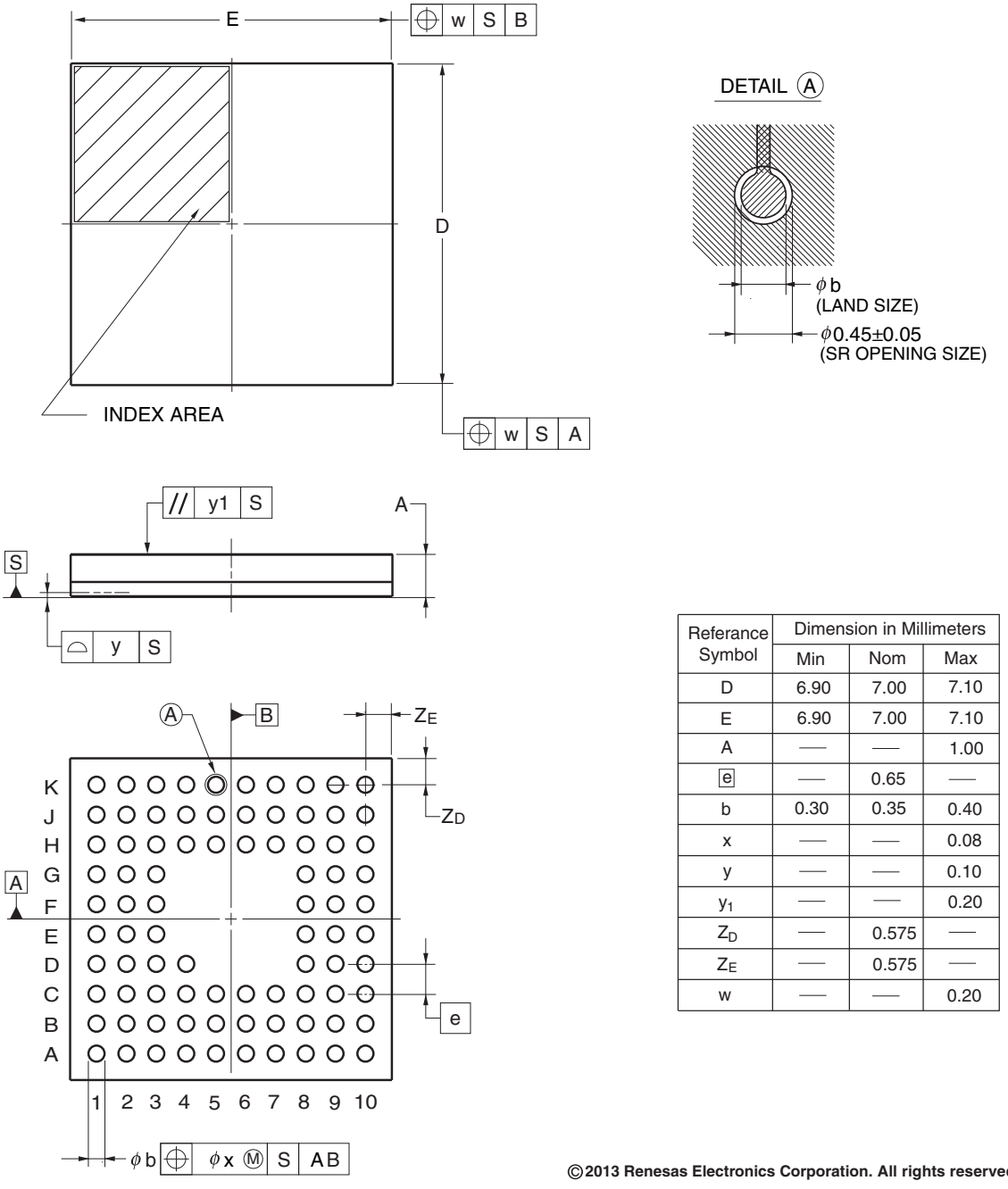
(T_A = -40 to +105°C, 2.4 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES					8	bit
Overall error	AINL	Rload = 4 MΩ	2.4 V ≤ V_{DD} ≤ 3.6 V			±2.5	LSB
		Rload = 8 MΩ	2.4 V ≤ V_{DD} ≤ 3.6 V			±2.5	LSB
Settling time	tSET	Cload = 20 pF	2.7 V ≤ V_{DD} ≤ 3.6 V			3	µs
			2.4 V ≤ V_{DD} < 2.7 V			6	µs

4.2 85-pin products

R5F110NEALA, R5F110NFALA, R5F110NGALA, R5F110NHALA, R5F110NJALA
R5F111NEALA, R5F111NFALA, R5F111NGALA, R5F111NHALA, R5F111NJALA
R5F110NEGLA, R5F110NFGLA, R5F110NGGLA, R5F110NHGLA, R5F110NJGLA
R5F111NEGLA, R5F111NFGLA, R5F111NGGLA, R5F111NHGLA, R5F111NJGLA

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-VFLGA85-7x7-0.65	PVLG0085JA-A	P85FC-65-BN4	0.1



Referance Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.90	7.00	7.10
E	6.90	7.00	7.10
A	—	—	1.00
e	—	0.65	—
b	0.30	0.35	0.40
x	—	—	0.08
y	—	—	0.10
y_1	—	—	0.20
Z_D	—	0.575	—
Z_E	—	0.575	—
w	—	—	0.20

REVISION HISTORY	RL78/L1C Datasheet

Rev.	Date	Description	
		Page	Summary
0.01	Oct 15, 2012	—	First Edition issued
1.00	Nov 18, 2013	1, 2	Modification of 1.1 Features
		3, 4	Modification of 1.2 Ordering Information
		5 to 8	Modification of package type in 1.3 Pin Configuration (Top View)
		14 to 17	Modification of vectored interrupt sources in 1.6 Outline of Functions
		14 to 17	Modification of operating ambient temperature in 1.6 Outline of Functions
		19 to 21	Modification of description in tables in 2.1 Absolute Maximum Ratings
		22, 23	Modification of description in 2.2 Oscillator Characteristics
		25	Modification of low-level output current in 2.3.1 Pin characteristics
		26	Modification of error of high-level input voltage conditions in 2.3.1 Pin characteristics
		26	Modification of error of low-level input voltage conditions in 2.3.1 Pin characteristics
		27	Modification of low-level output voltage in 2.3.1 Pin characteristics
		28	Modification of error of internal pull-up resistor conditions in 2.3.1 Pin characteristics
		29 to 34	Modification of 2.3.2 Supply current characteristics
		35, 36	Modification of 2.4 AC Characteristics
		37, 38	Addition of minimum instruction execution time during main system clock operation
		41 to 63	Addition of LS mode and LV mode characteristics in 2.5.1 Serial array unit
		64 to 66	Addition of LS mode and LV mode characteristics in 2.5.2 Serial interface IICA
		67, 68	Modification of conditions in 2.5.3 USB
		69	Addition of (3) BC option standard in 2.5.3 USB
		70 to 75	Addition of characteristics about conversion of internal reference voltage and temperature sensor in 2.6.1 A/D converter characteristics
		76	Addition of characteristic in 2.6.4 Comparator
		76	Deletion of detection delay in 2.6.5 POR circuit characteristics
		78	Modification of 2.7 Power supply voltage rising slope characteristics
		79 to 82	Modification of 2.8 LCD Characteristics
		83	Modification of 2.9 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics
		83	Modification of 2.10 Flash Memory Programming Characteristics
		84	Addition of 2.12 Timing Specs for Switching Modes
		85 to 144	Addition of 3. ELECTRICAL SPECIFICATIONS (G: T_A = -40 to +105°C)
2.00	Feb 21, 2014	All	Addition of 85-pin product information
		All	Modification from 80-pin to 80/85-pin
		All	Modification from x = M, P to x = M, N, P
		All	Modification from high-accuracy real-time clock to real-time clock 2
		All	Modification from RTC to RTC2
		1	Modification of 1.1 Features
		3	Modification of 1.2 Ordering Information

REVISION HISTORY	RL78/L1C Datasheet