Renesas Electronics America Inc - R5F111NJALA#W0 Datasheet

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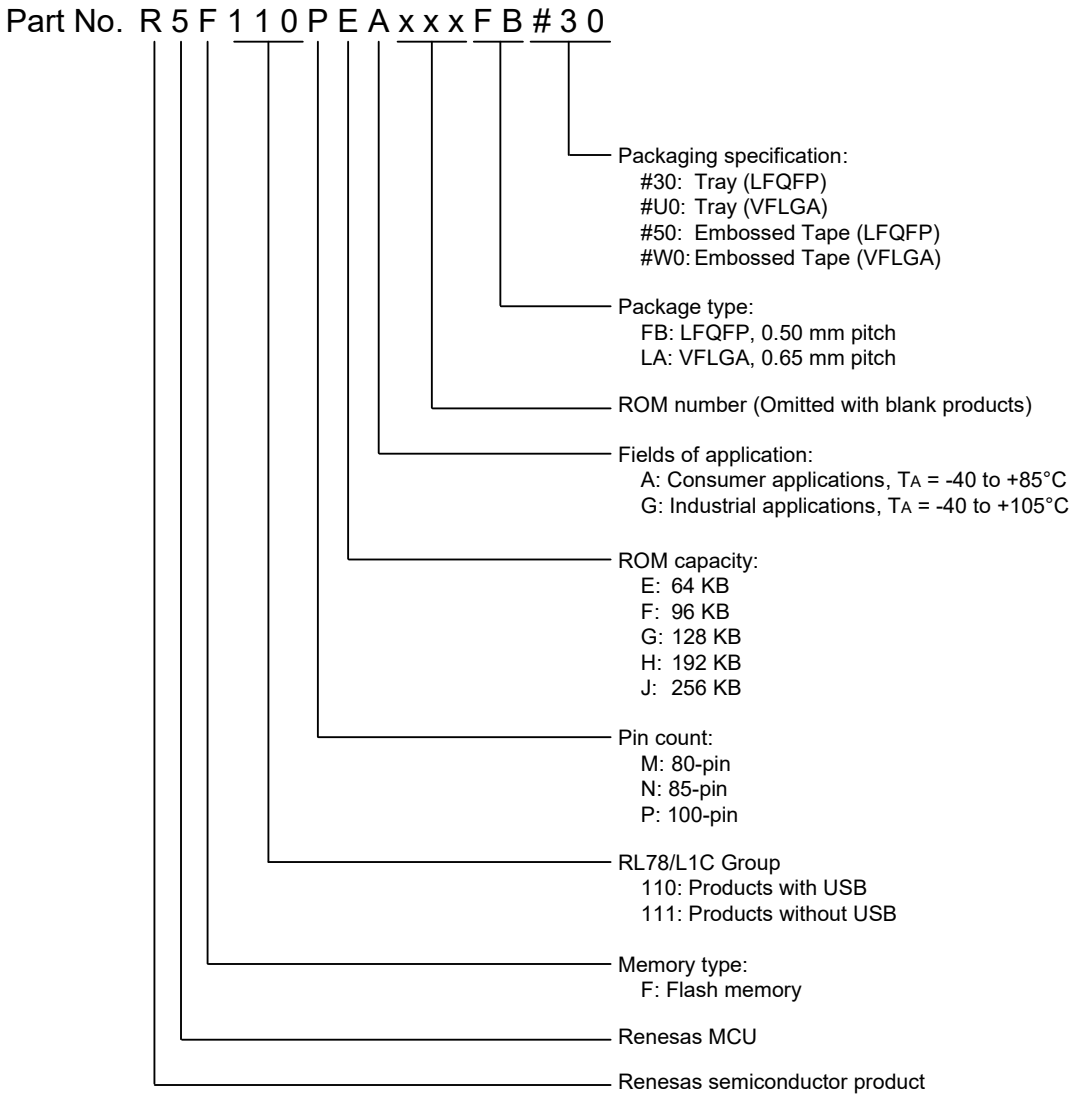
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	55
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 11x8/12b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	85-VFLGA
Supplier Device Package	85-VFLGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f111njala-w0

Figure 1 - 1 Part Number, Memory Size, and Package of RL78/L1C



Caution Orderable part numbers are current as of when this manual was published.
Please make sure to refer to the relevant product page on the Renesas website for the latest part numbers.

(2/2)

Item			80/85-pin	100-pin
			R5F110Mx/R5F110Nx (x = E to H, J)	R5F110Px (x = E to H, J)
Clock output/buzzer output			2	2
			• 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f_{MAIN} = 20 MHz operation) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: f_{SUB} = 32.768 kHz operation)	
8/12-bit resolution A/D converter			9 channels	13 channels
D/A converter			2 channels	2 channels
Comparator			1 channel	2 channels
Serial interface			• CSI: 1 channel/UART (UART supporting LIN-bus): 1 channel/simplified I^2C: 1 channel • CSI: 1 channel/UART: 1 channel/simplified I^2C: 1 channel • CSI: 1 channel/UART: 1 channel/simplified I^2C: 1 channel • CSI: 1 channel/UART: 1 channel/simplified I^2C: 1 channel	
	I^2C bus		1 channel	1 channel
USB	Function		1 channel	
LCD controller/driver			Internal voltage boosting method, capacitor split method, and external resistance division method are switchable.	
	Segment signal output		44 (40) Note 1	56 (52) Note 1
	Common signal output		4 (8) Note 1	
Data transfer controller (DTC)			32 sources	33 sources
Event link controller (ELC)			Event input: 30, Event trigger output: 22	Event input: 31, Event trigger output: 22
Vectored interrupt sources	Internal		36	37
	External		9	9
Key interrupt			8	8
Reset			• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution Note 2 • Internal reset by RAM parity error • Internal reset by illegal-memory access	
Power-on-reset circuit			• Power-on-reset: 1.51 ± 0.03 V • Power-down-reset: 1.50 ± 0.03 V	
Voltage detector			• Rising edge: 1.67 V to 3.13 V (12 stages) • Falling edge: 1.63 V to 3.06 V (12 stages)	
On-chip debug function			Provided	
<R> Power supply voltage			V_{DD} = 1.6 to 3.6 V (T_A = -40 to +85°C) V_{DD} = 2.4 to 3.6 V (T_A = -40 to +105°C)	
Operating ambient temperature			T_A = -40 to +85°C (A: Consumer applications), T_A = -40 to +105°C (G: Industrial applications)	

Note 1. The number in parentheses indicates the number of signal outputs when 8 coms are used.

Note 2. The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution not is issued by emulation with the in-circuit emulator or on-chip debug emulator.

(T_A = -40 to +85°C, 1.6 V ≤ AV_{DD} = V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P46, P50 to P57, P70 to P77, P80 to P83, P125 to P127, P140 to P143	Normal input buffer	0.8 V_{DD}		V_{DD}	V
	V_{IH2}	P00, P01, P10, P11, P24, P25, P33, P34, P43, P44	TTL input buffer 3.3 V ≤ V_{DD} ≤ 3.6 V	2.0		V_{DD}	V
			TTL input buffer 1.6 V ≤ V_{DD} < 3.3 V	1.50		V_{DD}	V
	V_{IH3}	P150 to P156		0.7 AV_{DD}		AV_{DD}	V
	V_{IH4}	P60, P61		0.7 V_{DD}		6.0	V
	V_{IH5}	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$		0.8 V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P46, P50 to P57, P70 to P77, P80 to P83, P125 to P127, P140 to P143	Normal input buffer	0		0.2 V_{DD}	V
	V_{IL2}	P00, P01, P10, P11, P24, P25, P33, P34, P43, P44	TTL input buffer 3.3 V ≤ V_{DD} ≤ 3.6 V	0		0.5	V
			TTL input buffer 1.6 V ≤ V_{DD} < 3.3 V	0		0.32	V
	V_{IL3}	P150 to P156		0		0.3 AV_{DD}	V
	V_{IL4}	P60, P61		0		0.3 V_{DD}	V
	V_{IL5}	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$		0		0.2 V_{DD}	V

Caution The maximum value of V_{IH} of pins P00 to P02, P10 to P12, P24 to P26, P33 to P35, and P42 to P44 is V_{DD}, even in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = -40 to +85°C, 1.6 V ≤ AV_{DD} = V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P46, P50 to P57, P60, P61, P70 to P77, P80 to P83, P125 to P127, P137, P140 to P143, $\overline{RESET}$	V_I = V_{DD}				1	μA
	I_{LIH2}	P20, P21, P140 to P143	V_I = V_{DD}				1	μA
	I_{LIH3}	P121 to P124 (X1, X2, EXCLK, XT1, XT2, EXCLKS)	V_I = V_{DD}	In input port or external clock input			1	μA
				In resonator connection			10	μA
	I_{LIH4}	P150 to P156	V_I = AV_{DD}				1	μA
Input leakage current, low	I_{LIL1}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P46, P50 to P57, P60, P61, P70 to P77, P80 to P83, P125 to P127, P137, P140 to P143, $\overline{RESET}$	V_I = V_{SS}				-1	μA
	I_{LIL2}	P20, P21, P140 to P143	V_I = V_{SS}				-1	μA
	I_{LIL3}	P121 to P124 (X1, X2, EXCLK, XT1, XT2, EXCLKS)	V_I = V_{SS}	In input port or external clock input			-1	μA
				In resonator connection			-10	μA
	I_{LIL4}	P150 to P156	V_I = AV_{SS}				-1	μA
On-chip pull-up resistance	R_{U1}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P50 to P57, P70 to P77, P140 to P143, P125 to P127	V_I = V_{SS}	2.4 V ≤ V_{DD} ≤ 3.6 V	10	20	100	kΩ
				1.6 V ≤ V_{DD} ≤ 2.4 V	10	30	100	
	R_{U2}	P40 to P46, P80 to P83	V_I = V_{SS}		10	20	100	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Note 1. Total current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, or V_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the LCD controller/driver, A/D converter, D/A converter, comparator, LVD circuit, USB 2.0 function module, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

Note 2. When high-speed on-chip oscillator and subsystem clock are stopped.

Note 3. When high-speed system clock and subsystem clock are stopped.

Note 4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the real-time clock 2, 12-bit interval timer, and watchdog timer.

Note 5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode:	2.7 V ≤ V_{DD} ≤ 3.6 V@1 MHz to 24 MHz
	2.4 V ≤ V_{DD} ≤ 3.6 V@1 MHz to 16 MHz
LS (low-speed main) mode:	1.8 V ≤ V_{DD} ≤ 3.6 V@1 MHz to 8 MHz
LV (low-voltage main) mode	1.6 V ≤ V_{DD} ≤ 3.6 V@1 MHz to 4 MHz

Remark 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 2. f_{HOCO}: High-speed on-chip oscillator clock frequency (48 MHz max.)

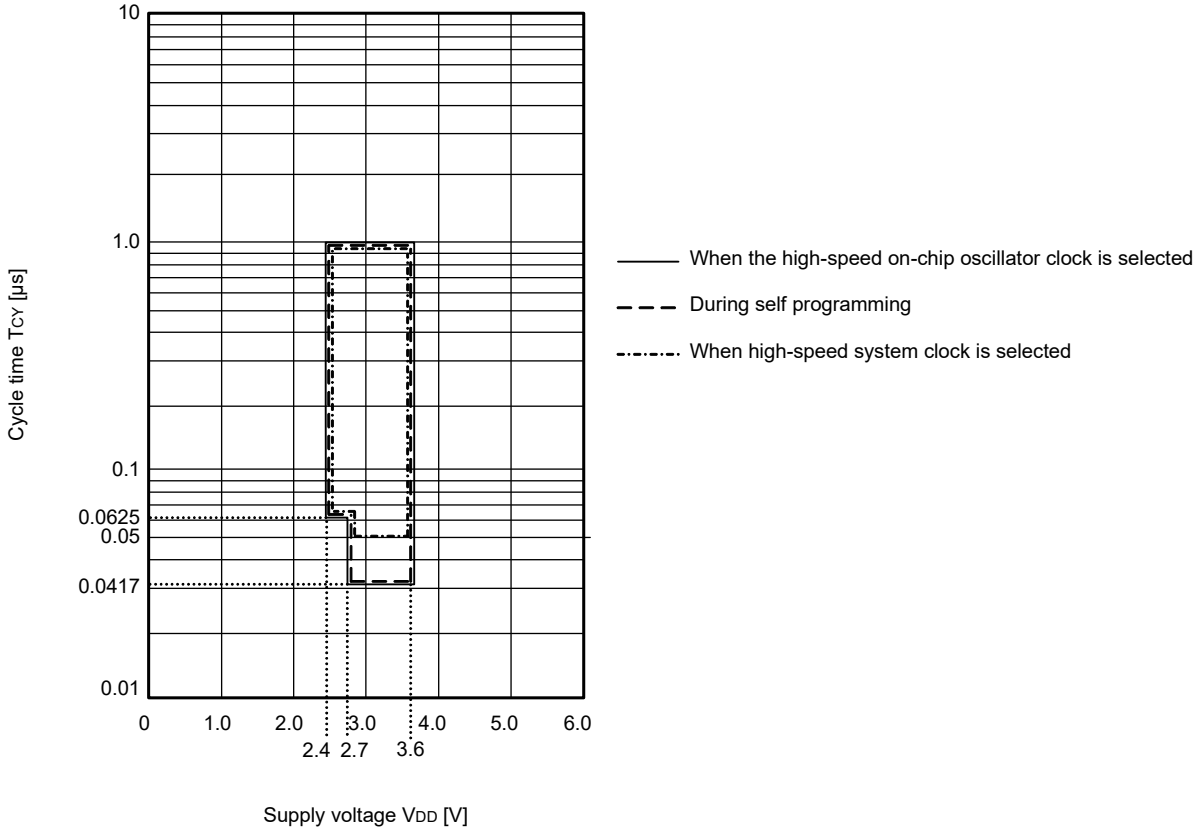
Remark 3. f_{IH}: Main system clock source frequency when the high-speed on-chip oscillator clock divided 1, 2, 4, or 8, or the PLL clock divided by 2, 4, or 8 is selected (24 MHz max.)

Remark 4. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

Remark 5. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

Minimum Instruction Execution Time during Main System Clock Operation

T_{CY} vs V_{DD} (HS (high-speed main) mode)



(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only)

(T_A = -40 to +85°C, 2.7 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq f_{CLK}/2$	2.7 V ≤ V_{DD} ≤ 3.6 V	167		250		500		ns
SCKp high-/low-level width	t_{KL1}	2.7 V ≤ V_{DD} ≤ 3.6 V		t_{KCY1}/2 - 10		t_{KCY1}/2 - 50		t_{KCY1}/2 - 50		ns
SIp setup time (to SCKp↑) Note 1	t_{SIK1}	2.7 V ≤ V_{DD} ≤ 3.6 V		33		110		110		ns
SIp hold time (from SCKp↑) Note 2	t_{KSI1}	2.7 V ≤ V_{DD} ≤ 3.6 V		10		10		10		ns
Delay time from SCKp↓ to SOp output Note 3	t_{KSO1}	C = 20 pF Note 4			10		10		10	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

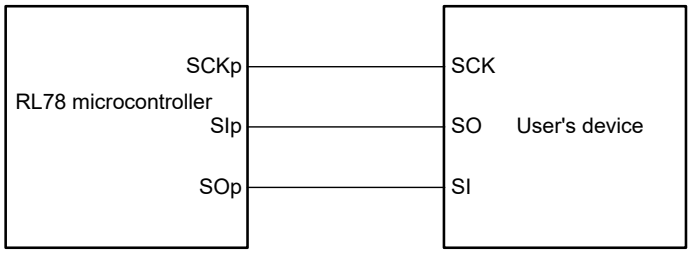
Note 4. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM number (g = 2)

Remark 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))

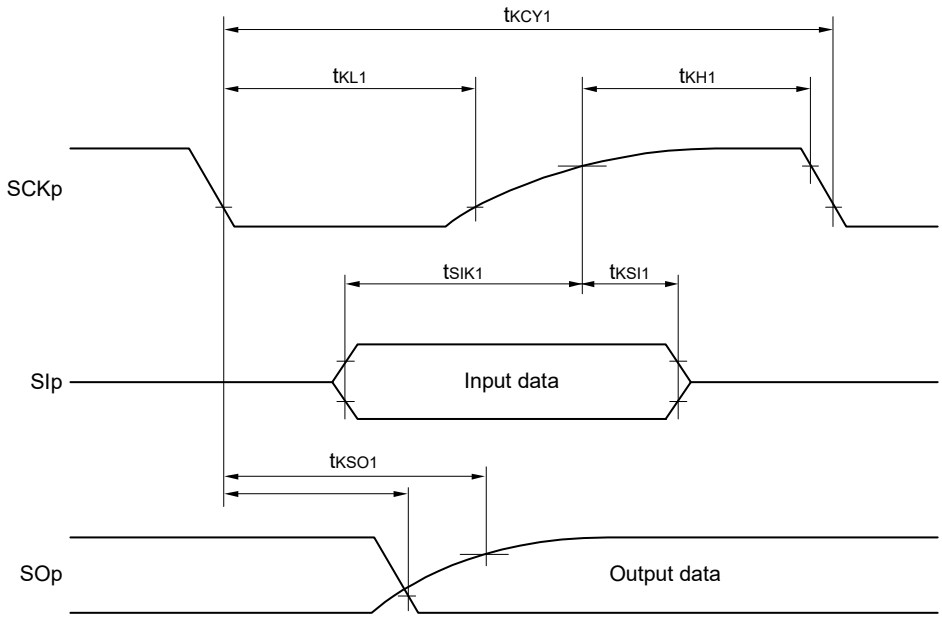
CSI mode connection diagram (during communication at same potential)



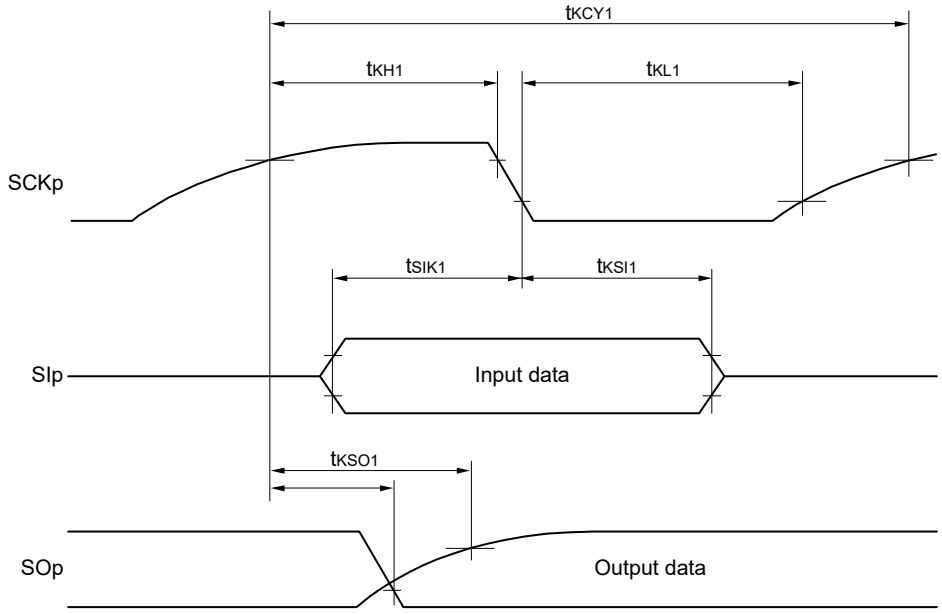
Remark 1. p: CSI number (p = 00, 10, 20, 30)

Remark 2. m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark p: CSI number (p = 00, 10, 20, 30), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),
g: PIM and POM number (g = 0 to 3)

2.5.2 Serial interface IICA

(1) I²C standard mode

(T_A = -40 to +85°C, 1.6 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Standard mode: f_{CLK} ≥ 1 MHz	2.7 V ≤ V_{DD} ≤ 3.6 V	0	100	0	100	0	100	kHz
			1.8 V ≤ V_{DD} ≤ 3.6 V	—	—	0	100	0	100	kHz
			1.6 V ≤ V_{DD} ≤ 3.6 V	—	—	—	—	0	100	kHz
Setup time of restart condition	$t_{SU: STA}$	2.7 V ≤ V_{DD} ≤ 3.6 V		4.7		4.7		4.7		µs
		1.8 V ≤ V_{DD} ≤ 3.6 V		—		4.7		4.7		µs
		1.6 V ≤ V_{DD} ≤ 3.6 V		—		—		4.7		µs
Hold time Note 1	$t_{HD: STA}$	2.7 V ≤ V_{DD} ≤ 3.6 V		4.0		4.0		4.0		µs
		1.8 V ≤ V_{DD} ≤ 3.6 V		—		4.0		4.0		µs
		1.6 V ≤ V_{DD} ≤ 3.6 V		—		—		4.0		µs
Hold time when SCLA0 = “L”	t_{LOW}	2.7 V ≤ V_{DD} ≤ 3.6 V		4.7		4.7		4.7		µs
		1.8 V ≤ V_{DD} ≤ 3.6 V		—		4.7		4.7		µs
		1.6 V ≤ V_{DD} ≤ 3.6 V		—		—		4.7		µs
Hold time when SCLA0 = “H”	t_{HIGH}	2.7 V ≤ V_{DD} ≤ 3.6 V		4.0		4.0		4.0		µs
		1.8 V ≤ V_{DD} ≤ 3.6 V		—		4.0		4.0		µs
		1.6 V ≤ V_{DD} ≤ 3.6 V		—		—		4.0		µs
Data setup time (reception)	$t_{SU: DAT}$	2.7 V ≤ V_{DD} ≤ 3.6 V		250		250		250		ns
		1.8 V ≤ V_{DD} ≤ 3.6 V		—		250		250		ns
		1.6 V ≤ V_{DD} ≤ 3.6 V		—		—		250		ns
Data hold time (transmission) Note 2	$t_{HD: DAT}$	2.7 V ≤ V_{DD} ≤ 3.6 V		0	3.45	0	3.45	0	3.45	µs
		1.8 V ≤ V_{DD} ≤ 3.6 V		—	—	0	3.45	0	3.45	µs
		1.6 V ≤ V_{DD} ≤ 3.6 V		—	—	—	—	0	3.45	µs
Setup time of stop condition	$t_{SU: STO}$	2.7 V ≤ V_{DD} ≤ 3.6 V		4.0		4.0		4.0		µs
		1.8 V ≤ V_{DD} ≤ 3.6 V		—		4.0		4.0		µs
		1.6 V ≤ V_{DD} ≤ 3.6 V		—		—		4.0		µs
Bus-free time	t_{BUF}	2.7 V ≤ V_{DD} ≤ 3.6 V		4.7		4.7		4.7		µs
		1.8 V ≤ V_{DD} ≤ 3.6 V		—		4.7		4.7		µs
		1.6 V ≤ V_{DD} ≤ 3.6 V		—		—		4.7		µs

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.

Note 2. The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.
Standard mode: C_b = 400 pF, R_b = 2.7 kΩ

(2) 1/4 bias method

(T_A = -40 to +85°C, 1.8 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

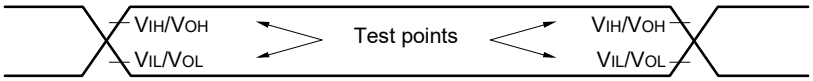
Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
LCD output voltage variation range	V_{L1}	C1 to C4 Note 1 = 0.47 μF Note 2	VLCD = 04H	0.90	1.00	1.08	V
			VLCD = 05H	0.95	1.05	1.13	V
			VLCD = 06H	1.00	1.10	1.18	V
			VLCD = 07H	1.05	1.15	1.23	V
			VLCD = 08H	1.10	1.20	1.28	V
			VLCD = 09H	1.15	1.25	1.33	V
			VLCD = 0AH	1.20	1.30	1.38	V
Doubler output voltage	V_{L2}	C1 to C4 Note 1 = 0.47 μF		2 V_{L1} - 0.08	2 V_{L1}	2 V_{L1}	V
Tripler output voltage	V_{L3}	C1 to C4 Note 1 = 0.47 μF		3 V_{L1} - 0.12	3 V_{L1}	3 V_{L1}	V
Quadruply output voltage	V_{L4}	C1 to C5 Note 1 = 0.47 μF		4 V_{L1} - 0.16	4 V_{L1}	4 V_{L1}	V
Reference voltage setup time Note 2	t_{VWAIT1}			5			ms
Voltage boost wait time Note 3	t_{VWAIT2}	C1 to C5 Note 1 = 0.47μF		500			ms

Note 1. This is a capacitor that is connected between voltage pins used to drive the LCD.
C1: A capacitor connected between CAPH and CAPL
C2: A capacitor connected between V_{L1} and GND
C3: A capacitor connected between V_{L2} and GND
C4: A capacitor connected between V_{L3} and GND
C5: A capacitor connected between V_{L4} and GND
C1 = C2 = C3 = C4 = 0.47 μF±30%

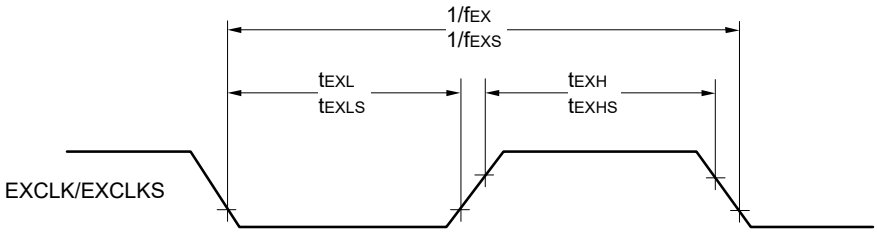
Note 2. This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected (by setting the MDSET1 and MDSET0 bits of the LCDM0 register to 01B) if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).

Note 3. This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

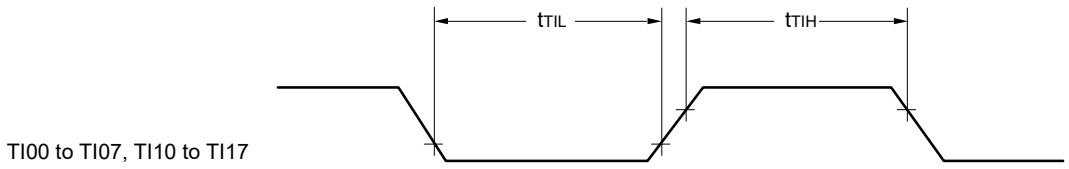
AC Timing Test Points

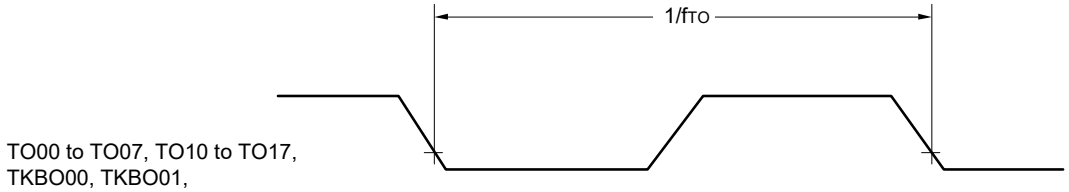


External System Clock Timing

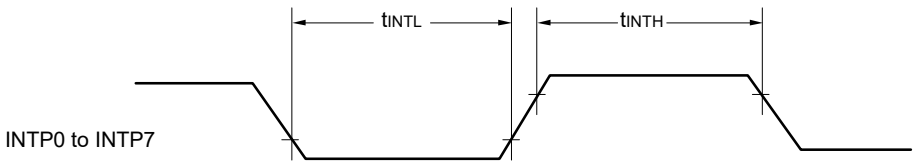


TI/TO Timing

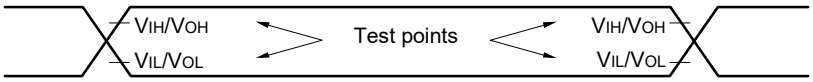




Interrupt Request Input Timing



3.5 Peripheral Functions Characteristics



3.5.1 Serial array unit

(1) During communication at same potential (UART mode)

(TA = -40 to +105°C, 2.4 V ≤ VDD ≤ 3.6 V, VSS = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
Transfer rate Note 1		2.4 V ≤ VDD ≤ 3.6 V		fMCK/12 Note 2	bps
		Theoretical value of the maximum transfer rate fMCK = fCLK Note 3		2.0	Mbps

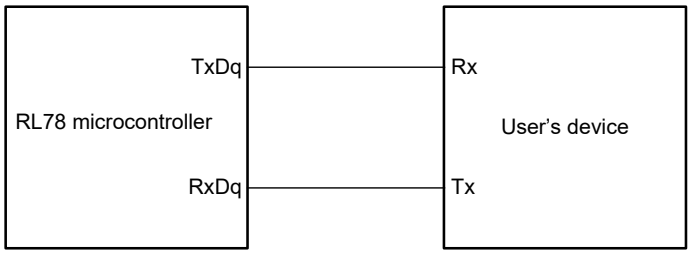
Note 1. Transfer rate in the SNOOZE mode is 4800 bps only.

Note 2. The following conditions are required for low voltage interface.
2.4 V ≤ VDD < 2.7 V: MAX. 1.3 Mbps

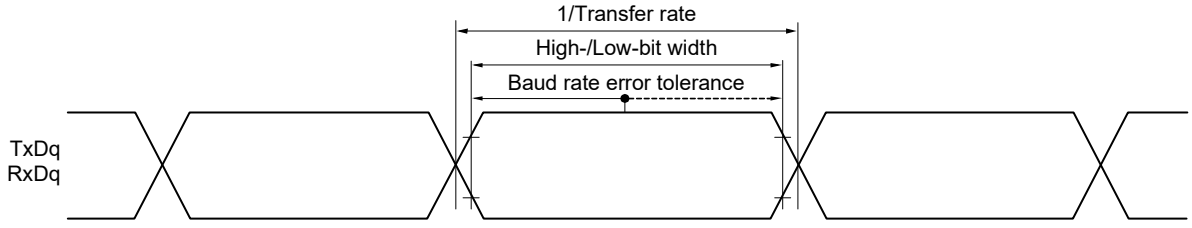
Note 3. The maximum operating frequencies of the CPU/peripheral hardware clock (fCLK) are:
HS (high-speed main) mode: 24 MHz (2.7 V ≤ VDD ≤ 3.6 V)
16 MHz (2.4 V ≤ VDD ≤ 3.6 V)

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

UART mode connection diagram (during communication at same potential)



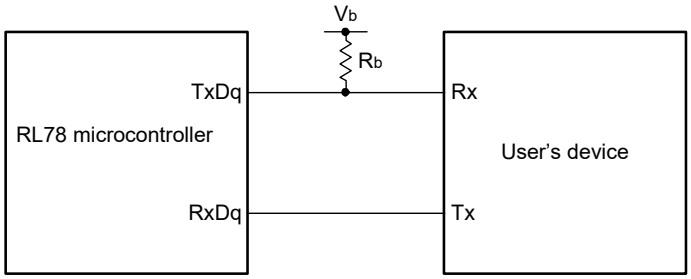
UART mode bit width (during communication at same potential) (reference)



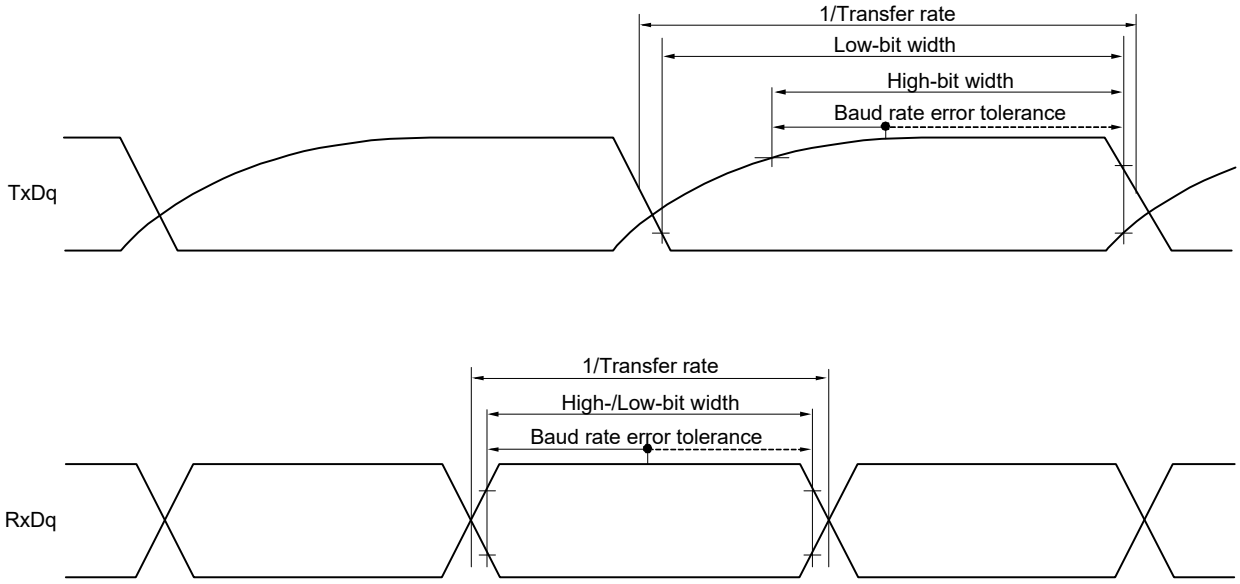
Remark 1. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0 to 3)

Remark 2. fMCK: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

UART mode connection diagram (during communication at different potential)



UART mode bit width (during communication at different potential) (reference)

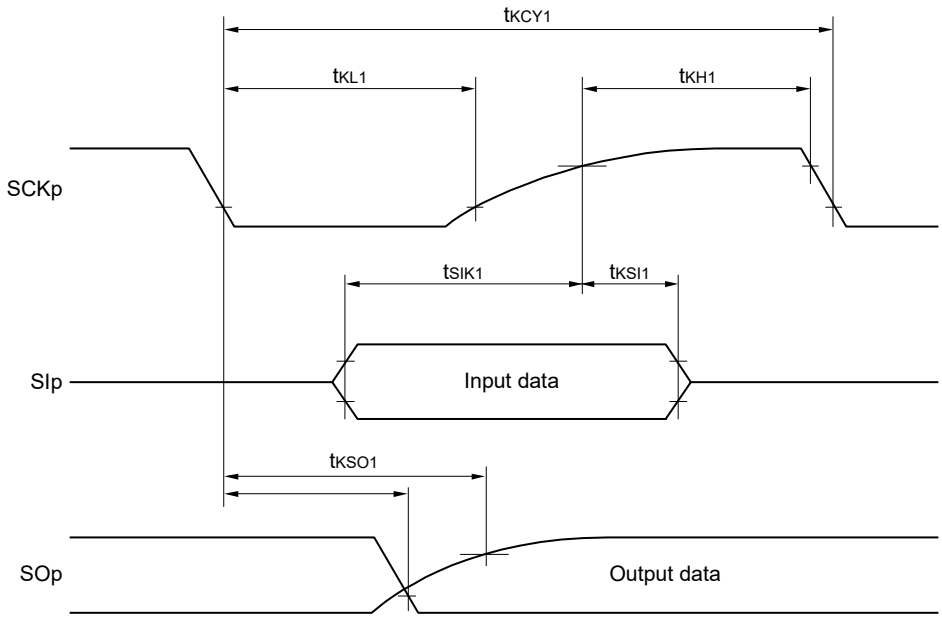


Remark 1. R_b[Ω]: Communication line (TxDq) pull-up resistance, C_b[F]: Communication line (TxDq) load capacitance, V_b[V]: Communication line voltage

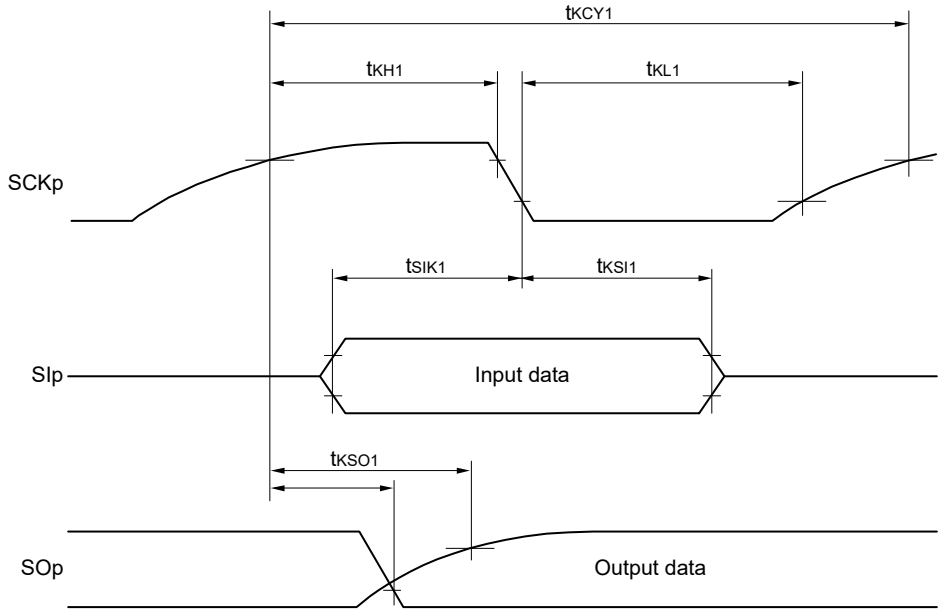
Remark 2. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0 to 3)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark p: CSI number (p = 00, 10, 20, 30), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),
g: PIM and POM number (g = 0 to 3)

3.5.2 Serial interface IICA

(T_A = -40 to +105°C, 2.4 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode				Unit
			Standard mode		Fast mode		
			MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Fast mode: f_{CLK} ≥ 3.5 MHz	—	—	0	400	kHz
		Standard mode: f_{CLK} ≥ 1 MHz	0	100	—	—	kHz
Setup time of restart condition	$t_{SU: STA}$		4.7		0.6		µs
Hold time Note 1	$t_{HD: STA}$		4.0		0.6		µs
Hold time when SCLA0 = "L"	t_{LOW}		4.7		1.3		µs
Hold time when SCLA0 = "H"	t_{HIGH}		4.0		0.6		µs
Data setup time (reception)	$t_{SU: DAT}$		250		100		ns
Data hold time (transmission) Note 2	$t_{HD: DAT}$		0	3.45	0	0.9	µs
Setup time of stop condition	$t_{SU: STO}$		4.0		0.6		µs
Bus-free time	t_{BUF}		4.7		1.3		µs

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.

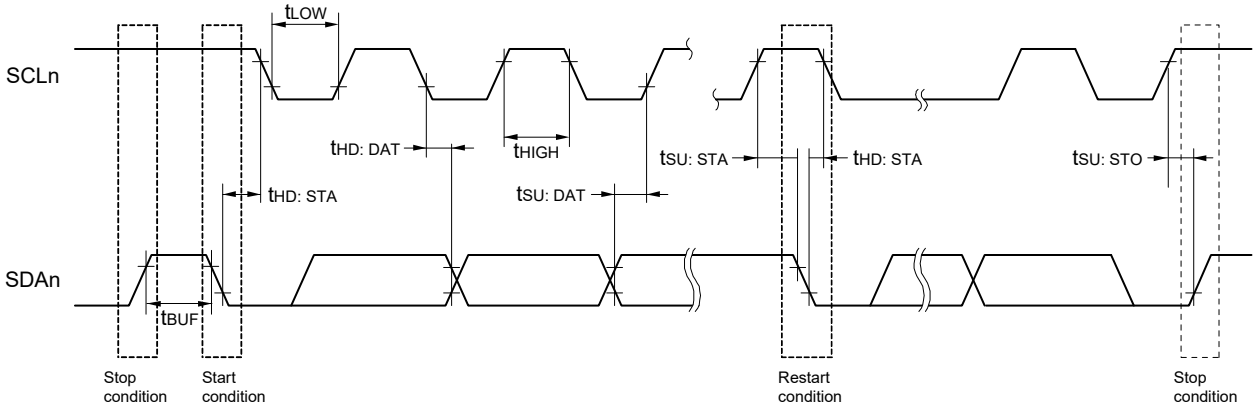
Note 2. The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: C_b = 400 pF, R_b = 2.7 kΩ

Fast mode: C_b = 320 pF, R_b = 1.1 kΩ

IICA serial transfer timing



3.5.3 USB

(1) Electrical specifications

(T_A = -40 to +105°C, 2.4 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
UREGC	UREGC output voltage characteristic	UREGC	UVBUS = 4.0 to 5.5 V, PXXCON = VDDUSBE = 1	3.0	3.3	3.6	V
UVBUS	UVBUS input voltage characteristic	UVBUS	Function	4.35 (4.02 Note)	5.00	5.25	V

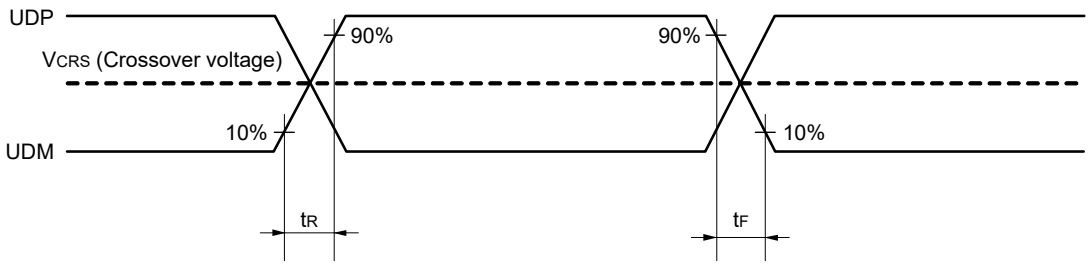
Note Value of instantaneous voltage

(T_A = -40 to +105°C, 4.35 V ≤ UVBUS ≤ 5.25 V, 2.4 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

Parameter			Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input characteristic (FS/LS receiver)	Input voltage		VIH		2.0			V
			VIL				0.8	V
	Difference input sensitivity		VDI	| UDP voltage - UDM voltage |	0.2			V
	Difference common mode range		VCM		0.8		2.5	V
Output characteristic (FS driver)	Output voltage		VOH	IOH = -200 μA	2.8		3.6	V
			VOL	IOL = 2 mA	0		0.3	V
	Transition time	Rising	tFR	Rising: From 10% to 90% of amplitude, Falling: From 90% to 10% of amplitude, CL = 50 pF	4		20	ns
		Falling	tFF		4		20	ns
	Matching (TFR/TFF)		VFRFM		90		111.1	%
	Crossover voltage		VFCRS		1.3		2.0	V
	Output Impedance		ZDRV		28		44	Ω
Output characteristic (LS driver)	Output voltage		VOH		2.8		3.6	V
			VOL		0		0.3	V
	Transition time	Rising	tLR	Rising: From 10% to 90% of amplitude, Falling: From 90% to 10% of amplitude, CL = 250 pF to 750 pF The UDP and UDM pins are individually pulled down via 15 kΩ	75		300	ns
		Falling	tLF		75		300	ns
	Matching (TFR/TFF) Note		VLTFM		80		125	%
	Crossover voltage Note		VLCRS		1.3		2.0	V
Pull-up, Pull-down	Pull-down resistor		RPD		14.25		24.80	kΩ
	Pull-up resistor	Idle	RPUI		0.9		1.575	kΩ
		Reception	RPUA		1.425		3.09	kΩ
UVBUS	UVBUS pull-down resistor		RVBUS	UVBUS voltage = 5.5 V		1000		kΩ
	UVBUS input voltage		VIH		3.20			V
			VIL				0.8	V

Note Excludes the first signal transition from the idle state.

Timing of UDP and UDM



(2) BC standard

(TA = -40 to +105°C, 4.35 V ≤ UVBUS ≤ 5.25 V, 2.4 V ≤ VDD ≤ 3.6 V, VSS = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
USB standard BC1.2	UDP sink current	IDP_SINK		25	100	175	μA
	UDM sink current	IDM_SINK		25	100	175	μA
	DCD source current	IDP_SRC		7	10	13	μA
	Data detection voltage	VDAT_REF		0.25	0.325	0.4	V
	UDP source voltage	VDP_SRC	Output current 250 μA	0.5	0.6	0.7	V
	UDM source voltage	VDM_SRC	Output current 250 μA	0.5	0.6	0.7	V

3.10 Flash Memory Programming Characteristics

(T_A = -40 to +105°C, 2.4 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CPU/peripheral hardware clock frequency	f_{CLK}	2.4 V ≤ V_{DD} ≤ 3.6 V	1		24	MHz
Number of code flash rewrites Notes 1, 2, 3	C_{erwr}	Retained for 20 years T_A = 85°C Note 4	1,000			Times
Number of data flash rewrites Notes 1, 2, 3		Retained for 1 year T_A = 25°C		1,000,000		
		Retained for 5 years T_A = 85°C Note 4	100,000			
		Retained for 20 years T_A = 85°C Note 4	10,000			

Note 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

Note 2. When using flash memory programmer and Renesas Electronics self programming library

Note 3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

Note 4. This temperature is the average value at which data are retained.

3.11 Dedicated Flash Memory Programmer Communication (UART)

(T_A = -40 to +105°C, 2.4 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

REVISION HISTORY	RL78/L1C Datasheet

Rev.	Date	Description	
		Page	Summary
2.00	Feb 21, 2014	4	Modification of Figure 1 - 1 Part Number, Memory Size, and Package of RL78/L1C
		69	Modification of (1) Electrical specifications in 2.5.3 USB
		82	Modification of note 1 in (1) 1/3 bias method in 2.8.2 Internal voltage boosting method
		130	Modification of (1) Electrical specifications in 3.5.3 USB
		142	Modification of note 1 in (1) 1/3 bias method in 3.8.2 Internal voltage boosting method
2.10	Aug 12, 2016	5	Addition of product name (RL78/L1C) and description (Top View) in 1.3.1 80-pin products (with USB)
		6	Addition of product name (RL78/L1C) and description (Top View) in 1.3.2 80-pin products (without USB)
		9	Addition of product name (RL78/L1C) and description (Top View) in 1.3.5 100-pin products (with USB)
		10	Addition of product name (RL78/L1C) and description (Top View) in 1.3.6 100-pin products (without USB)
		17, 19	Modification of 1.6 Outline of Functions
		23	Modification of description in Absolute Maximum Ratings (T_A = 25°C)
		26, 27	Modification of description in 2.3.1 Pin characteristics
		39, 40	Modification of the graph for Minimum Instruction Execution Time during Main System Clock Operation
		72	Modification of conditions in (1) of 2.6.1 A/D converter characteristics
		85	Modification of the title and note in 2.9 RAM Data Retention Characteristics
		85	Modification of conditions in 2.10 Flash Memory Programming Characteristics
		87	Modification of description in 3. ELECTRICAL SPECIFICATIONS (G: INDUSTRIAL APPLICATIONS T_A = -40 to +105 °C)
		88, 90	Modification of description in Absolute Maximum Ratings (T_A = 25°C)
		93, 94, 96	Modification of description in 3.3.1 Pin characteristics
		106	Modification of the graph for Minimum Instruction Execution Time during Main System Clock Operation
		144	Modification of the title and note in 3.9 RAM Data Retention Characteristics
		145	Modification of conditions and addition of note 4 in 3.10 Flash Memory Programming Characteristics
2.20	Dec 28, 2017	13	Modification of figure in 1.5.2 80/85-pin products (without USB)
		17, 19	Modification of tables in 1.6 Outline of Functions
		26, 27	Modification of table and note 3 in 2.3.1 Pin characteristics
		85	Modification of figure in 2.12 Timing of Entry to Flash Memory Programming Modes
		89	Modification of table in 3.1 Absolute Maximum Ratings
		92, 93	Modification of table and note 3 in 3.3.1 Pin characteristics
		144	Modification of figure in 3.12 Timing of Entry to Flash Memory Programming Modes