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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I <sup>2</sup> C, IrDA, SPI, UART/USART
Peripherals	DMA, I <sup>2</sup> S, LVD, POR, PWM, WDT
Number of I/O	60
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 24x16b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-FQFP (12x12)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/nxp-semiconductors/mk12dx256vlk5">https://www.e-xfl.com/product-detail/nxp-semiconductors/mk12dx256vlk5</a>

# 1 Ordering parts

## 1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to [freescale.com](http://freescale.com) and perform a part number search for the following device numbers: PK12 and MK12 .

# 2 Part identification

## 2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

## 2.2 Format

Part numbers for this device have the following format:

Q K## A M FFF R T PP CC N

## 2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	<ul style="list-style-type: none"> <li>M = Fully qualified, general market flow</li> <li>P = Prequalification</li> </ul>
K##	Kinetis family	<ul style="list-style-type: none"> <li>K12</li> </ul>
A	Key attribute	<ul style="list-style-type: none"> <li>D = Cortex-M4 w/ DSP</li> <li>F = Cortex-M4 w/ DSP and FPU</li> </ul>
M	Flash memory type	<ul style="list-style-type: none"> <li>N = Program flash only</li> <li>X = Program flash and FlexMemory</li> </ul>

Table continues on the next page...

## Part identification

Field	Description	Values
FFF	Program flash memory size	<ul style="list-style-type: none"> <li>• 32 = 32 KB</li> <li>• 64 = 64 KB</li> <li>• 128 = 128 KB</li> <li>• 256 = 256 KB</li> <li>• 512 = 512 KB</li> <li>• 1M0 = 1 MB</li> <li>• 2M0 = 2 MB</li> </ul>
R	Silicon revision	<ul style="list-style-type: none"> <li>• Z = Initial</li> <li>• (Blank) = Main</li> <li>• A = Revision after main</li> </ul>
T	Temperature range (°C)	<ul style="list-style-type: none"> <li>• V = -40 to 105</li> <li>• C = -40 to 85</li> </ul>
PP	Package identifier	<ul style="list-style-type: none"> <li>• FM = 32 QFN (5 mm x 5 mm)</li> <li>• FT = 48 QFN (7 mm x 7 mm)</li> <li>• LF = 48 LQFP (7 mm x 7 mm)</li> <li>• LH = 64 LQFP (10 mm x 10 mm)</li> <li>• MP = 64 MAPBGA (5 mm x 5 mm)</li> <li>• LK = 80 LQFP (12 mm x 12 mm)</li> <li>• LL = 100 LQFP (14 mm x 14 mm)</li> <li>• MC = 121 MAPBGA (8 mm x 8 mm)</li> <li>• LQ = 144 LQFP (20 mm x 20 mm)</li> <li>• MD = 144 MAPBGA (13 mm x 13 mm)</li> </ul>
CC	Maximum CPU frequency (MHz)	<ul style="list-style-type: none"> <li>• 5 = 50 MHz</li> <li>• 7 = 72 MHz</li> <li>• 10 = 100 MHz</li> <li>• 12 = 120 MHz</li> <li>• 15 = 150 MHz</li> <li>• 18 = 180 MHz</li> </ul>
N	Packaging type	<ul style="list-style-type: none"> <li>• R = Tape and reel</li> <li>• (Blank) = Trays</li> </ul>

## 2.4 Example

This is an example part number:

MK12DX128VLK5

## 2.5 Small package marking

In an effort to save space, small package devices use special marking on the chip. These markings have the following format:

Q ## C F T PP

This table lists the possible values for each field in the part number for small packages (not all combinations are valid):

Field	Description	Values
Q	Qualification status	<ul style="list-style-type: none"> <li>M = Fully qualified, general market flow</li> <li>P = Prequalification</li> </ul>
C	Speed	<ul style="list-style-type: none"> <li>G = 50 MHz</li> </ul>
F	Flash memory configuration	<ul style="list-style-type: none"> <li>G = 128 KB + Flex</li> <li>H = 256 KB + Flex</li> <li>9 = 512 KB</li> </ul>
T	Temperature range (°C)	<ul style="list-style-type: none"> <li>V = -40 to 105</li> </ul>
PP	Package identifier	<ul style="list-style-type: none"> <li>MC = 121 MAPBGA</li> </ul>

This table lists some examples of small package marking along with the original part numbers:

Original part number	Alternate part number
MK12DX256VLF5	M12GHVLF
MK12DN512VLH5	M12G9VLH

## 3 Terminology and guidelines

### 3.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

#### 3.1.1 Example

This is an example of an operating requirement:

Symbol	Description	Min.	Max.	Unit
V <sub>DD</sub>	1.0 V core supply voltage	0.9	1.1	V

**Table 1. Voltage and current operating requirements (continued)**

Symbol	Description	Min.	Max.	Unit	Notes
$I_{Ccont}$	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins <ul style="list-style-type: none"> <li>Negative current injection</li> <li>Positive current injection</li> </ul>	-25 —	— +25	mA	
$V_{RAM}$	$V_{DD}$ voltage required to retain RAM	1.2	—	V	
$V_{RFVBAT}$	$V_{BAT}$ voltage required to retain the VBAT register file	$V_{POR\_VBAT}$	—	V	

- All analog pins are internally clamped to  $V_{SS}$  and  $V_{DD}$  through ESD protection diodes. If  $V_{IN}$  is less than  $V_{AIO\_MIN}$  or greater than  $V_{AIO\_MAX}$ , a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as  $R=(V_{AIO\_MIN}-V_{IN})/|I_{ICAIO}|$ . The positive injection current limiting resistor is calculated as  $R=(V_{IN}-V_{AIO\_MAX})/|I_{ICAIO}|$ . Select the larger of these two calculated resistances if the pin is exposed to positive and negative injection currents.

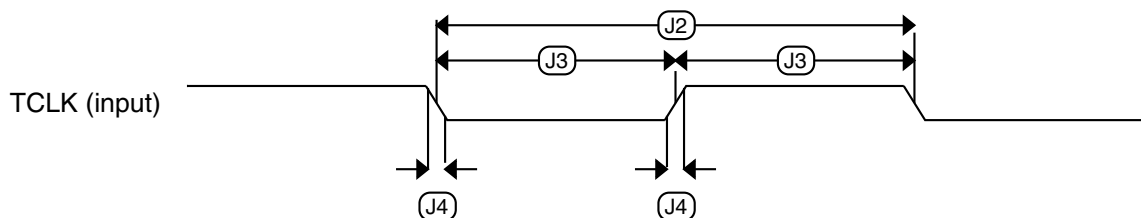
## 5.2.2 LVD and POR operating requirements

**Table 2.  $V_{DD}$  supply LVD and POR operating requirements**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$V_{POR}$	Falling VDD POR detect voltage	0.8	1.1	1.5	V	
$V_{LVDH}$	Falling low-voltage detect threshold — high range (LVDV=01)	2.48	2.56	2.64	V	
$V_{LVW1H}$	Low-voltage warning thresholds — high range <ul style="list-style-type: none"> <li>Level 1 falling (LVWV=00)</li> </ul>	2.62	2.70	2.78	V	1
$V_{LVW2H}$	<ul style="list-style-type: none"> <li>Level 2 falling (LVWV=01)</li> </ul>	2.72	2.80	2.88	V	
$V_{LVW3H}$	<ul style="list-style-type: none"> <li>Level 3 falling (LVWV=10)</li> </ul>	2.82	2.90	2.98	V	
$V_{LVW4H}$	<ul style="list-style-type: none"> <li>Level 4 falling (LVWV=11)</li> </ul>	2.92	3.00	3.08	V	
$V_{HYSH}$	Low-voltage inhibit reset/recover hysteresis — high range	—	80	—	mV	
$V_{LVDL}$	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	
$V_{LVW1L}$	Low-voltage warning thresholds — low range <ul style="list-style-type: none"> <li>Level 1 falling (LVWV=00)</li> </ul>	1.74	1.80	1.86	V	1
$V_{LVW2L}$	<ul style="list-style-type: none"> <li>Level 2 falling (LVWV=01)</li> </ul>	1.84	1.90	1.96	V	
$V_{LVW3L}$	<ul style="list-style-type: none"> <li>Level 3 falling (LVWV=10)</li> </ul>	1.94	2.00	2.06	V	
$V_{LVW4L}$	<ul style="list-style-type: none"> <li>Level 4 falling (LVWV=11)</li> </ul>	2.04	2.10	2.16	V	
$V_{HYSL}$	Low-voltage inhibit reset/recover hysteresis — low range	—	60	—	mV	
$V_{BG}$	Bandgap voltage reference	0.97	1.00	1.03	V	
$t_{LPO}$	Internal low power oscillator period — factory trimmed	900	1000	1100	$\mu$ s	

**Table 13. JTAG full voltage range electricals**

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	TCLK frequency of operation <ul style="list-style-type: none"> <li>Boundary Scan</li> <li>JTAG and CJTAG</li> <li>Serial Wire Debug</li> </ul>	0 0 0	10 20 40	MHz
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width <ul style="list-style-type: none"> <li>Boundary Scan</li> <li>JTAG and CJTAG</li> <li>Serial Wire Debug</li> </ul>	50 25 12.5	— — —	ns ns ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	0	—	ns
J7	TCLK low to boundary scan output data valid	—	25	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1.4	—	ns
J11	TCLK low to TDO data valid	—	22.1	ns
J12	TCLK low to TDO high-Z	—	22.1	ns
J13	TRST assert time	100	—	ns
J14	TRST setup time (negation) to TCLK high	8	—	ns


**Figure 4. Test clock input timing**

**Table 14. MCG specifications (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{pll\_lock}$	Lock detector detection time	—	—	$150 \times 10^{-6} + 1075(1/f_{pll\_ref})$	s	10

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2.  $2\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ .
3. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.
4. The resulting system clock frequencies should not exceed their maximum specified values. The DCO frequency deviation ( $\Delta f_{dco\_t}$ ) over voltage and temperature should be considered.
5. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.
6. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
7. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
8. Excludes any oscillator currents that are also consuming power while PLL is in operation.
9. This specification was obtained using a Freescale developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.
10. This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

## 6.3.2 Oscillator electrical specifications

### 6.3.2.1 Oscillator DC electrical specifications

**Table 15. Oscillator DC electrical specifications**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$V_{DD}$	Supply voltage	1.71	—	3.6	V	
$I_{DDOSC}$	Supply current — low-power mode (HGO=0)					1
	• 32 kHz	—	500	—	nA	
	• 4 MHz	—	200	—	$\mu\text{A}$	
	• 8 MHz (RANGE=01)	—	300	—	$\mu\text{A}$	
	• 16 MHz	—	950	—	$\mu\text{A}$	
	• 24 MHz	—	1.2	—	mA	
	• 32 MHz	—	1.5	—	mA	

Table continues on the next page...

**Table 15. Oscillator DC electrical specifications (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$I_{DDOSC}$	Supply current — high-gain mode (HGO=1)					1
	• 32 kHz	—	25	—	$\mu A$	
	• 4 MHz	—	400	—	$\mu A$	
	• 8 MHz (RANGE=01)	—	500	—	$\mu A$	
	• 16 MHz	—	2.5	—	mA	
	• 24 MHz	—	3	—	mA	
	• 32 MHz	—	4	—	mA	
$C_x$	EXTAL load capacitance	—	—	—		2, 3
$C_y$	XTAL load capacitance	—	—	—		2, 3
$R_F$	Feedback resistor — low-frequency, low-power mode (HGO=0)	—	—	—	M $\Omega$	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	—	10	—	M $\Omega$	
	Feedback resistor — high-frequency, low-power mode (HGO=0)	—	—	—	M $\Omega$	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	—	1	—	M $\Omega$	
$R_S$	Series resistor — low-frequency, low-power mode (HGO=0)	—	—	—	k $\Omega$	
	Series resistor — low-frequency, high-gain mode (HGO=1)	—	200	—	k $\Omega$	
	Series resistor — high-frequency, low-power mode (HGO=0)	—	—	—	k $\Omega$	
	Series resistor — high-frequency, high-gain mode (HGO=1)	—	0	—	k $\Omega$	
$V_{pp}$ <sup>5</sup>	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)	—	$V_{DD}$	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1)	—	$V_{DD}$	—	V	

1.  $V_{DD}$ =3.3 V, Temperature =25 °C

2. See crystal or resonator manufacturer's recommendation

3.  $C_x$  and  $C_y$  can be provided by using either integrated capacitors or external components.

4. When low-power mode is selected,  $R_F$  is integrated and must not be attached externally.

5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other device.



### 6.3.2.2 Oscillator frequency specifications

**Table 16. Oscillator frequency specifications**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$f_{osc\_lo}$	Oscillator crystal or resonator frequency — low-frequency mode (MCG_C2[RANGE]=00)	32	—	40	kHz	
$f_{osc\_hi\_1}$	Oscillator crystal or resonator frequency — high-frequency mode (low range) (MCG_C2[RANGE]=01)	3	—	8	MHz	
$f_{osc\_hi\_2}$	Oscillator crystal or resonator frequency — high-frequency mode (high range) (MCG_C2[RANGE]=1x)	8	—	32	MHz	
$f_{ec\_extal}$	Input clock frequency (external clock mode)	—	—	50	MHz	1, 2
$t_{dc\_extal}$	Input clock duty cycle (external clock mode)	40	50	60	%	
$t_{cst}$	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)	—	750	—	ms	3, 4
	Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1)	—	250	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0)	—	0.6	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1)	—	1	—	ms	

1. Other frequency limits may apply when external clock is being used as a reference for FLL or PLL.
2. When transitioning from FBE to FEI mode, restrict the frequency of the input clock so that—it remains within the limits of DCO input clock frequency when divided by FRDIV.
3. Proper PC board layout procedures must be followed to achieve specifications.
4. Crystal startup time is defined as the time between oscillator being enabled and OSCINIT bit in the MCG\_S register being set.

#### NOTE

The 32 kHz oscillator works in low power mode by default and cannot be moved into high power/gain mode.

### 6.3.3 32 kHz oscillator electrical characteristics

#### 6.3.3.1 32 kHz oscillator DC electrical specifications

**Table 17. 32kHz oscillator DC electrical specifications**

Symbol	Description	Min.	Typ.	Max.	Unit
$V_{BAT}$	Supply voltage	1.71	—	3.6	V
$R_F$	Internal feedback resistor	—	100	—	MΩ
$C_{para}$	Parasitical capacitance of EXTAL32 and XTAL32	—	5	7	pF

Table continues on the next page...

**Table 17. 32kHz oscillator DC electrical specifications (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit
$V_{pp}^1$	Peak-to-peak amplitude of oscillation	—	0.6	—	V

1. When a crystal is being used with the 32 kHz oscillator, the EXTAL32 and XTAL32 pins should only be connected to required oscillator components and must not be connected to any other devices.

### 6.3.3.2 32 kHz oscillator frequency specifications

**Table 18. 32 kHz oscillator frequency specifications**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$f_{osc\_lo}$	Oscillator crystal	—	32.768	—	kHz	
$t_{start}$	Crystal start-up time	—	1000	—	ms	1
$V_{ec\_extal32}$	Externally provided input clock amplitude	700	—	$V_{BAT}$	mV	2, 3

1. Proper PC board layout procedures must be followed to achieve specifications.
2. This specification is for an externally supplied clock driven to EXTAL32 and does not apply to any other clock input. The oscillator remains enabled and XTAL32 must be left unconnected.
3. The parameter specified is a peak-to-peak value and  $V_{IH}$  and  $V_{IL}$  specifications do not apply. The voltage of the applied clock must be within the range of  $V_{SS}$  to  $V_{BAT}$ .

## 6.4 Memories and memory interfaces

### 6.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

#### 6.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

**Table 19. NVM program/erase timing specifications**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{hvp4}$	Longword Program high-voltage time	—	7.5	18	$\mu$ s	
$t_{hversscr}$	Sector Erase high-voltage time	—	13	113	ms	1
$t_{hversblk256k}$	Erase Block high-voltage time for 256 KB	—	104	904	ms	1

1. Maximum time based on expectations at cycling end-of-life.

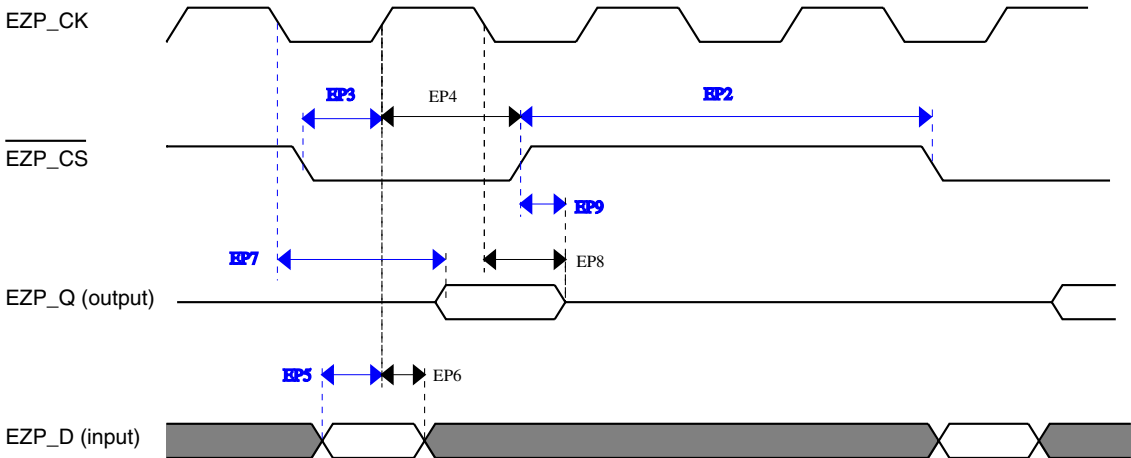


Figure 8. EzPort Timing Diagram

## 6.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

## 6.6 Analog

### 6.6.1 ADC electrical specifications

The 16-bit accuracy specifications listed in [Table 24](#) and [Table 25](#) are achievable on the differential pins ADCx\_DP0, ADCx\_DM0.

All other ADC channels meet the 13-bit differential/12-bit single-ended accuracy specifications.

#### 6.6.1.1 16-bit ADC operating conditions

Table 24. 16-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ. <sup>1</sup>	Max.	Unit	Notes
$V_{DDA}$	Supply voltage	Absolute	1.71	—	3.6	V	
$\Delta V_{DDA}$	Supply voltage	Delta to $V_{DD}$ ( $V_{DD} - V_{DDA}$ )	-100	0	+100	mV	<a href="#">2</a>
$\Delta V_{SSA}$	Ground voltage	Delta to $V_{SS}$ ( $V_{SS} - V_{SSA}$ )	-100	0	+100	mV	<a href="#">2</a>

Table continues on the next page...

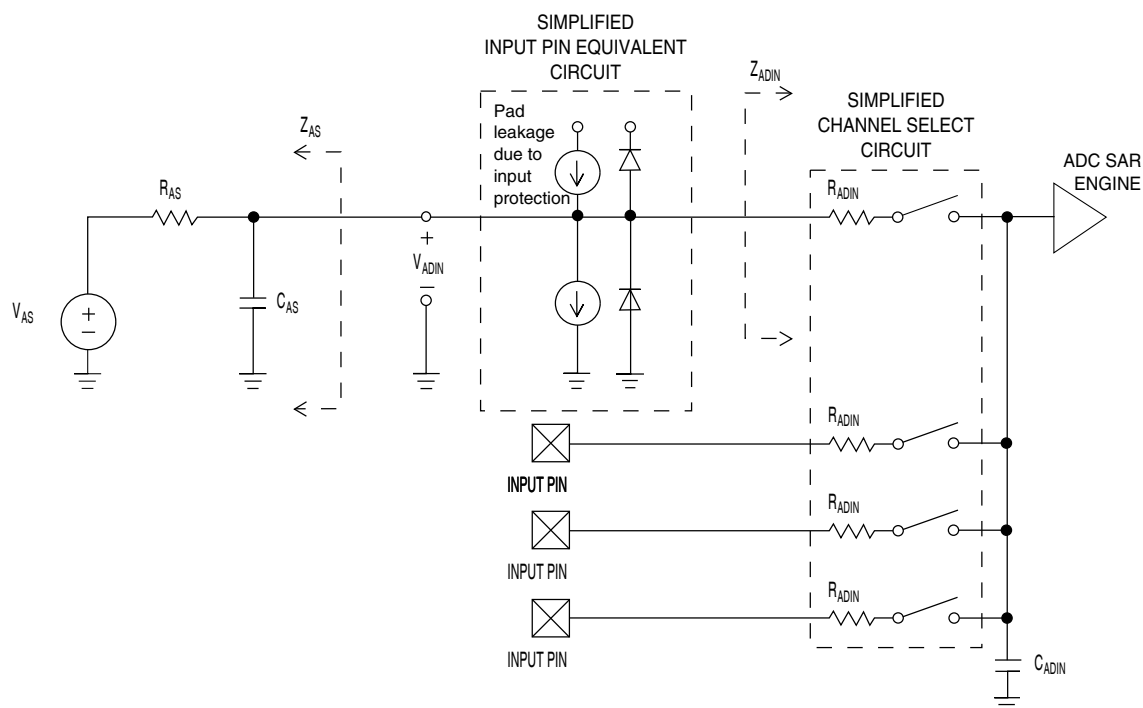


Figure 9. ADC input impedance equivalency diagram

### 6.6.1.2 16-bit ADC electrical characteristics

Table 25. 16-bit ADC characteristics ( $V_{REFH} = V_{DDA}$ ,  $V_{REFL} = V_{SSA}$ )

Symbol	Description	Conditions <sup>1</sup>	Min.	Typ. <sup>2</sup>	Max.	Unit	Notes
$I_{DDA\_ADC}$	Supply current		0.215	—	1.7	mA	3
$f_{ADACK}$	ADC asynchronous clock source	<ul style="list-style-type: none"> <li>ADLPC = 1, ADHSC = 0</li> <li>ADLPC = 1, ADHSC = 1</li> <li>ADLPC = 0, ADHSC = 0</li> <li>ADLPC = 0, ADHSC = 1</li> </ul>	1.2 2.4 3.0 4.4	2.4 4.0 5.2 6.2	3.9 6.1 7.3 9.5	MHz MHz MHz MHz	$t_{ADACK} = 1/f_{ADACK}$
	Sample Time	See Reference Manual chapter for sample times					
TUE	Total unadjusted error	<ul style="list-style-type: none"> <li>12-bit modes</li> <li>&lt;12-bit modes</li> </ul>	— —	±4 ±1.4	±6.8 ±2.1	LSB <sup>4</sup>	5
DNL	Differential non-linearity	<ul style="list-style-type: none"> <li>12-bit modes</li> <li>&lt;12-bit modes</li> </ul>	— —	±0.7 ±0.2	-1.1 to +1.9 -0.3 to 0.5	LSB <sup>4</sup>	5
INL	Integral non-linearity	<ul style="list-style-type: none"> <li>12-bit modes</li> <li>&lt;12-bit modes</li> </ul>	— —	±1.0 ±0.5	-2.7 to +1.9 -0.7 to +0.5	LSB <sup>4</sup>	5
$E_{FS}$	Full-scale error	<ul style="list-style-type: none"> <li>12-bit modes</li> <li>&lt;12-bit modes</li> </ul>	— —	-4 -1.4	-5.4 -1.8	LSB <sup>4</sup>	$V_{ADIN} = V_{DDA}$ 5

Table continues on the next page...

### 6.6.3.2 12-bit DAC operating behaviors

**Table 28. 12-bit DAC operating behaviors**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$I_{DDA\_DACLP}$	Supply current — low-power mode	—	—	330	$\mu A$	
$I_{DDA\_DACHP}$	Supply current — high-speed mode	—	—	1200	$\mu A$	
$t_{DACLP}$	Full-scale settling time (0x080 to 0xF7F) — low-power mode	—	100	200	$\mu s$	1
$t_{DACHP}$	Full-scale settling time (0x080 to 0xF7F) — high-power mode	—	15	30	$\mu s$	1
$t_{CCDACLP}$	Code-to-code settling time (0xBF8 to 0xC08) — low-power mode and high-speed mode	—	0.7	1	$\mu s$	1
$V_{dacoutl}$	DAC output voltage range low — high-speed mode, no load, DAC set to 0x000	—	—	100	mV	
$V_{dacouth}$	DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFFF	$V_{DACR} - 100$	—	$V_{DACR}$	mV	
INL	Integral non-linearity error — high speed mode	—	—	$\pm 8$	LSB	2
DNL	Differential non-linearity error — $V_{DACR} > 2$ V	—	—	$\pm 1$	LSB	3
DNL	Differential non-linearity error — $V_{DACR} = V_{REF\_OUT}$	—	—	$\pm 1$	LSB	4
$V_{OFFSET}$	Offset error	—	$\pm 0.4$	$\pm 0.8$	%FSR	5
$E_G$	Gain error	—	$\pm 0.1$	$\pm 0.6$	%FSR	5
PSRR	Power supply rejection ratio, $V_{DDA} \geq 2.4$ V	60	—	90	dB	
$T_{CO}$	Temperature coefficient offset voltage	—	3.7	—	$\mu V/C$	6
$T_{GE}$	Temperature coefficient gain error	—	0.000421	—	%FSR/C	
$R_{op}$	Output resistance (load = 3 k $\Omega$ )	—	—	250	$\Omega$	
SR	Slew rate -80h → F7Fh → 80h <ul style="list-style-type: none"> <li>High power (<math>SP_{HP}</math>)</li> <li>Low power (<math>SP_{LP}</math>)</li> </ul>	1.2 0.05	1.7 0.12	— —	V/ $\mu s$	
CT	Channel to channel cross talk	—	—	-80	dB	
BW	3dB bandwidth <ul style="list-style-type: none"> <li>High power (<math>SP_{HP}</math>)</li> <li>Low power (<math>SP_{LP}</math>)</li> </ul>	550 40	— —	— —	kHz	

- Settling within  $\pm 1$  LSB
- The INL is measured for 0 + 100 mV to  $V_{DACR} - 100$  mV
- The DNL is measured for 0 + 100 mV to  $V_{DACR} - 100$  mV
- The DNL is measured for 0 + 100 mV to  $V_{DACR} - 100$  mV with  $V_{DDA} > 2.4$  V
- Calculated by a best fit curve from  $V_{SS} + 100$  mV to  $V_{DACR} - 100$  mV
- $V_{DDA} = 3.0$  V, reference select set for  $V_{DDA}$  (DACx\_CO:DACRFS = 1), high power mode (DACx\_C0:LPEN = 0), DAC set to 0x800, temperature range is across the full range of the device

**Table 30. VREF full-range operating behaviors**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$V_{out}$	Voltage reference output with factory trim at nominal $V_{DDA}$ and temperature=25C	1.1915	1.195	1.1977	V	1
$V_{out}$	Voltage reference output — factory trim	1.1584	—	1.2376	V	1
$V_{out}$	Voltage reference output — user trim	1.193	—	1.197	V	1
$V_{step}$	Voltage reference trim step	—	0.5	—	mV	1
$V_{tdrift}$	Temperature drift ( $V_{max} - V_{min}$ across the full temperature range)	—	—	80	mV	1
$I_{bg}$	Bandgap only current	—	—	80	$\mu A$	1
$\Delta V_{LOAD}$	Load regulation • current = $\pm 1.0$ mA	—	200	—	$\mu V$	1, 2
$T_{stup}$	Buffer startup time	—	—	100	$\mu s$	
$V_{vdift}$	Voltage drift ( $V_{max} - V_{min}$ across the full voltage range)	—	2	—	mV	1

1. See the chip's Reference Manual for the appropriate settings of the VREF Status and Control register.
2. Load regulation voltage is the difference between the VREF\_OUT voltage with no load vs. voltage with defined load

**Table 31. VREF limited-range operating requirements**

Symbol	Description	Min.	Max.	Unit	Notes
$T_A$	Temperature	0	50	$^{\circ}C$	

**Table 32. VREF limited-range operating behaviors**

Symbol	Description	Min.	Max.	Unit	Notes
$V_{out}$	Voltage reference output with factory trim	1.173	1.225	V	

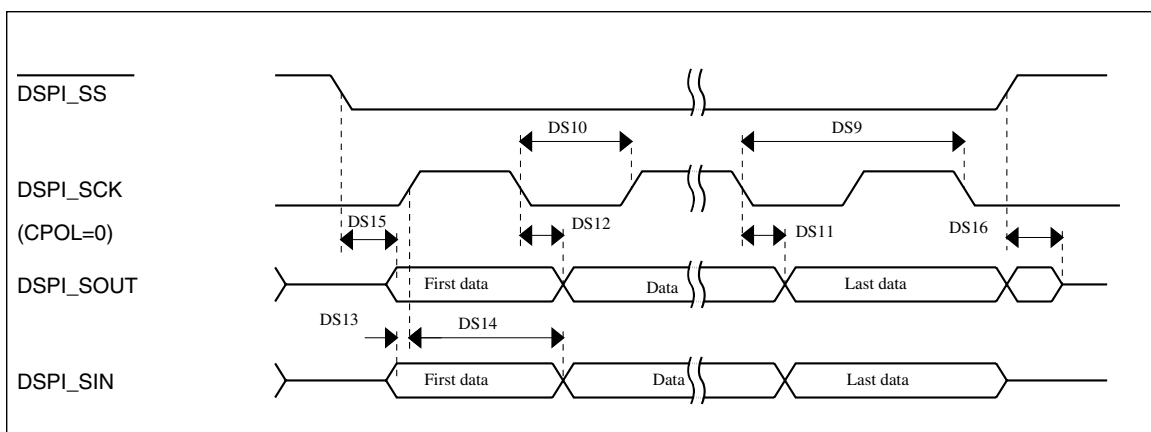
## 6.7 Timers

See [General switching specifications](#).

## 6.8 Communication interfaces

**Table 34. Slave mode DSPI timing (limited voltage range) (continued)**

Num	Description	Min.	Max.	Unit
DS10	DSPI_SCK input high/low time	$(t_{\text{SCK}}/2) - 2$	$(t_{\text{SCK}}/2) + 2$	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	10	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	DSPI_SS active to DSPI_SOUT driven	—	14	ns </td
DS16	DSPI_SS inactive to DSPI_SOUT not driven	—	14	ns


**Figure 17. DSPI classic SPI timing — slave mode**

## 6.8.2 DSPI switching specifications (full voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provides DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

**Table 35. Master mode DSPI timing (full voltage range)**

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	1
	Frequency of operation	—	12.5	MHz	
DS1	DSPI_SCK output cycle time	$4 \times t_{\text{BUS}}$	—	ns	
DS2	DSPI_SCK output high/low time	$(t_{\text{SCK}}/2) - 4$	$(t_{\text{SCK}}/2) + 4$	ns	
DS3	DSPI_PCSn valid to DSPI_SCK delay	$(t_{\text{BUS}} \times 2) - 4$	—	ns	2

Table continues on the next page...

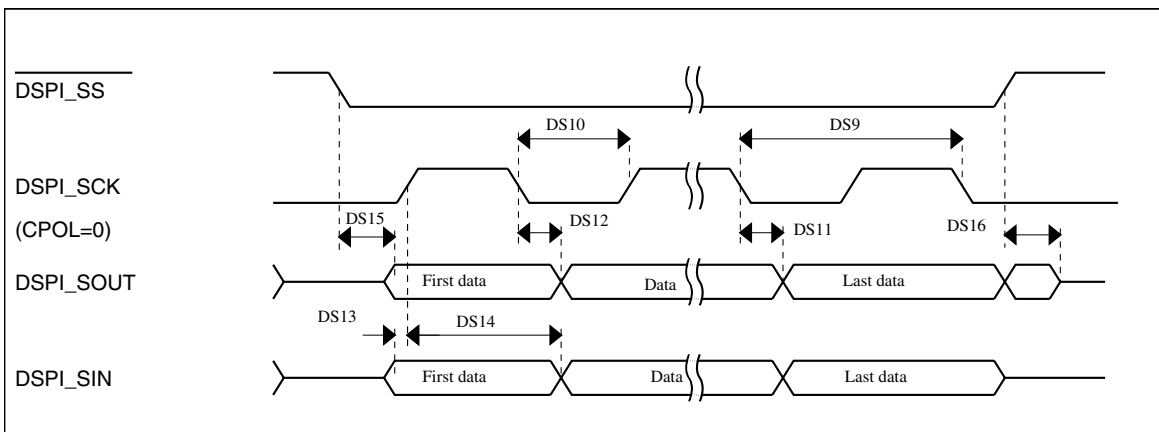


Figure 19. DSPI classic SPI timing — slave mode

### 6.8.3 I<sup>2</sup>C switching specifications

See [General switching specifications](#).

### 6.8.4 UART switching specifications

See [General switching specifications](#).

### 6.8.5 Normal Run, Wait and Stop mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in Normal Run, Wait and Stop modes.

Table 37. I2S/SAI master mode timing

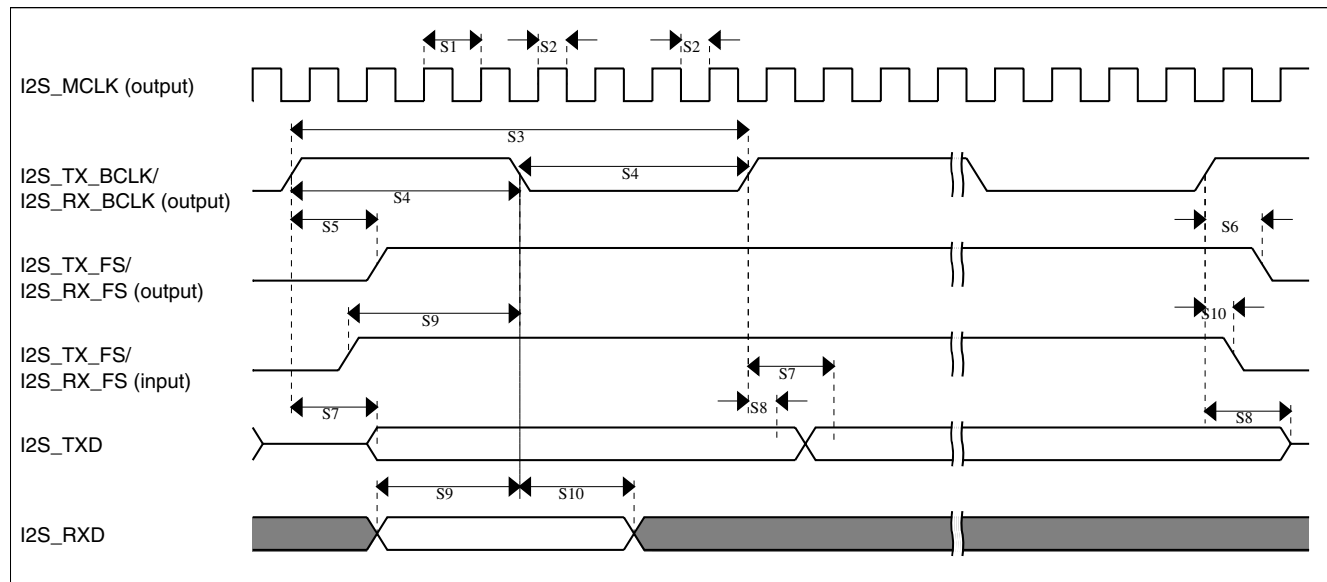
Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	40	—	ns
S2	I2S_MCLK (as an input) pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	80	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	15	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	0	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	15	ns

Table continues on the next page...



**Table 37. I2S/SAI master mode timing (continued)**

Num.	Characteristic	Min.	Max.	Unit
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	25	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns

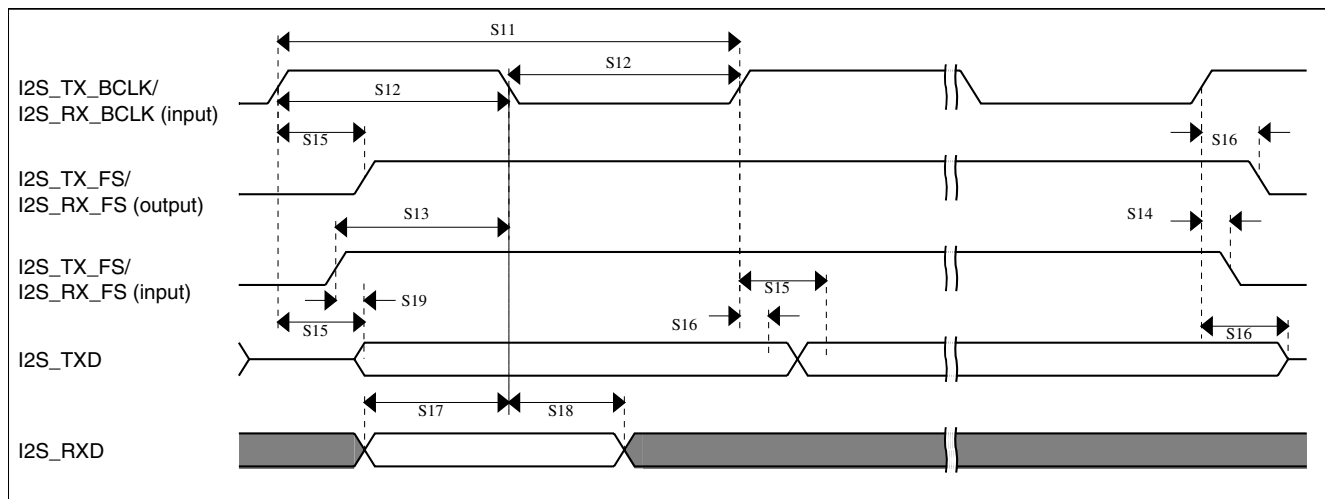


**Figure 20. I2S/SAI timing — master modes**

**Table 38. I2S/SAI slave mode timing**

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	80	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	10	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	2	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	29	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	10	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid <sup>1</sup>	—	21	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear



**Figure 21. I2S/SAI timing — slave modes**

### 6.8.6 VLPR, VLPW, and VLPS mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in VLPR, VLPW, and VLPS modes.

**Table 39. I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes (full voltage range)**

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	62.5	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	250	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/I2S_RX_FS output valid	—	45	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/I2S_RX_FS output invalid	0	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	45	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	75	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns

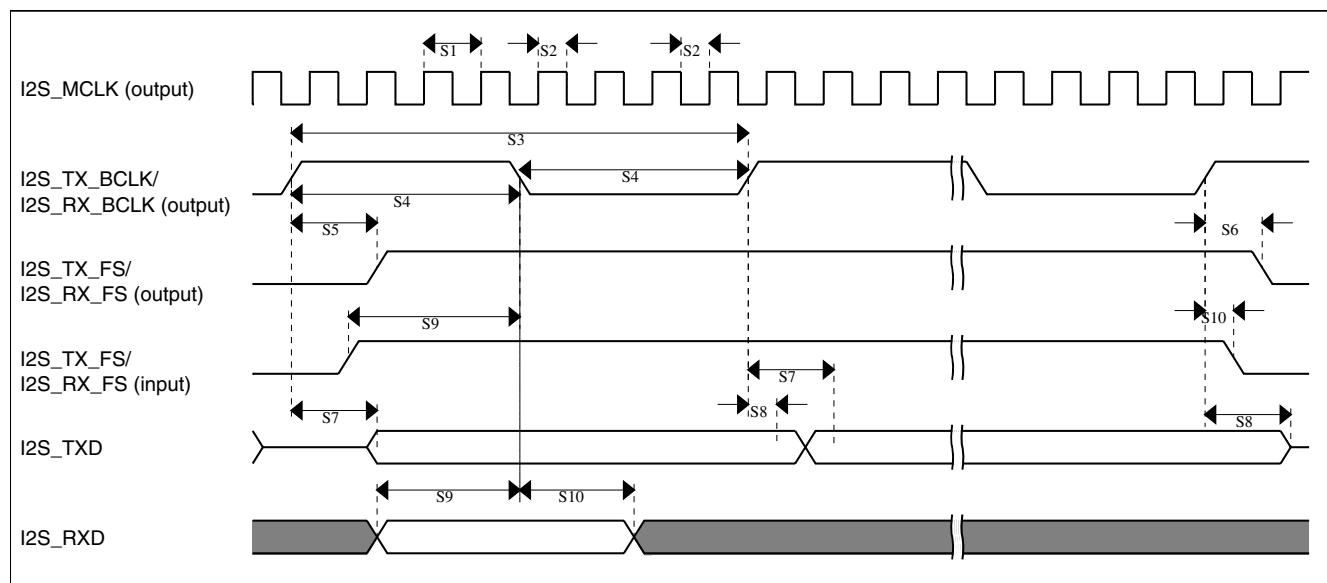


Figure 22. I2S/SAI timing — master modes

Table 40. I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	250	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	30	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	2	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	87	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	30	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid <sup>1</sup>	—	72	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

## 8.2 K12 Pinouts

The below figure shows the pinout diagram for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see the previous section.

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