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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	18MHz
Connectivity	UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	8
Program Memory Size	1KB (1K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	10-VFDFN Exposed Pad
Supplier Device Package	10-HVSON (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p89lpc9103ftk-115

- In-Application Programming (IAP-Lite) and byte erase allows code memory to be used for non-volatile data storage.
- Serial flash ICP allows simple production coding with commercial EPROM programmers. Flash security bits prevent reading of sensitive application programs.
- Watchdog timer with separate on-chip oscillator, requiring no external components. The watchdog prescaler is selectable from eight values.
- Low voltage reset (Brownout detect) allows a graceful system shutdown when power fails. May optionally be configured as an interrupt.
- Idle mode and two different reduced power Power-down modes. Improved wake-up from Power-down mode (a LOW interrupt input starts execution). Typical Power-down mode current is **less than 1 μA** (total Power-down mode with voltage comparators disabled).
- Active-LOW reset. On-chip power-on reset allows operation without external reset components. A reset counter and reset glitch suppression circuitry prevent spurious and incomplete resets. A software reset function is also available.
- Programmable port output configuration options: quasi-bidirectional, open drain, push-pull, input-only.
- Port ‘input pattern match’ detect. Port 0 may generate an interrupt when the value of the pins match or do not match a programmable pattern.
- LED drive capability (20 mA) on all port pins. A maximum limit is specified for the entire chip.
- Controlled slew rate port outputs to reduce EMI. Outputs have approximately 10 ns minimum ramp times.
- Only power and ground connections are required to operate the P89LPC9102/9103/9107 when internal reset option is selected.
- Four interrupt priority levels.
- Two keypad interrupt inputs.
- Second data pointer.
- External clock input.
- Clock output (P89LPC9102/9107).
- Schmitt trigger port inputs.
- Emulation support.

3. Product comparison overview

Table 1 highlights the differences between these two devices. For a complete list of device features, please see Section 2 “Features”.

Table 1. Product comparison overview

Type number	UART	T0 toggle/PWM	T1 toggle/PWM	CLKOUT
P89LPC9102	-	X	X	X
P89LPC9103	X	-	-	-
P89LPC9107	X	X	X	X

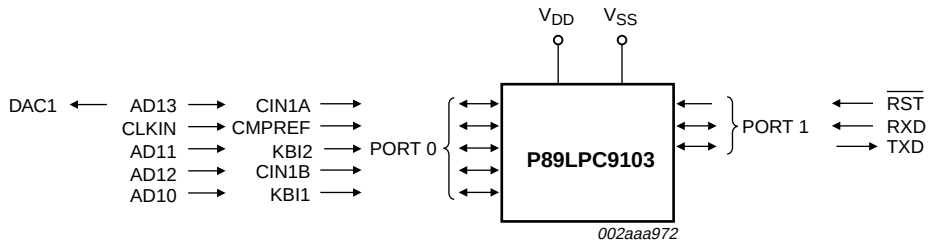


Fig 5. Functional diagram of P89LPC9103

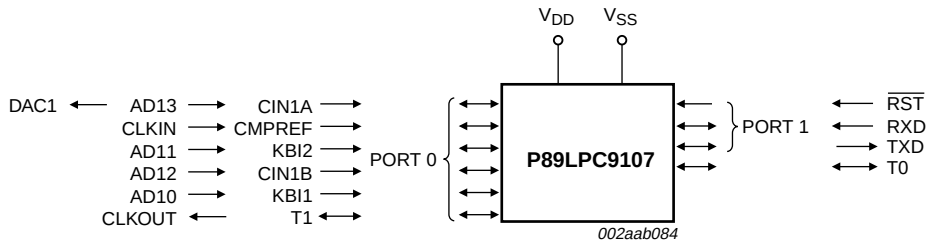


Fig 6. Functional diagram of P89LPC9107

Table 5. P89LPC9103 pin description

Symbol	Pin	Type	Description
P0.1 to P0.5		I/O	**Port 0:** Port 0 is an I/O port with a user-configurable output type. During reset Port 0 latches are configured in the input-only mode with the internal pull-up disabled. The operation of Port 0 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 8.12.1 "Port configurations" and Table 12 "Static characteristics" for details. The Keypad Interrupt feature operates with Port 0 pins. All pins have Schmitt triggered inputs. Port 0 also provides various special functions as described below:
P0.1/KBI1/ AD10	4	I/O	**P0.1 —** Port 0 bit 1.
		I	**KBI1 —** Keyboard input 1.
		I	**AD10 —** ADC1 channel 0 analog input.
P0.2/KBI2/ AD11	1	I/O	**P0.2 —** Port 0 bit 2.
		I	**KBI2 —** Keyboard input 2.
		I	**AD11 —** ADC1 channel 1 analog input.
P0.3/CIN1B/ AD12	10	I/O	**P0.3 —** Port 0 bit 3.
		I	**CIN1B —** Comparator 1 positive input.
		I	**AD12 —** ADC1 channel 2 analog input.
P0.4/CIN1A/ AD13/DAC1	9	I/O	**P0.4 —** Port 0 bit 4.
		I	**CIN1A —** Comparator 1 positive input.
		I	**AD13 —** ADC1 channel 3 analog input.
		O	**DAC1 —** Digital to analog converter output.
P0.5/CMPREF/ CLKIN	6	I/O	**P0.5 —** Port 0 bit 5.
		I	**CMPREF —** Comparator reference (negative) input.
		I	**CLKIN —** External clock input.
P1.0 to P1.5		I/O	**Port 1:** Port 1 is an I/O port with a user-configurable output type. During reset Port 1 latches are configured in the input-only mode with the internal pull-up disabled. The operation of the configurable Port 1 pins as inputs and outputs depends upon the port configuration selected. Each of the configurable port pins are programmed independently. Refer to Section 8.12.1 "Port configurations" and Table 12 "Static characteristics" for details. P1.5 is input-only. All pins have Schmitt triggered inputs. Port 1 also provides various special functions as described below:
P1.0/TXD	5	I/O	**P1.0 —** Port 1 bit 0.
		O	**TXD —** Serial port transmitter data.
P1.1/RXD	6	I/O	**P1.1 —** Port 1 bit 1.
		I	**RXD —** Serial port receiver data.

Table 5. P89LPC9103 pin description *…continued*

Symbol	Pin	Type	Description
P1.5/$\overline{\text{RST}}$	2	I	**P1.5 —** Port 1 bit 5 (input-only).
		I	**$\overline{\text{RST}}$ —** External Reset input during Power-on or if selected via UCFG1. When functioning as a reset input a LOW on this pin resets the microcontroller, causing I/O ports and peripherals to take on their default states, and the processor begins execution at address 0. **When using an oscillator frequency above 12 MHz, the reset input function of P1.5 must be enabled. An external circuit is required to hold the device in reset at power-up until V_{DD} has reached its specified level. When system power is removed V_{DD} will fall below the minimum specified operating voltage. When using an oscillator frequency above 12 MHz, in some applications, an external brownout detect circuit may be required to hold the device in reset when V_{DD} falls below the minimum specified operating voltage.**
V_{SS}	3	I	**Ground:** 0 V reference.
V_{DD}	7	I	**Power supply:** This is the power supply voltage for normal operation as well as Idle mode and Power-down mode.

Table 6. P89LPC9107 pin description

Symbol	Pin	Type	Description
P0.1 to P0.5, P0.7		I/O	**Port 0:** Port 0 is an I/O port with a user-configurable output type. During reset Port 0 latches are configured in the input-only mode with the internal pull-up disabled. The operation of Port 0 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 8.12.1 “Port configurations” and Table 12 “Static characteristics” for details. The Keypad Interrupt feature operates with Port 0 pins. All pins have Schmitt triggered inputs. Port 0 also provides various special functions as described below:
P0.1/KBI1/ AD10	5	I/O	**P0.1 —** Port 0 bit 1.
		I	**KBI1 —** Keyboard input 1.
		I	**AD10 —** ADC1 channel 0 analog input.
P0.2/KBI2/ AD11	1	I/O	**P0.2 —** Port 0 bit 2.
		I	**KBI2 —** Keyboard input 2.
		I	**AD11 —** ADC1 channel 1 analog input.
P0.3/CIN1B/ AD12	14	I/O	**P0.3 —** Port 0 bit 3.
		I	**CIN1B —** Comparator 1 positive input.
		I	**AD12 —** ADC1 channel 2 analog input.
P0.4/CIN1A/ AD13/DAC1	12	I/O	**P0.4 —** Port 0 bit 4.
		I	**CIN1A —** Comparator 1 positive input.
		I	**AD13 —** ADC1 channel 3 analog input.
		O	**DAC1 —** Digital to analog converter output.
P0.5/CMPREF/ CLKIN	11	I/O	**P0.5 —** Port 0 bit 5.
		I	**CMPREF —** Comparator reference (negative) input.
		I	**CLKIN —** External clock input.
P0.7/T1/ CLKOUT	8	I/O	**P0.7 —** Port 0 bit 7.
		I/O	**T1 —** Timer/counter 1 external count input or overflow/PWM output.
		I	**CLKOUT —** Clock output.

Table 8. P89LPC9103 special function registers *…continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
	Bit address		D7	D6	D5	D4	D3	D2	D1	D0		
PSW*	Program status word	D0H	CY	AC	F0	RS1	RS0	OV	F1	P	00	0000 0000
PT0AD	Port 0 digital input disable	F6H	-	-	PT0AD.5	PT0AD.4	PT0AD.3	PT0AD.2	PT0AD.1	-	00	xx00 000x
RSTSRC	Reset source register	DFH	-	-	BOF	POF	R_BK	R_WD	R_SF	R_EX	[4]	
RTCCON	Real-time clock control	D1H	RTCF	RTCS1	RTCS0	-	-	-	ERTC	RTCEN	60[5]	011x xx00
RTCH	Real-time clock register high	D2H									00[5]	0000 0000
RTCL	Real-time clock register low	D3H									00[5]	0000 0000
SADDR	Serial port address register	A9H									00	0000 0000
SADEN	Serial port address enable	B9H									00	0000 0000
SBUF	Serial port data buffer register	99H									xx	xxxx xxxx
	Bit address		9F	9E	9D	9C	9B	9A	99	98		
SCON*	Serial port control	98H	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI	00	0000 0000
SSTAT	Serial port extended status register	BAH	DBMOD	INTLO	CIDIS	DBISEL	FE	BR	OE	STINT	00	0000 0000
SP	Stack pointer	81H									07	0000 0111
	Bit address		8F	8E	8D	8C	8B	8A	89	88		
TCON*	Timer 0 and 1 control	88H	TF1	TR1	TF0	TR0	-	-	-	-	00	0000 0000
TH0	Timer 0 high	8CH									00	0000 0000
TH1	Timer 1 high	8DH									00	0000 0000
TL0	Timer 0 low	8AH									00	0000 0000
TL1	Timer 1 low	8BH									00	0000 0000
TMOD	Timer 0 and 1 mode	89H	-	-	T1M1	T1M0	-	-	T0M1	T0M0	00	0000 0000
TRIM	Internal oscillator trim register	96H	RCCLK	-	TRIM.5	TRIM.4	TRIM.3	TRIM.2	TRIM.1	TRIM.0	[5][6]	
WDCON	Watchdog control register	A7H	PRE2	PRE1	PRE0	-	-	WDRUN	WDTOF	WDCLK	[5][7]	
WDL	Watchdog load	C1H									FF	1111 1111
WFEED1	Watchdog feed 1	C2H										
WFEED2	Watchdog feed 2	C3H										

[1] Unimplemented bits in SFRs (labeled '-') are X (unknown) at all times. Unless otherwise specified, ones should not be written to these bits since they may be used for other purposes in future derivatives. The reset values shown for these bits are logic 0s although they are unknown when read.

[2] BRGR1 and BRGR0 must only be written if BRGEN in BRGCON SFR is logic 0. If any are written while BRGEN = 1, the result is unpredictable.

8.5 Watchdog oscillator option

The watchdog timer has a separate oscillator which has a frequency of 400 kHz. This oscillator can be used to save power when a high clock frequency is not needed.

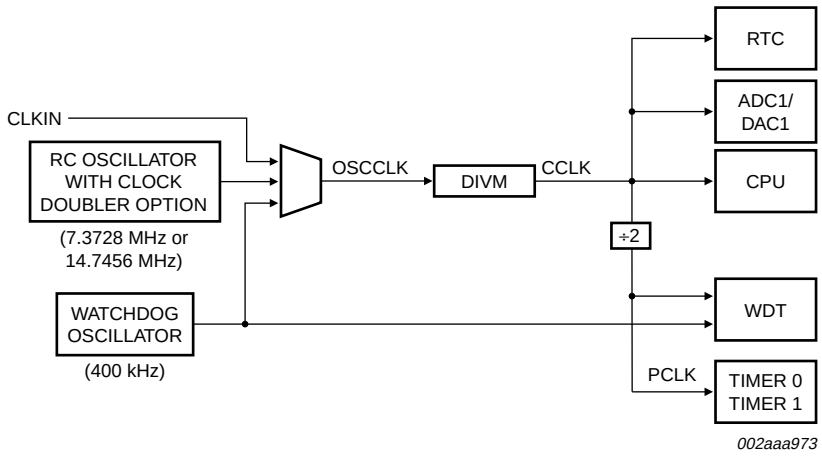


Fig 11. Block diagram of P89LPC9102 oscillator control

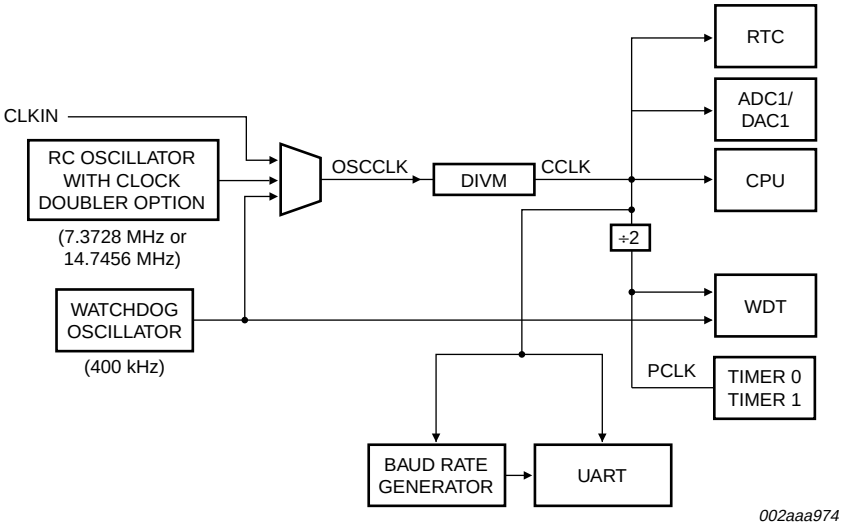


Fig 12. Block diagram of P89LPC9103/9107 oscillator control

8.6 External clock input option

In this configuration, the processor clock is derived from an external source driving the P0.5/CMPREF/CLKIN pin. The rate may be from 0 Hz up to 18 MHz. The P0.5/CMPREF/CLKIN pin may also be used as a standard port pin. **When using an oscillator frequency above 12 MHz, the reset input function of P1.5 must be enabled. An external circuit is required to hold the device in reset at power-up until V_{DD} has reached its specified level. When system power is removed V_{DD} will fall below the minimum specified operating voltage. When using an oscillator**

Each interrupt source can be individually programmed to one of four priority levels by setting or clearing bits in the interrupt priority registers IP0, IP0H, IP1, and IP1H. An interrupt service routine in progress can be interrupted by a higher priority interrupt, but not by another interrupt of the same or lower priority. The highest priority interrupt service cannot be interrupted by any other interrupt source. If two requests of different priority levels are pending at the start of an instruction, the request of higher priority level is serviced.

If requests of the same priority level are pending at the start of an instruction, an internal polling sequence determines which request is serviced. This is called the arbitration ranking. Note that the arbitration ranking is only used to resolve pending requests of the same priority level.

8.11.1 External interrupt inputs

The P89LPC9102/9103/9107 has a Keypad Interrupt function. This can be used as an external interrupt input.

If enabled when the P89LPC9102/9103/9107 is put into Power-down mode or Idle mode, the interrupt will cause the processor to wake-up and resume operation. Refer to Section 8.14 “Power reduction modes” for details.

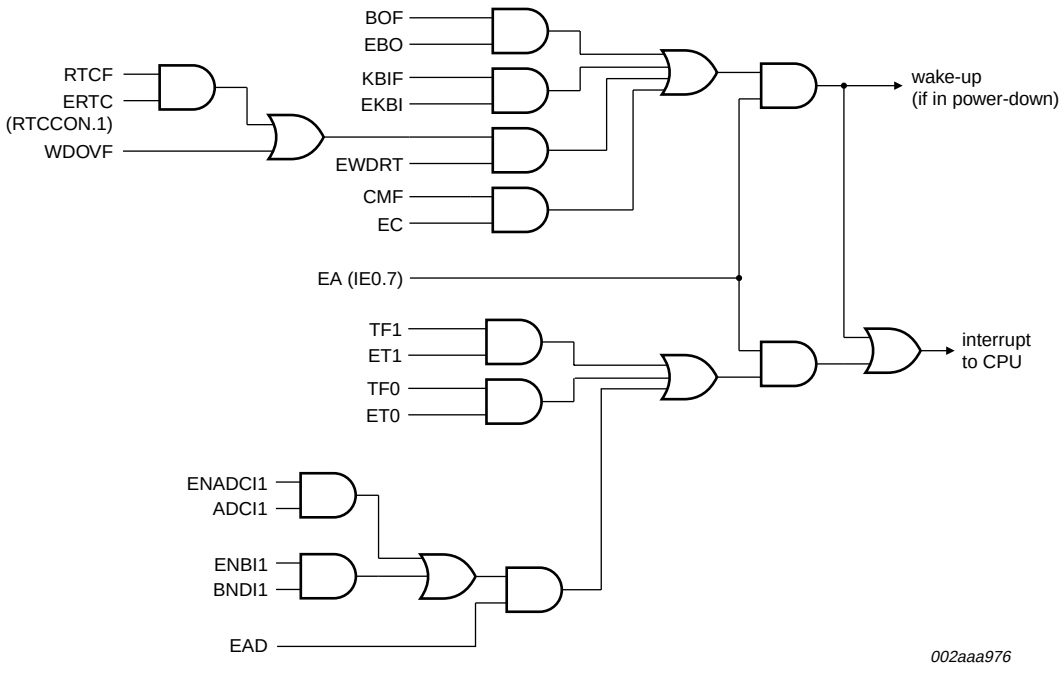


Fig 13. Interrupt sources, interrupt enables, and power-down wake-up sources (P89LPC9102)

8.12.2 Quasi-bidirectional output configuration

Quasi-bidirectional output type can be used as both an input and output without the need to reconfigure the port. This is possible because when the port outputs a logic HIGH, it is weakly driven, allowing an external device to pull the pin LOW. When the pin is driven LOW, it is driven strongly and able to sink a fairly large current. These features are somewhat similar to an open-drain output except that there are three pull-up transistors in the quasi-bidirectional output that serve different purposes.

The P89LPC9102/9103/9107 is a 3 V device, however, the pins are 5 V-tolerant. In quasi-bidirectional mode, if a user applies 5 V on the pin, there will be a current flowing from the pin to V_{DD}, causing extra power consumption. Therefore, applying 5 V in quasi-bidirectional mode is discouraged.

A quasi-bidirectional port pin has a Schmitt triggered input that also has a glitch suppression circuit.

8.12.3 Open-drain output configuration

The open-drain output configuration turns off all pull-ups and only drives the pull-down transistor of the port driver when the port latch contains a logic 0. To be used as a logic output, a port configured in this manner must have an external pull-up, typically a resistor tied to V_{DD}.

An open-drain port pin has a Schmitt triggered input that also has a glitch suppression circuit.

8.12.4 Input-only configuration

The input-only port configuration has no output drivers. It is a Schmitt triggered input that also has a glitch suppression circuit.

8.12.5 Push-pull output configuration

The push-pull output configuration has the same pull-down structure as both the open-drain and the quasi-bidirectional output modes, but provides a continuous strong pull-up when the port latch contains a logic 1. The push-pull mode may be used when more source current is needed from a port output. A push-pull port pin has a Schmitt triggered input that also has a glitch suppression circuit.

8.12.6 Port 0 analog functions

The P89LPC9102/9103/9107 incorporates an Analog Comparator. In order to give the best analog function performance and to minimize power consumption, pins that are being used for analog functions must have the digital outputs and digital inputs disabled.

Digital outputs are disabled by putting the port output into the Input-only (high-impedance) mode as described in Section 8.12.4 “Input-only configuration”.

Digital inputs on Port 0 may be disabled through the use of the PT0AD register. On any reset, the PT0AD bits default to logic 0s to enable digital functions.

8.12.7 Additional port features

After power-up, all pins are in Input-only mode. **Please note that this is different from the LPC76x series of devices.**

- After power-up all I/O pins, except P1.5, may be configured by software.
- Pin P1.5 is input-only.

Every output on the P89LPC9102/9103/9107 has been designed to sink typical LED drive current. However, there is a maximum total output current for all ports which must not be exceeded. Please refer to Table 12 “Static characteristics” for detailed specifications.

All ports pins that can function as an output have slew rate controlled outputs to limit noise generated by quickly switching output signals. The slew rate is factory-set to approximately 10 ns rise and fall times.

8.13 Power monitoring functions

The P89LPC9102/9103/9107 incorporates power monitoring functions designed to prevent incorrect operation during initial power-up and power loss or reduction during operation. This is accomplished with two hardware functions: Power-on Detect and Brownout detect.

8.13.1 Brownout detection

The Brownout detect function determines if the power supply voltage drops below a certain level. The default operation is for a Brownout detection to cause a processor reset, however, it may alternatively be configured to generate an interrupt.

Brownout detection may be enabled or disabled in software.

If Brownout detection is enabled, the brownout condition occurs when V_{DD} falls below the brownout trip voltage, V_{bo} (see Table 12 “Static characteristics”), and is negated when V_{DD} rises above V_{bo}. If the P89LPC9102/9103/9107 device is to operate with a power supply that can be below 2.7 V, Brownout detect Enable (BOE) should be left in the unprogrammed state so that the device can operate at 2.4 V, otherwise continuous brownout reset may prevent the device from operating.

For correct activation of Brownout detect, the V_{DD} rise and fall times must be observed. Please see Table 12 “Static characteristics” for specifications.

8.13.2 Power-on detection

The Power-on Detect has a function similar to the Brownout detect, but is designed to work as power comes up initially, before the power supply voltage reaches a level where Brownout detect can work. The Power-on detect flag (POF) in the RSTSRC register is set to indicate an initial power-up condition. The POF flag will remain set until cleared by software.

8.14 Power reduction modes

The P89LPC9102/9103/9107 supports three different power reduction modes. These modes are Idle mode, Power-down mode, and Total Power-down mode.

8.14.1 Idle mode

Idle mode leaves peripherals running in order to allow them to activate the processor when an interrupt is generated. Any enabled interrupt source or reset may terminate Idle mode.

- Power-on detect
- Brownout detect
- Watchdog timer
- Software reset
- UART break character detect reset (P89LPC9103/9107).

For every reset source, there is a flag in the Reset Register, RSTSRC. The user can read this register to determine the most recent reset source. These flag bits can be cleared in software by writing a logic 0 to the corresponding bit. More than one flag bit may be set:

- During a power-on reset, both POF and BOF are set but the other flag bits are cleared.
- For any other reset, previously set flag bits that have not been cleared will remain set.

8.16 Timers 0 and 1

The P89LPC9102 has two general purpose timer/counters which are similar to the standard 80C51 Timer 0 and Timer 1. These timers have five operating modes (modes 0, 1, 2, 3, and 6). Modes 0, 1, and 2 are the same for both Timers. Mode 3 is different.

The P89LPC9103/9107 has two general purpose timers which are similar to the standard 80C51 Timer 0 and Timer 1. These timers have four operating modes (modes 0, 1, 2, and 3). Modes 0, 1, and 2 are the same for both Timers. Mode 3 is different.

8.16.1 Mode 0

Putting either Timer into Mode 0 makes it look like an 8048 Timer, which is an 8-bit Counter with a divide-by-32 prescaler. In this mode, the Timer register is configured as a 13-bit register. Mode 0 operation is the same for Timer 0 and Timer 1.

8.16.2 Mode 1

Mode 1 is the same as Mode 0, except that all 16 bits of the timer register are used.

8.16.3 Mode 2

Mode 2 configures the Timer register as an 8-bit counter with automatic reload. Mode 2 operation is the same for Timer 0 and Timer 1.

8.16.4 Mode 3

When Timer 1 is in Mode 3 it is stopped. Timer 0 in Mode 3 forms two separate 8-bit counters and is provided for applications that require an extra 8-bit timer. When Timer 1 is in Mode 3 it can still be used by the serial port as a baud rate generator.

8.16.5 Mode 6 (P89LPC9102/9107)

In this mode, the corresponding timer can be changed to a PWM with a full period of 256 timer clocks.

8.21 Comparator interrupt

The comparator has an interrupt flag contained in its configuration register. This flag is set whenever the comparator output changes state. The flag may be polled by software or may be used to generate an interrupt.

8.22 Comparator and power reduction modes

The comparator may remain enabled when Power-down mode or Idle mode is activated, but the comparator is disabled automatically in Total Power-down mode.

If the comparator interrupt is enabled (except in Total Power-down mode), a change of the comparator output state will generate an interrupt and wake-up the processor. If the comparator output to a pin is enabled, the pin should be configured in the push-pull mode in order to obtain fast switching times while in Power-down mode. The reason is that with the oscillator stopped, the temporary strong pull-up that normally occurs during switching on a quasi-bidirectional port pin does not take place.

The comparator consumes power in Power-down mode and Idle mode, as well as in the normal operating mode. This fact should be taken into account when system power consumption is an issue. To minimize power consumption, the user can disable the comparator via PCONA.5 or put the device in Total Power-down mode.

8.23 Keypad interrupt (KBI)

The Keypad Interrupt function is intended primarily to allow a single interrupt to be generated when Port 0 is equal to or not equal to a certain pattern. This function can be used for bus address recognition or keypad recognition. The user can configure the port via SFRs for different tasks.

The Keypad Interrupt Mask Register (KBMASK) is used to define which input pins connected to Port 0 can trigger the interrupt. The Keypad Pattern Register (KBPATN) is used to define a pattern that is compared to the value of Port 0. The Keypad Interrupt Flag (KBIF) in the Keypad Interrupt Control Register (KBCON) is set when the condition is matched while the Keypad Interrupt function is active. An interrupt will be generated if enabled. The PATN_SEL bit in the Keypad Interrupt Control Register (KBCON) is used to define equal or not-equal for the comparison.

In order to use the Keypad Interrupt as an original KBI function like in 87LPC76x series, the user needs to set KBPATN = 0FFH and PATN_SEL = 1 (not equal), then any key connected to Port 0 which is enabled by the KBMASK register will cause the hardware to set KBIF and generate an interrupt if it has been enabled. The interrupt may be used to wake-up the CPU from Idle mode or Power-down mode. This feature is particularly useful in handheld, battery powered systems that need to carefully manage power consumption yet also need to be convenient to use.

In order to set the flag and cause an interrupt, the pattern on Port 0 must be held longer than six CCLKs.

8.24 Watchdog timer

The watchdog timer causes a system reset when it underflows as a result of a failure to feed the timer prior to the timer reaching its terminal count. It consists of a programmable 12-bit prescaler, and an 8-bit down counter. The down counter is decremented by a tap

8.26 Flash program memory

8.26.1 General description

The P89LPC9102/9103/9107 flash memory provides in-circuit electrical erasure and programming. The flash can be erased, read, and written as bytes. The Sector and Page Erase functions can erase any flash sector (256 bytes) or page (16 bytes). The Chip Erase operation will erase the entire program memory. In-Circuit Programming using standard commercial programmers is available. In addition, In-Application Programming Lite (IAP-Lite) and byte erase allows code memory to be used for non-volatile data storage. On-chip erase and write timing generation contribute to a user-friendly programming interface. The P89LPC9102/9103/9107 flash reliably stores memory contents even after more than 400000 erase and program cycles. The cell is designed to optimize the erase and programming mechanisms. The P89LPC9102/9103/9107 uses V_{DD} as the supply voltage to perform the Program/Erase algorithms.

8.26.2 Features

- Programming and erase over the full operating voltage range.
- Byte-erase allowing code memory to be used for data storage.
- Read/Programming/Erase using ICP.
- Any flash program/erase operation in 2 ms.
- Programming with industry-standard commercial programmers.
- Programmable security for the code in the flash for each sector.
- More than 400000 minimum erase/program cycles for each byte.
- 20-year minimum data retention.

8.26.3 Flash organization

The P89LPC9102/9103/9107 program memory consists of four 256 byte sectors. Each sector can be further divided into 16-byte pages. In addition to sector erase, page erase, and byte erase, a 16-byte page register is included which allows from 1 byte to 16 bytes of a given page to be programmed at the same time, substantially reducing overall programming time. In addition, erasing and reprogramming of user-programmable configuration bytes including UCFG1, the Boot Status Bit, and the Boot Vector is supported.

8.26.4 Flash programming and erasing

Different methods of erasing or programming of the flash are available. The flash may be programmed or erased in the end-user application (IAP-Lite) under control of the application's firmware. Another option is to use the ICP mechanism. This ICP system provides for programming through a serial clock- serial data interface. Third, the flash may be programmed or erased using a commercially available EPROM programmer which supports this device. This device does not provide for direct verification of code memory contents. Instead this device provides a 32-bit CRC result on either a sector or the entire 1 kB of user code space.

9. A/D Converter

9.1 General description

The P89LPC9102/9103/9107 has an 8-bit, 4-channel multiplexed successive approximation analog-to-digital converter. The A/D consists of a 4-input multiplexer which feeds a sample-and-hold circuit providing an input signal to one of two comparator inputs. The control logic in combination with the Successive Approximation Register (SAR) drives a digital-to-analog converter which provides the other input to the comparator. The output of the comparator is fed to the SAR. A block diagram of the A/D converter is shown in Figure 18.

9.2 Features

- 8-bit, 4-channel multiplexed input, successive approximation A/D converter
- Four result registers
- Six operating modes
  - Fixed channel, single conversion mode
  - Fixed channel, continuous conversion mode
  - Auto scan, single conversion mode
  - Auto scan, continuous conversion mode
  - Dual channel, continuous conversion mode
  - Single step mode
- Two conversion start modes
  - Timer triggered start
  - Start immediately
- 8-bit conversion time of ≥ 3.9 µs at an ADC clock of 3.3 MHz
- Interrupt or polled operation
- Boundary limits interrupt
- DAC output to a port pin with high output impedance
- Clock divider
- Power-down mode

9.3 Block diagram

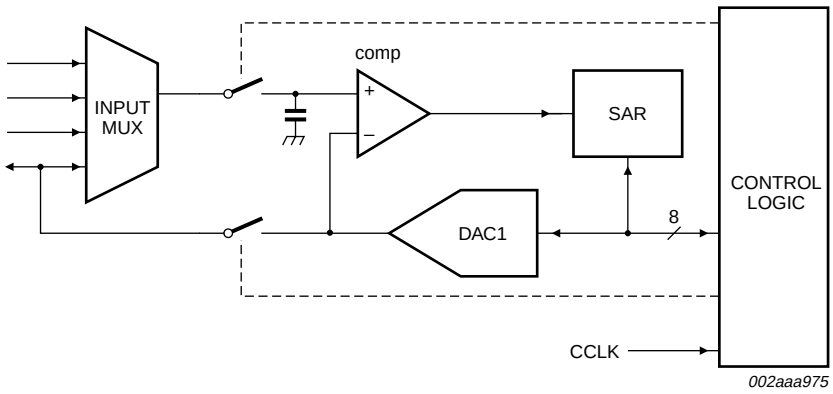


Fig 18. ADC block diagram

9.4 A/D operating modes

9.4.1 Fixed channel, single conversion mode

A single input channel can be selected for conversion. A single conversion will be performed and the result placed in the result register which corresponds to the selected input channel. An interrupt, if enabled, will be generated after the conversion completes.

9.4.2 Fixed channel, continuous conversion mode

A single input channel can be selected for continuous conversion. The results of the conversions will be sequentially placed in the four result registers. An interrupt, if enabled, will be generated after every four conversions. Additional conversion results will again cycle through the four result registers, overwriting the previous results. Continuous conversions continue until terminated by the user.

9.4.3 Auto scan, single conversion mode

Any combination of the four input channels can be selected for conversion. A single conversion of each selected input will be performed and the result placed in the result register which corresponds to the selected input channel. An interrupt, if enabled, will be generated after all selected channels have been converted. If only a single channel is selected this is equivalent to single channel, single conversion mode.

9.4.4 Auto scan, continuous conversion mode

Any combination of the four input channels can be selected for conversion. A conversion of each selected input will be performed and the result placed in the result register which corresponds to the selected input channel. An interrupt, if enabled, will be generated after all selected channels have been converted. The process will repeat starting with the first selected channel. Additional conversion results will again cycle through the four result registers, overwriting the previous results. Continuous conversions continue until terminated by the user.

9.4.5 Dual channel, continuous conversion mode

This is a variation of the auto scan continuous conversion mode where conversion occurs on two user-selectable inputs. The result of the conversion of the first channel is placed in result register, AD1DAT0. The result of the conversion of the second channel is placed in result register, AD1DAT1. The first channel is again converted and its result stored in AD1DAT2. The second channel is again converted and its result placed in AD1DAT3. An interrupt is generated, if enabled, after every set of four conversions (two conversions per channel).

9.4.6 Single step mode

This special mode allows ‘single-stepping’ in an auto scan conversion mode. Any combination of the four input channels can be selected for conversion. After each channel is converted, an interrupt is generated, if enabled, and the A/D waits for the next start condition. May be used with any of the start modes.

9.5 Conversion start modes

9.5.1 Timer triggered start

An A/D conversion is started by the overflow of Timer 0. Once a conversion has started, additional Timer 0 triggers are ignored until the conversion has completed. The Timer triggered start mode is available in all A/D operating modes.

9.5.2 Start immediately

Programming this mode immediately starts a conversion. This start mode is available in all A/D operating modes.

9.6 Boundary limits interrupt

The A/D converter has both a high and low boundary limit register. After the four MSBs have been converted, these four bits are compared with the four MSBs of the boundary high and low registers. If the four MSBs of the conversion are outside the limit an interrupt will be generated, if enabled. If the conversion result is within the limits, the boundary limits will again be compared after all 8 bits have been converted. An interrupt will be generated, if enabled, if the result is outside the boundary limits. The boundary limit may be disabled by clearing the boundary limit interrupt enable.

9.7 DAC output to a port pin with high output impedance

The A/D converter’s DAC block can be output to a port pin. In this mode, the AD1DAT3 register is used to hold the value fed to the DAC. After a value has been written to the DAC (written to AD1DAT3), the DAC output will appear on the channel 3 pin.

9.8 Clock divider

The A/D converter requires that its internal clock source be in the range of 500 kHz to 3.3 MHz to maintain accuracy. A programmable clock divider that divides the clock from 1 to 8 is provided for this purpose.

10. Limiting values

Table 11. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions	Min	Max	Unit
$T_{amb(bias)}$	bias ambient temperature		–55	+125	°C
T_{stg}	storage temperature		–65	+150	°C
$I_{OH(I/O)}$	HIGH-level output current per input/output pin		-	8	mA
$I_{OL(I/O)}$	LOW-level output current per input/output pin		-	20	mA
$I_{I/Otot(max)}$	maximum total input/output current		-	120	mA
V_n	voltage on any other pin	except V_{SS}, with respect to V_{DD}	–0.5	+5.5	V
$P_{tot(pack)}$	total power dissipation per package	based on package heat transfer, not device power consumption	-	1.5	W

[1] The following applies to Table 11 “Limiting values”:

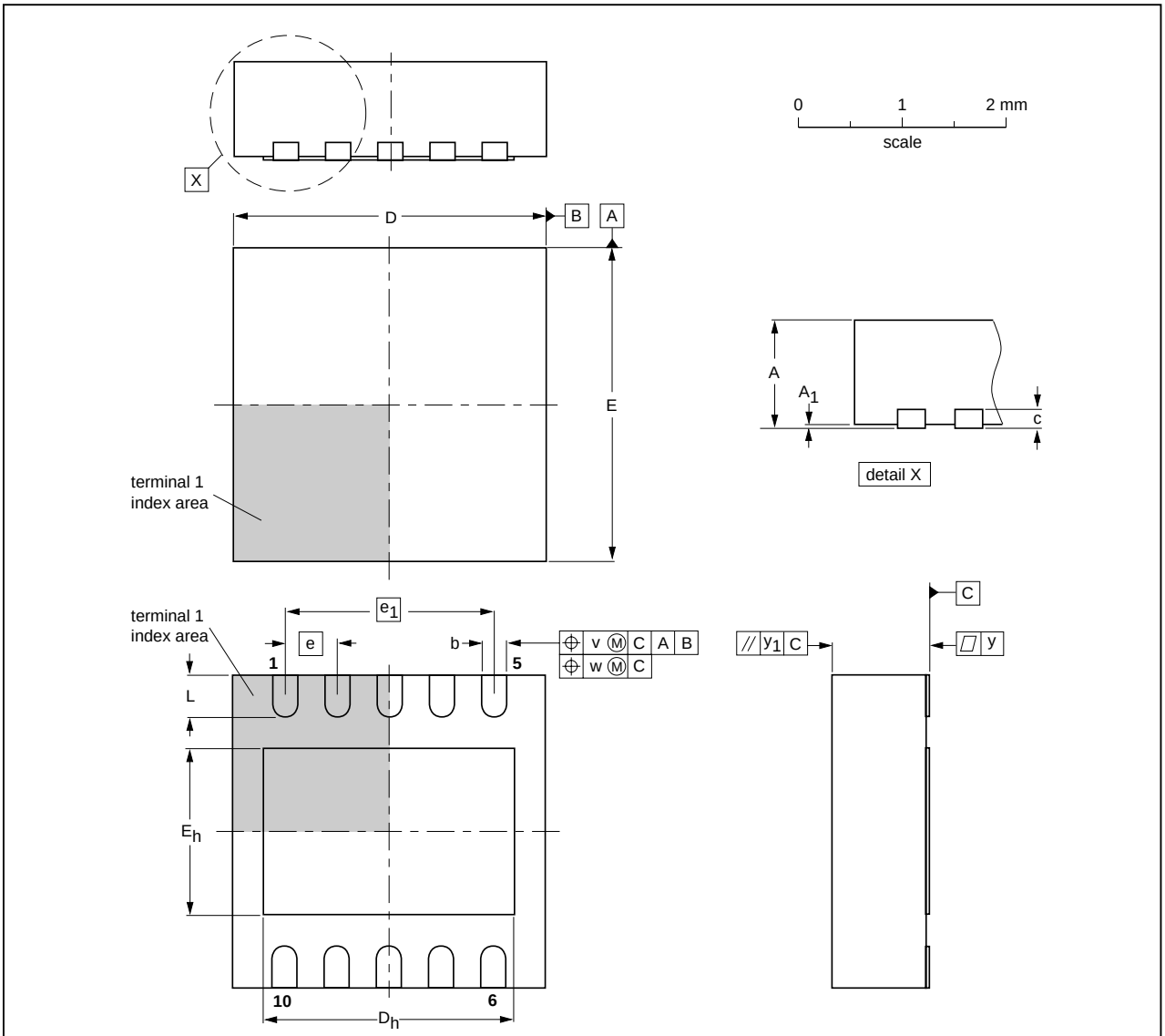
a) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in Table 12 “Static characteristics” and Table 13 “Dynamic characteristics (12 MHz)” section of this specification are not implied.

b) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

c) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

14. Package outline

HVSON10: plastic thermal enhanced very thin small outline package; no leads; 10 terminals; body 3 x 3 x 0.85 mm **SOT650-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.1 2.9	2.55 2.15	3.1 2.9	1.75 1.45	0.5	2	0.55 0.30	0.1	0.05	0.05	0.1

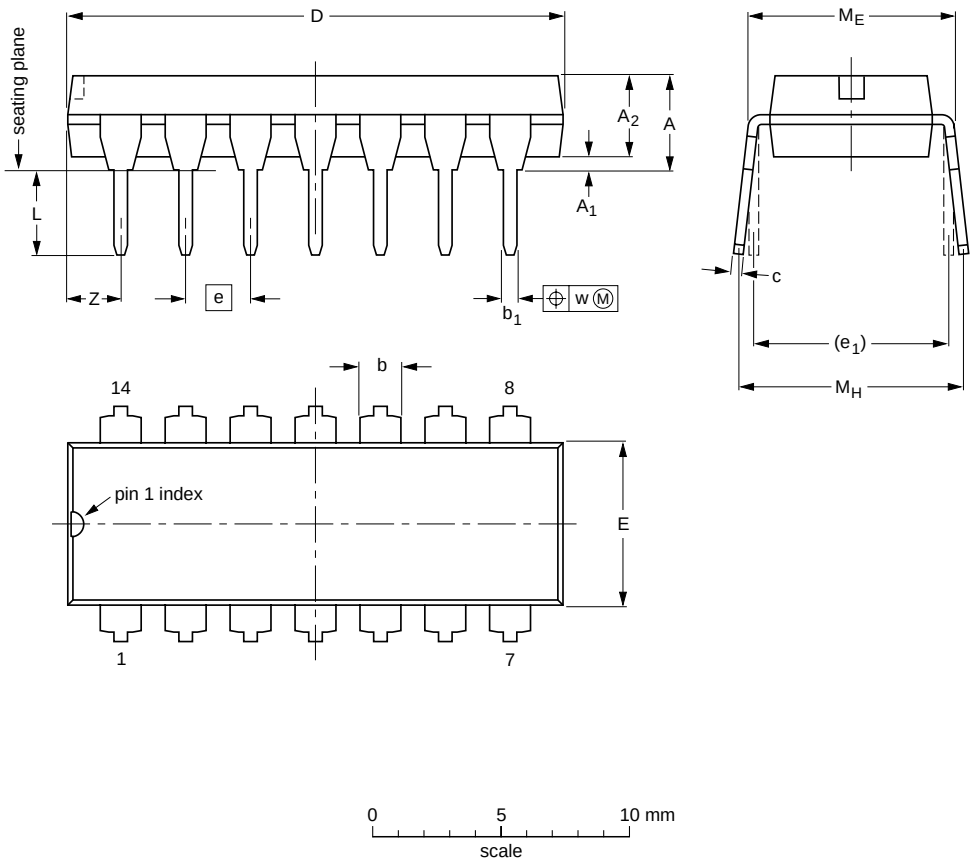
Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT650-1	- - -	MO-229	- - -			~~01-01-22~~ 02-02-08

Fig 21. Package outline SOT650-1 (HVSON10)

DIP14: plastic dual in-line package; 14 leads (300 mil) **SOT27-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.02	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT27-1	050G04	MO-001	SC-501-14			~~99-12-27~~ 03-02-13

Fig 23. Package outline SOT27-1 (DIP14)

16. Revision history

Table 18. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
P89LPC9102_9103_ 9107_3	20070710	Product data sheet	-	P89LPC9102_9103_9107_2
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Added new device P89LPC9107FN.			
P89LPC9102_9103_ 9107_2	20050411	Product data sheet	-	P89LPC9102_9103_9107_1
P89LPC9102_9103_ 9107_1	20050111	Product data sheet	-	-

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 10 July 2007
Document identifier: P89LPC9102_9103_9107_3