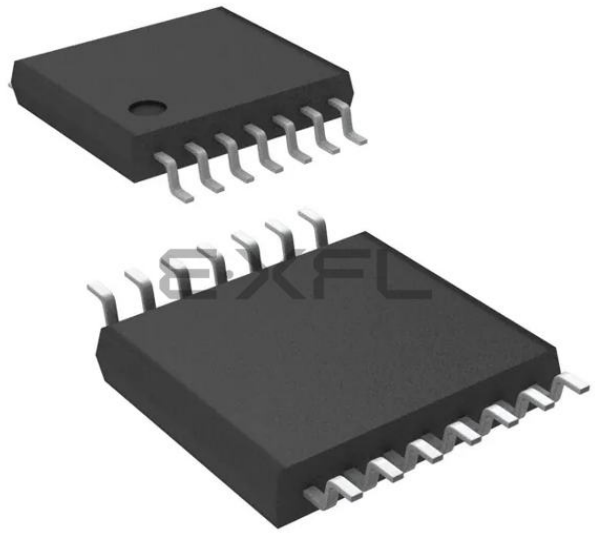

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	18MHz
Connectivity	UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	12
Program Memory Size	1KB (1K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	14-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	14-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p89lpc9107fdh-129

5. Block diagram

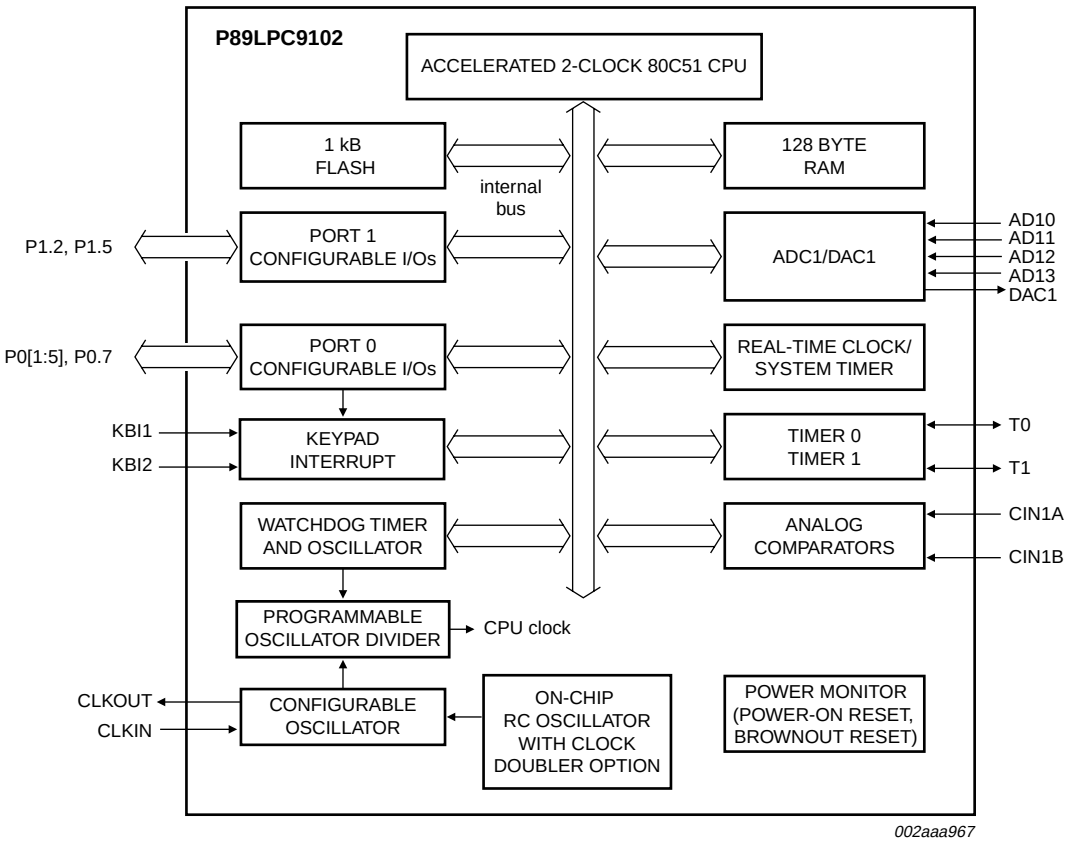

Fig 1. Block diagram of P89LPC9102

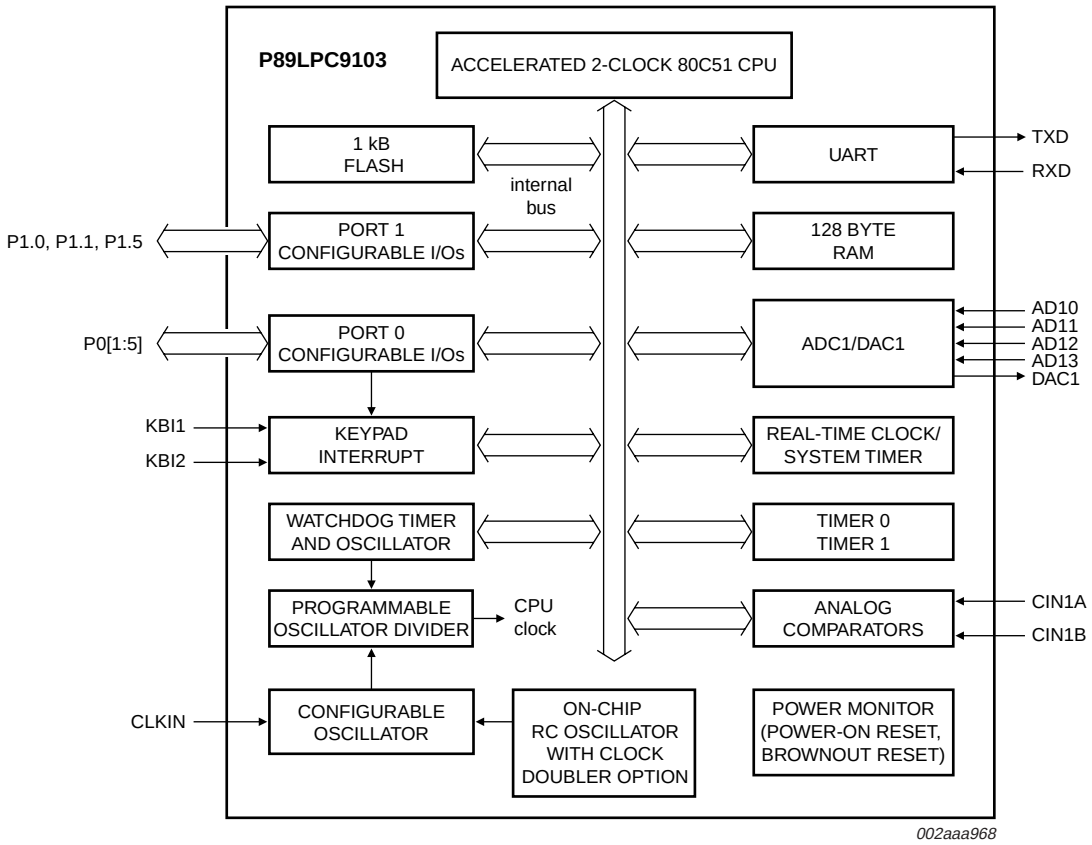

Fig 2. Block diagram of P89LPC9103

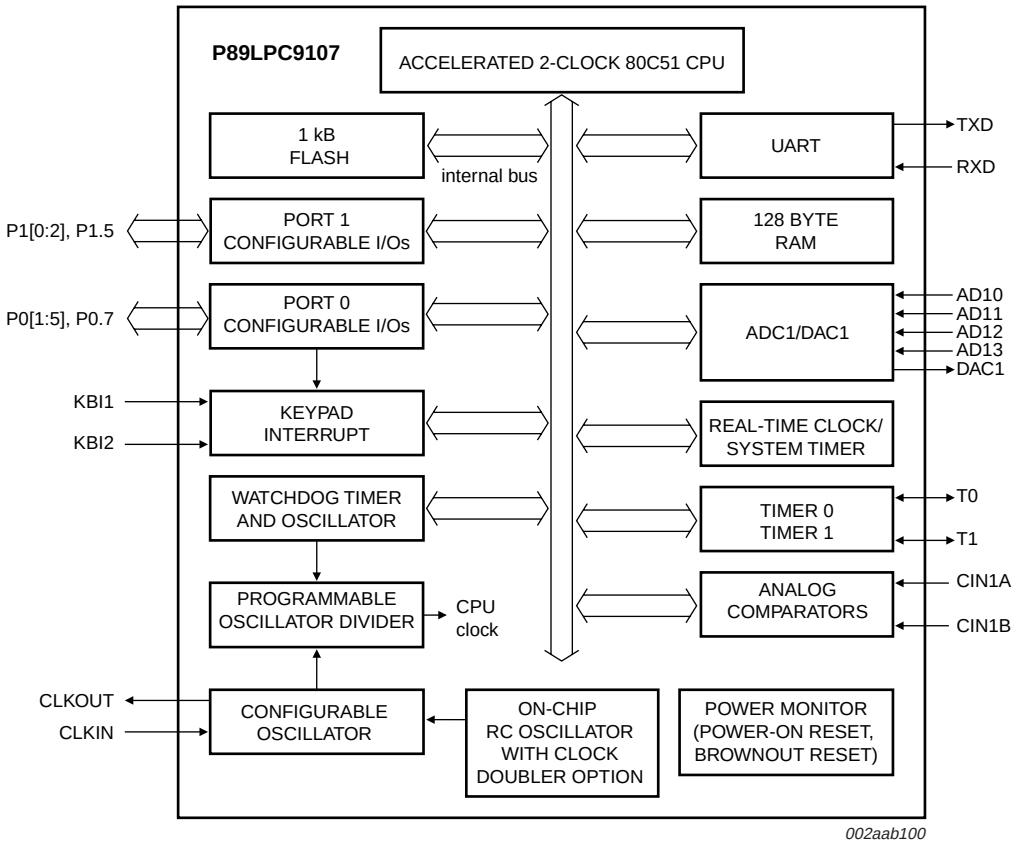

Fig 3. Block diagram of P89LPC9107

6. Functional diagram

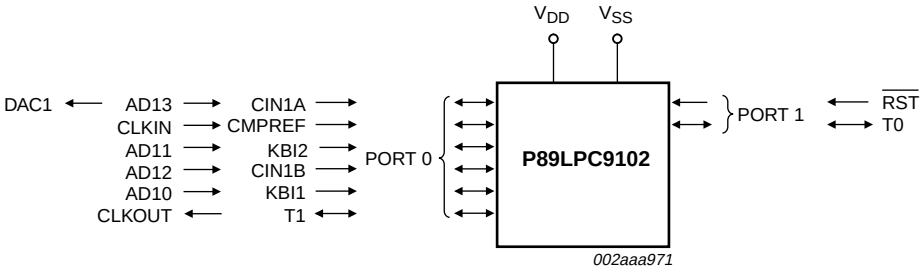

Fig 4. Functional diagram of P89LPC9102

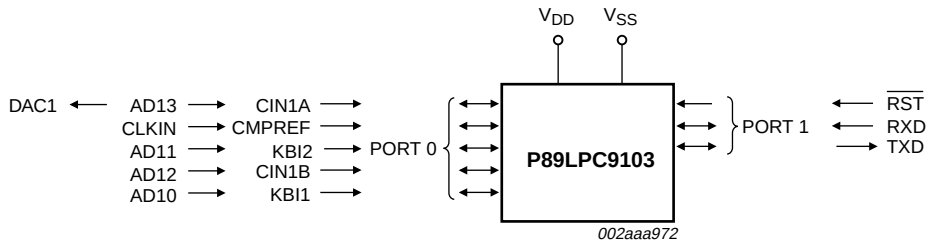

Fig 5. Functional diagram of P89LPC9103

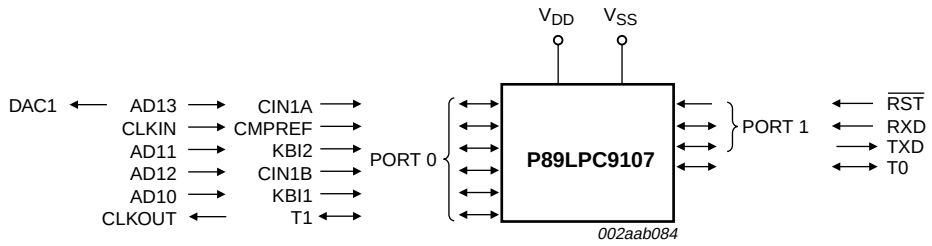

Fig 6. Functional diagram of P89LPC9107

7.2 Pin description

Table 4. P89LPC9102 pin description

Symbol	Pin	Type	Description
P0.1 to P0.5, P0.7		I/O	**Port 0:** Port 0 is an I/O port with a user-configurable output type. During reset Port 0 latches are configured in the input-only mode with the internal pull-up disabled. The operation of Port 0 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 8.12.1 “Port configurations” and Table 12 “Static characteristics” for details. The Keypad Interrupt feature operates with Port 0 pins. All pins have Schmitt triggered inputs. Port 0 also provides various special functions as described below:
P0.1/KBI1/ AD10	4	I/O	**P0.1 —** Port 0 bit 1.
		I	**KBI1 —** Keyboard input 1.
		I	**AD10 —** ADC1 channel 0 analog input.
P0.2/KBI2/ AD11	1	I/O	**P0.2 —** Port 0 bit 2.
		I	**KBI2 —** Keyboard input 2.
		I	**AD11 —** ADC1 channel 1 analog input.
P0.3/CIN1B/ AD12	10	I/O	**P0.3 —** Port 0 bit 3.
		I	**CIN1B —** Comparator 1 positive input.
		I	**AD12 —** ADC1 channel 2 analog input.
P0.4/CIN1A/ AD13/DAC1	9	I/O	**P0.4 —** Port 0 bit 4.
		I	**CIN1A —** Comparator 1 positive input.
		I	**AD13 —** ADC1 channel 3 analog input.
		O	**DAC1 —** Digital to analog converter output.
P0.5/CMPREF/CLKIN	8	I/O	**P0.5 —** Port 0 bit 5.
		I	**CMPREF —** Comparator reference (negative) input.
		I	**CLKIN —** External clock input.
P0.7/T1/ CLKOUT	6	I/O	**P0.7 —** Port 0 bit 7.
		I/O	**T1 —** Timer/counter 1 external count input or overflow/PWM output.
		I	**CLKOUT —** Clock output.
P1.2, P1.5		I/O	**Port 1:** Port 1 is an I/O port with a user-configurable output type. During reset Port 1 latches are configured in the input-only mode with the internal pull-up disabled. The operation of the configurable Port 1 pins as inputs and outputs depends upon the port configuration selected. Each of the configurable port pins are programmed independently. Refer to Section 8.12.1 “Port configurations” and Table 12 “Static characteristics” for details. P1.5 is input-only. All pins have Schmitt triggered inputs. Port 1 also provides various special functions as described below:
P1.2/T0	5	I/O	**P1.2 —** Port 1 bit 2.
		I/O	**T0 —** Timer/counter 0 external count input or overflow/PWM output.

Table 6. P89LPC9107 pin description *…continued*

Symbol	Pin	Type	Description
P1.0 to P1.2, P1.5		I/O	**Port 1:** Port 1 is an I/O port with a user-configurable output type. During reset Port 1 latches are configured in the input-only mode with the internal pull-up disabled. The operation of the configurable Port 1 pins as inputs and outputs depends upon the port configuration selected. Each of the configurable port pins are programmed independently. Refer to Section 8.12.1 "Port configurations" and Table 12 "Static characteristics" for details. P1.5 is input-only. All pins have Schmitt triggered inputs. Port 1 also provides various special functions as described below:
P1.0/TXD	6	I/O	**P1.0 —** Port 1 bit 0.
		O	**TXD —** Serial port transmitter data.
P1.1/RXD	9	I/O	**P1.1 —** Port 1 bit 1.
		I	**RXD —** Serial port receiver data.
P1.2/T0	7	I/O	**P1.2 —** Port 1 bit 2.
		I/O	**T0 —** Timer/counter 0 external count input or overflow/PWM output.
P1.5/$\overline{\text{RST}}$	3	I	**P1.5 —** Port 1 bit 5 (input-only).
		I	**$\overline{\text{RST}}$ —** External Reset input during Power-on or if selected via UCFG1. When functioning as a reset input a LOW on this pin resets the microcontroller, causing I/O ports and peripherals to take on their default states, and the processor begins execution at address 0. **When using an oscillator frequency above 12 MHz, the reset input function of P1.5 must be enabled. An external circuit is required to hold the device in reset at power-up until V_{DD} has reached its specified level. When system power is removed V_{DD} will fall below the minimum specified operating voltage. When using an oscillator frequency above 12 MHz, in some applications, an external brownout detect circuit may be required to hold the device in reset when V_{DD} falls below the minimum specified operating voltage.**
V_{SS}	4	I	**Ground:** 0 V reference.
V_{DD}	10	I	**Power supply:** This is the power supply voltage for normal operation as well as Idle mode and Power-down mode.

Table 7. P89LPC9102 special function registers *...continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
		Bit address	EF	EE	ED	EC	EB	EA	E9	E8		
IEN1*	Interrupt enable 1	E8H	EAD	-	-	-	-	EC	EKBI	-	00[1]	00x0 0000
		Bit address	BF	BE	BD	BC	BB	BA	B9	B8		
IP0*	Interrupt priority 0	B8H	-	PWDRT	PBO	-	PT1	-	PT0	-	00[1]	x000 0000
IP0H	Interrupt priority 0 high	B7H	-	PWDRTH	PBOH	-	PT1H	-	PT0H	-	00[1]	x000 0000
		Bit address	FF	FE	FD	FC	FB	FA	F9	F8		
IP1*	Interrupt priority 1	F8H	PAD	-	-	-	-	PC	PKBI	-	00[1]	00x0 0000
IP1H	Interrupt priority 1 high	F7H	PADH	-	-	-	-	PCH	PKBIH	-	00[1]	00x0 0000
KBCON	Keypad control register	94H	-	-	-	-	-	-	PATN_SEL	KBIF	00[1]	xxxx xx00
KBMASK	Keypad interrupt mask register	86H		-	-	-	KBMASK.2	KBMASK.1	-	-	00	xxxx x00x
KBPATN	Keypad pattern register	93H	-	-	-	-	KBPATN.2	KBPATN.1	-	-	FF	xxxx x11x
		Bit address	87	86	85	84	83	82	81	80		
P0*	Port 0	80H	CLKOUT/T1	-	CMPREF/CLKIN	CIN1A	CIN1B	CIN2A/KBI2	KBI1	-	[2]	
		Bit address	97	96	95	94	93	92	91	90		
P1*	Port 1	90H	-	-	$\overline{\text{RST}}$	-	-	T0	-	-		
P0M1	Port 0 output mode 1	84H	(P0M1.7)	-	(P0M1.5)	(P0M1.4)	(P0M1.3)	(P0M1.2)	(P0M1.1)	-	FF	1111 1111
P0M2	Port 0 output mode 2	85H	(P0M2.7)	-	(P0M2.5)	(P0M2.4)	(P0M2.3)	(P0M2.2)	(P0M2.1)	-	00	0000 0000
P1M1	Port 1 output mode 1	91H	-	-	-	-	-	(P1M1.2)	-	-	FF[1]	1111 1111
P1M2	Port 1 output mode 2	92H	-	-	-	-	-	(P1M2.2)	-	-	00[1]	0000 0000
PCON	Power control register	87H	-	-	BOPD	BOI	GF1	GF0	PMOD1	PMOD0	00	0000 0000
PCONA	Power control register A	B5H	RTCPD		VCPD	ADPD		-	-		00[1]	0000 0000
PCONB	reserved for Power control register B	B6H	-	-	-	-	-	-	-	-	00[1]	xxxx xxxx
		Bit address	D7	D6	D5	D4	D3	D2	D1	D0		
PSW*	Program status word	D0H	CY	AC	F0	RS1	RS0	OV	F1	P	00	0000 0000
PT0AD	Port 0 digital input disable	F6H	-	-	PT0AD.5	PT0AD.4	PT0AD.3	PT0AD.2	PT0AD.1	-	00	xx00 000x

Table 8. P89LPC9103 special function registers *...continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
FMDATA	Program flash data	E5H									00	0000 0000
IEN0*	Interrupt enable 0	A8H	EA	EWDRT	EBO	ES/ESR	ET1	-	ET0	-	00	0000 0000
	Bit address		EF	EE	ED	EC	EB	EA	E9	E8		
IEN1*	Interrupt enable 1	E8H	EAD	EST	-	-	-	EC	EKBI	-	00[1]	00x0 0000
	Bit address		BF	BE	BD	BC	BB	BA	B9	B8		
IP0*	Interrupt priority 0	B8H	-	PWDRT	PBO	PS/PSR	PT1	-	PT0	-	00[1]	x000 0000
IP0H	Interrupt priority 0 high	B7H	-	PWDRTH	PBOH	PSH/PSRH	PT1H	-	PT0H	-	00[1]	x000 0000
	Bit address		FF	FE	FD	FC	FB	FA	F9	F8		
IP1*	Interrupt priority 1	F8H	PAD	PST	-	-	-	PC	PKBI	-	00[1]	00x0 0000
IP1H	Interrupt priority 1 high	F7H	PADH	PSTH	-	-	-	PCH	PKBIH	-	00[1]	00x0 0000
KBCON	Keypad control register	94H	-	-	-	-	-	-	PATN_SEL	KBIF	00[1]	xxxx xx00
KBMASK	Keypad interrupt mask register	86H		-	-	-	-	KBMASK.2	KBMASK.1	-	00	xxxx x00x
KBPATN	Keypad pattern register	93H	-	-	-	-	-	KBPATN.2	KBPATN.1	-	FF	xxxx x11x
	Bit address		87	86	85	84	83	82	81	80		
P0*	Port 0	80H	-	-	CMPREF/CLKIN	CIN1A	CIN1B	KBI2	KBI1	-	[3]	
	Bit address		97	96	95	94	93	92	91	90		
P1*	Port 1	90H	-	-	$\overline{\text{RST}}$	-	-	-	RXD	TXD		
P0M1	Port 0 output mode 1	84H	-	-	(P0M1.5)	(P0M1.4)	(P0M1.3)	(P0M1.2)	(P0M1.1)	-	FF	1111 1111
P0M2	Port 0 output mode 2	85H	-	-	(P0M2.5)	(P0M2.4)	(P0M2.3)	(P0M2.2)	(P0M2.1)	-	00	0000 0000
P1M1	Port 1 output mode 1	91H	-	-	-	-	-	-	(P1M1.1)	(P1M1.0)	FF[1]	1111 1111
P1M2	Port 1 output mode 2	92H	-	-	-	-	-	-	(P1M2.1)	(P1M2.0)	00[1]	0000 0000
PCON	Power control register	87H	SMOD1	SMOD0	BOPD	BOI	GF1	GF0	PMOD1	PMOD0	00	0000 0000
PCONA	Power control register A	B5H	RTCPD		VCPD	ADPD		-	SPD		00[1]	0000 0000
PCONB	reserved for Power control register B	B6H	-	-	-	-	-	-	-	-	00[1]	xxxx xxxx

Table 8. P89LPC9103 special function registers *…continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
	Bit address		D7	D6	D5	D4	D3	D2	D1	D0		
PSW*	Program status word	D0H	CY	AC	F0	RS1	RS0	OV	F1	P	00	0000 0000
PT0AD	Port 0 digital input disable	F6H	-	-	PT0AD.5	PT0AD.4	PT0AD.3	PT0AD.2	PT0AD.1	-	00	xx00 000x
RSTSRC	Reset source register	DFH	-	-	BOF	POF	R_BK	R_WD	R_SF	R_EX	[4]	
RTCCON	Real-time clock control	D1H	RTCF	RTCS1	RTCS0	-	-	-	ERTC	RTCEN	60[5]	011x xx00
RTCH	Real-time clock register high	D2H									00[5]	0000 0000
RTCL	Real-time clock register low	D3H									00[5]	0000 0000
SADDR	Serial port address register	A9H									00	0000 0000
SADEN	Serial port address enable	B9H									00	0000 0000
SBUF	Serial port data buffer register	99H									xx	xxxx xxxx
	Bit address		9F	9E	9D	9C	9B	9A	99	98		
SCON*	Serial port control	98H	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI	00	0000 0000
SSTAT	Serial port extended status register	BAH	DBMOD	INTLO	CIDIS	DBISEL	FE	BR	OE	STINT	00	0000 0000
SP	Stack pointer	81H									07	0000 0111
	Bit address		8F	8E	8D	8C	8B	8A	89	88		
TCON*	Timer 0 and 1 control	88H	TF1	TR1	TF0	TR0	-	-	-	-	00	0000 0000
TH0	Timer 0 high	8CH									00	0000 0000
TH1	Timer 1 high	8DH									00	0000 0000
TL0	Timer 0 low	8AH									00	0000 0000
TL1	Timer 1 low	8BH									00	0000 0000
TMOD	Timer 0 and 1 mode	89H	-	-	T1M1	T1M0	-	-	T0M1	T0M0	00	0000 0000
TRIM	Internal oscillator trim register	96H	RCCLK	-	TRIM.5	TRIM.4	TRIM.3	TRIM.2	TRIM.1	TRIM.0	[5][6]	
WDCON	Watchdog control register	A7H	PRE2	PRE1	PRE0	-	-	WDRUN	WDTOF	WDCLK	[5][7]	
WDL	Watchdog load	C1H									FF	1111 1111
WFEED1	Watchdog feed 1	C2H										
WFEED2	Watchdog feed 2	C3H										

[1] Unimplemented bits in SFRs (labeled '-') are X (unknown) at all times. Unless otherwise specified, ones should not be written to these bits since they may be used for other purposes in future derivatives. The reset values shown for these bits are logic 0s although they are unknown when read.

[2] BRGR1 and BRGR0 must only be written if BRGEN in BRGCON SFR is logic 0. If any are written while BRGEN = 1, the result is unpredictable.

Table 9. P89LPC9107 special function registers

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
	Bit address		E7	E6	E5	E4	E3	E2	E1	E0		
ACC*	Accumulator	E0H									00	0000 0000
ADCON1	A/D control register 1	97H	ENBI1	ENADCI 1	TMM1	-	ADCI1	ENADC1	ADCS11	ADCS10	00	0000 0000
ADINS	A/D input select	A3H	AD13	AD12	AD11	AD10	-	-	-	-	00	0000 0000
ADMODA	A/D mode register A	C0H	BNDI1	BURST1	SCC1	SCAN1	-	-	-	-	00	0000 0000
ADMODB	A/D mode register B	A1H	CLK2	CLK1	CLK0	-	ENDAC1	-	BSA1	-	00	000x 0000
AD1BH	A/D_1 boundary high register	C4H									FF	1111 1111
AD1BL	A/D_1 boundary low register	BCH									00	0000 0000
AD1DAT0	A/D_1 data register 0	D5H									00	0000 0000
AD1DAT1	A/D_1 data register 1	D6H									00	0000 0000
AD1DAT2	A/D_1 data register 2	D7H									00	0000 0000
AD1DAT3	A/D_1 data register 3	F5H									00	0000 0000
AUXR1	Auxiliary function register	A2H	CLKLP	EBRR	ENT1	ENT0	SRST	0	-	DPS	00[1]	0000 00x0
	Bit address		F7	F6	F5	F4	F3	F2	F1	F0		
B*	B register	F0H									00	0000 0000
BRGR0[2]	Baud rate generator rate low	BEH									00	0000 0000
BRGR1[2]	Baud rate generator rate high	BFH									00	0000 0000
BRGCON	Baud rate generator control	BDH	-	-	-	-	-	-	SBRGS	BRGEN	00[2]	xxxx xx00
CMP1	Comparator 1 control register	ACH	-	-	CE1	CP1	CN1	-	CO1	CMF1	00[1]	xx00 0000
DIVM	CPU clock divide-by-M control	95H									00	0000 0000
DPTR	Data pointer (2 bytes)											
DPH	Data pointer high	83H									00	0000 0000
DPL	Data pointer low	82H									00	0000 0000
FMADRH	Program flash address high	E7H									00	0000 0000
FMADRL	Program flash address low	E6H									00	0000 0000
FMCON	Program flash Control (Read)	E4H	BUSY	-	-	-	HVA	HVE	SV	OI	70	0111 0000
	Program flash Control (Write)		FMCMD. 7	FMCMD. 6	FMCMD. 5	FMCMD. 4	FMCMD. 3	FMCMD. 2	FMCMD. 1	FMCMD. 0		

Table 9. P89LPC9107 special function registers *...continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
FMDATA	Program flash data	E5H									00	0000 0000
IEN0*	Interrupt enable 0	A8H	EA	EWDRT	EBO	ES/ESR	ET1	-	ET0	-	00	0000 0000
	Bit address		EF	EE	ED	EC	EB	EA	E9	E8		
IEN1*	Interrupt enable 1	E8H	EAD	EST	-	-	-	EC	EKBI	-	00[1]	00x0 0000
	Bit address		BF	BE	BD	BC	BB	BA	B9	B8		
IP0*	Interrupt priority 0	B8H	-	PWDRT	PBO	PS/PSR	PT1	-	PT0	-	00[1]	x000 0000
IP0H	Interrupt priority 0 high	B7H	-	PWDRTH	PBOH	PSH/PSRH	PT1H	-	PT0H	-	00[1]	x000 0000
	Bit address		FF	FE	FD	FC	FB	FA	F9	F8		
IP1*	Interrupt priority 1	F8H	PAD	PST	-	-	-	PC	PKBI	-	00[1]	00x0 0000
IP1H	Interrupt priority 1 high	F7H	PADH	PSTH	-	-	-	PCH	PKBIH	-	00[1]	00x0 0000
KBCON	Keypad control register	94H	-	-	-	-	-	-	PATN_SEL	KBIF	00[1]	xxxx xx00
KBMASK	Keypad interrupt mask register	86H		-	-	-	-	KBMASK.2	KBMASK.1	-	00	xxxx x00x
KBPATN	Keypad pattern register	93H	-	-	-	-	-	KBPATN.2	KBPATN.1	-	FF	xxxx x11x
	Bit address		87	86	85	84	83	82	81	80		
P0*	Port 0	80H	-	-	CMPREF/CLKIN	CIN1A	CIN1B	KBI2	KBI1	-	[3]	
	Bit address		97	96	95	94	93	92	91	90		
P1*	Port 1	90H	-	-	$\overline{\text{RST}}$	-	-	-	RXD	TXD		
P0M1	Port 0 output mode 1	84H	-	-	(P0M1.5)	(P0M1.4)	(P0M1.3)	(P0M1.2)	(P0M1.1)	-	FF	1111 1111
P0M2	Port 0 output mode 2	85H	-	-	(P0M2.5)	(P0M2.4)	(P0M2.3)	(P0M2.2)	(P0M2.1)	-	00	0000 0000
P1M1	Port 1 output mode 1	91H	-	-	-	-	-	-	(P1M1.1)	(P1M1.0)	FF[1]	1111 1111
P1M2	Port 1 output mode 2	92H	-	-	-	-	-	-	(P1M2.1)	(P1M2.0)	00[1]	0000 0000
PCON	Power control register	87H	SMOD1	SMOD0	BOPD	BOI	GF1	GF0	PMOD1	PMOD0	00	0000 0000
PCONA	Power control register A	B5H	RTCPD		VCPD	ADPD		-	SPD		00[1]	0000 0000
PCONB	reserved for Power control register B	B6H	-	-	-	-	-	-	-	-	00[1]	xxxx xxxx

Table 9. P89LPC9107 special function registers *…continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
	Bit address		D7	D6	D5	D4	D3	D2	D1	D0		
PSW*	Program status word	D0H	CY	AC	F0	RS1	RS0	OV	F1	P	00	0000 0000
PT0AD	Port 0 digital input disable	F6H	-	-	PT0AD.5	PT0AD.4	PT0AD.3	PT0AD.2	PT0AD.1	-	00	xx00 000x
RSTSRC	Reset source register	DFH	-	-	BOF	POF	R_BK	R_WD	R_SF	R_EX	[4]	
RTCCON	Real-time clock control	D1H	RTCF	RTCS1	RTCS0	-	-	-	ERTC	RTCEN	60[5]	011x xx00
RTCH	Real-time clock register high	D2H									00[5]	0000 0000
RTCL	Real-time clock register low	D3H									00[5]	0000 0000
SADDR	Serial port address register	A9H									00	0000 0000
SADEN	Serial port address enable	B9H									00	0000 0000
SBUF	Serial port data buffer register	99H									xx	xxxx xxxx
	Bit address		9F	9E	9D	9C	9B	9A	99	98		
SCON*	Serial port control	98H	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI	00	0000 0000
SSTAT	Serial port extended status register	BAH	DBMOD	INTLO	CIDIS	DBISEL	FE	BR	OE	STINT	00	0000 0000
SP	Stack pointer	81H									07	0000 0111

Table 9. P89LPC9107 special function registers *…continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
	Bit address		8F	8E	8D	8C	8B	8A	89	88		
TCON*	Timer 0 and 1 control	88H	TF1	TR1	TF0	TR0	-	-	-	-	00	0000 0000
TH0	Timer 0 high	8CH									00	0000 0000
TH1	Timer 1 high	8DH									00	0000 0000
TL0	Timer 0 low	8AH									00	0000 0000
TL1	Timer 1 low	8BH									00	0000 0000
TMOD	Timer 0 and 1 mode	89H	-	-	T1M1	T1M0	-	-	T0M1	T0M0	00	0000 0000
TRIM	Internal oscillator trim register	96H	RCCLK	ENCLK	TRIM.5	TRIM.4	TRIM.3	TRIM.2	TRIM.1	TRIM.0	[5][6]	
WDCON	Watchdog control register	A7H	PRE2	PRE1	PRE0	-	-	WDRUN	WDTOF	WDCLK	[5][7]	
WDL	Watchdog load	C1H									FF	1111 1111
WFEED1	Watchdog feed 1	C2H										
WFEED2	Watchdog feed 2	C3H										

[1] Unimplemented bits in SFRs (labeled '-') are X (unknown) at all times. Unless otherwise specified, ones should not be written to these bits since they may be used for other purposes in future derivatives. The reset values shown for these bits are logic 0s although they are unknown when read.

[2] BRGR1 and BRGR0 must only be written if BRGEN in BRGCON SFR is logic 0. If any are written while BRGEN = 1, the result is unpredictable.

[3] All ports are in input-only (high-impedance) state after power-up.

[4] The RSTSRC register reflects the cause of the P89LPC9102/9103/9107 reset. Upon a power-up reset, all reset source flags are cleared except POF and BOF; the power-on reset value is xx11 0000.

[5] The only reset source that affects these SFRs is power-on reset.

[6] On power-on reset, the TRIM SFR is initialized with a factory preprogrammed value. Other resets will not cause initialization of the TRIM register.

[7] After reset, the value is 1110 01x1, i.e., PRE2 to PRE0 are all logic 1s, WDRUN = 1 and WDCLK = 1. WDTOF bit is logic 1 after watchdog timer reset and is logic 0 after power-on reset. Other resets will not affect WDTOF.

8.21 Comparator interrupt

The comparator has an interrupt flag contained in its configuration register. This flag is set whenever the comparator output changes state. The flag may be polled by software or may be used to generate an interrupt.

8.22 Comparator and power reduction modes

The comparator may remain enabled when Power-down mode or Idle mode is activated, but the comparator is disabled automatically in Total Power-down mode.

If the comparator interrupt is enabled (except in Total Power-down mode), a change of the comparator output state will generate an interrupt and wake-up the processor. If the comparator output to a pin is enabled, the pin should be configured in the push-pull mode in order to obtain fast switching times while in Power-down mode. The reason is that with the oscillator stopped, the temporary strong pull-up that normally occurs during switching on a quasi-bidirectional port pin does not take place.

The comparator consumes power in Power-down mode and Idle mode, as well as in the normal operating mode. This fact should be taken into account when system power consumption is an issue. To minimize power consumption, the user can disable the comparator via PCONA.5 or put the device in Total Power-down mode.

8.23 Keypad interrupt (KBI)

The Keypad Interrupt function is intended primarily to allow a single interrupt to be generated when Port 0 is equal to or not equal to a certain pattern. This function can be used for bus address recognition or keypad recognition. The user can configure the port via SFRs for different tasks.

The Keypad Interrupt Mask Register (KBMASK) is used to define which input pins connected to Port 0 can trigger the interrupt. The Keypad Pattern Register (KBPATN) is used to define a pattern that is compared to the value of Port 0. The Keypad Interrupt Flag (KBIF) in the Keypad Interrupt Control Register (KBCON) is set when the condition is matched while the Keypad Interrupt function is active. An interrupt will be generated if enabled. The PATN_SEL bit in the Keypad Interrupt Control Register (KBCON) is used to define equal or not-equal for the comparison.

In order to use the Keypad Interrupt as an original KBI function like in 87LPC76x series, the user needs to set KBPATN = 0FFH and PATN_SEL = 1 (not equal), then any key connected to Port 0 which is enabled by the KBMASK register will cause the hardware to set KBIF and generate an interrupt if it has been enabled. The interrupt may be used to wake-up the CPU from Idle mode or Power-down mode. This feature is particularly useful in handheld, battery powered systems that need to carefully manage power consumption yet also need to be convenient to use.

In order to set the flag and cause an interrupt, the pattern on Port 0 must be held longer than six CCLKs.

8.24 Watchdog timer

The watchdog timer causes a system reset when it underflows as a result of a failure to feed the timer prior to the timer reaching its terminal count. It consists of a programmable 12-bit prescaler, and an 8-bit down counter. The down counter is decremented by a tap

8.26 Flash program memory

8.26.1 General description

The P89LPC9102/9103/9107 flash memory provides in-circuit electrical erasure and programming. The flash can be erased, read, and written as bytes. The Sector and Page Erase functions can erase any flash sector (256 bytes) or page (16 bytes). The Chip Erase operation will erase the entire program memory. In-Circuit Programming using standard commercial programmers is available. In addition, In-Application Programming Lite (IAP-Lite) and byte erase allows code memory to be used for non-volatile data storage. On-chip erase and write timing generation contribute to a user-friendly programming interface. The P89LPC9102/9103/9107 flash reliably stores memory contents even after more than 400000 erase and program cycles. The cell is designed to optimize the erase and programming mechanisms. The P89LPC9102/9103/9107 uses V_{DD} as the supply voltage to perform the Program/Erase algorithms.

8.26.2 Features

- Programming and erase over the full operating voltage range.
- Byte-erase allowing code memory to be used for data storage.
- Read/Programming/Erase using ICP.
- Any flash program/erase operation in 2 ms.
- Programming with industry-standard commercial programmers.
- Programmable security for the code in the flash for each sector.
- More than 400000 minimum erase/program cycles for each byte.
- 20-year minimum data retention.

8.26.3 Flash organization

The P89LPC9102/9103/9107 program memory consists of four 256 byte sectors. Each sector can be further divided into 16-byte pages. In addition to sector erase, page erase, and byte erase, a 16-byte page register is included which allows from 1 byte to 16 bytes of a given page to be programmed at the same time, substantially reducing overall programming time. In addition, erasing and reprogramming of user-programmable configuration bytes including UCFG1, the Boot Status Bit, and the Boot Vector is supported.

8.26.4 Flash programming and erasing

Different methods of erasing or programming of the flash are available. The flash may be programmed or erased in the end-user application (IAP-Lite) under control of the application's firmware. Another option is to use the ICP mechanism. This ICP system provides for programming through a serial clock- serial data interface. Third, the flash may be programmed or erased using a commercially available EPROM programmer which supports this device. This device does not provide for direct verification of code memory contents. Instead this device provides a 32-bit CRC result on either a sector or the entire 1 kB of user code space.

9.3 Block diagram

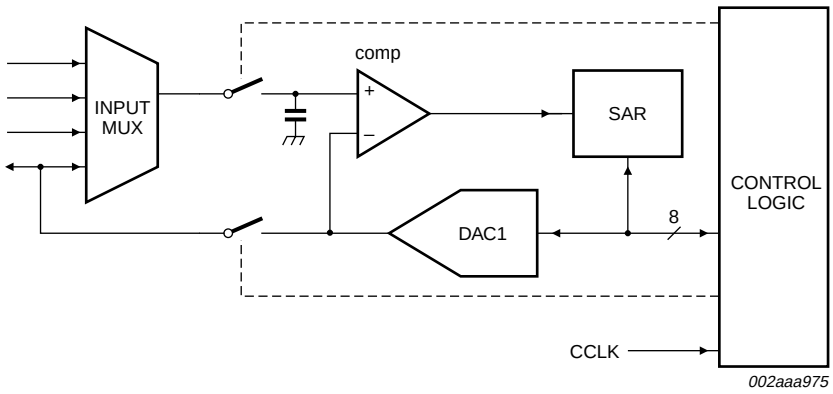

Fig 18. ADC block diagram

9.4 A/D operating modes

9.4.1 Fixed channel, single conversion mode

A single input channel can be selected for conversion. A single conversion will be performed and the result placed in the result register which corresponds to the selected input channel. An interrupt, if enabled, will be generated after the conversion completes.

9.4.2 Fixed channel, continuous conversion mode

A single input channel can be selected for continuous conversion. The results of the conversions will be sequentially placed in the four result registers. An interrupt, if enabled, will be generated after every four conversions. Additional conversion results will again cycle through the four result registers, overwriting the previous results. Continuous conversions continue until terminated by the user.

9.4.3 Auto scan, single conversion mode

Any combination of the four input channels can be selected for conversion. A single conversion of each selected input will be performed and the result placed in the result register which corresponds to the selected input channel. An interrupt, if enabled, will be generated after all selected channels have been converted. If only a single channel is selected this is equivalent to single channel, single conversion mode.

9.4.4 Auto scan, continuous conversion mode

Any combination of the four input channels can be selected for conversion. A conversion of each selected input will be performed and the result placed in the result register which corresponds to the selected input channel. An interrupt, if enabled, will be generated after all selected channels have been converted. The process will repeat starting with the first selected channel. Additional conversion results will again cycle through the four result registers, overwriting the previous results. Continuous conversions continue until terminated by the user.

10. Limiting values

Table 11. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions	Min	Max	Unit
$T_{amb(bias)}$	bias ambient temperature		–55	+125	°C
T_{stg}	storage temperature		–65	+150	°C
$I_{OH(I/O)}$	HIGH-level output current per input/output pin		-	8	mA
$I_{OL(I/O)}$	LOW-level output current per input/output pin		-	20	mA
$I_{I/Otot(max)}$	maximum total input/output current		-	120	mA
V_n	voltage on any other pin	except V_{SS}, with respect to V_{DD}	–0.5	+5.5	V
$P_{tot(pack)}$	total power dissipation per package	based on package heat transfer, not device power consumption	-	1.5	W

[1] The following applies to Table 11 “Limiting values”:

a) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in Table 12 “Static characteristics” and Table 13 “Dynamic characteristics (12 MHz)” section of this specification are not implied.

b) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

c) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

Table 14. Dynamic characteristics (18 MHz)

V_{DD} = 3.0 V to 3.6 V unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.[1]

Symbol	Parameter	Conditions	Variable clock		f_{ext} = 18 MHz		Unit
			Min	Max	Min	Max	
$f_{osc(RC)}$	internal RC oscillator frequency	clock doubler option = OFF (default); nominal f = 7.3728 MHz; trimmed to ±1 % at T_{amb} = 25 °C	7.189	7.557	7.189	7.557	MHz
		clock doubler option = ON; nominal f = 14.7456 MHz	14.378	15.114	14.378	15.114	MHz
$f_{osc(WD)}$	internal watchdog oscillator frequency	nominal f = 400 kHz	320	520	320	520	kHz
$T_{cy(clk)}$	clock cycle time	see Figure 20	83	-	-	-	ns
f_{CLKLP}	low-power select clock frequency		0	8	-	-	MHz
External clock							
f_{ext}	external clock frequency		-	-	0	18	MHz
t_{CHCX}	clock HIGH time	see Figure 20	22	$T_{cy(clk)} - t_{CLCX}$	22	-	ns
t_{CLCX}	clock LOW time		22	$T_{cy(clk)} - t_{CHCX}$	22	-	ns
t_{CLCH}	clock rise time		-	5	-	5	ns
t_{CHCL}	clock fall time		-	5	-	5	ns
Glitch filter							
t_{gr}	glitch rejection	P1.5/$\overline{RST}$ pin	-	50	-	50	ns
		any pin except P1.5/$\overline{RST}$	-	15	-	15	ns
t_{sa}	signal acceptance	P1.5/$\overline{RST}$ pin	125	-	125	-	ns
		any pin except P1.5/$\overline{RST}$	50	-	50	-	ns
Shift register (UART mode 0 - P89LPC9103)							
T_{XLXL}	serial port clock cycle time	see Figure 19	$16T_{cy(clk)}$	-	888	-	ns
t_{QVXH}	output data set-up to clock rising edge	see Figure 19	$13T_{cy(clk)}$	-	722	-	ns
t_{XHQX}	output data hold after clock rising edge	see Figure 19	-	$T_{cy(clk)}$ + 20	-	75	ns
t_{XHDX}	input data hold after clock rising edge	see Figure 19	-	0	-	0	ns
t_{XHDV}	input data valid to clock rising edge	see Figure 19	150	-	150	-	ns

[1] Parameters are valid over operating temperature range unless otherwise specified. Parts are tested to 2 MHz, but are guaranteed to operate down to 0 Hz.

12.1 Waveforms

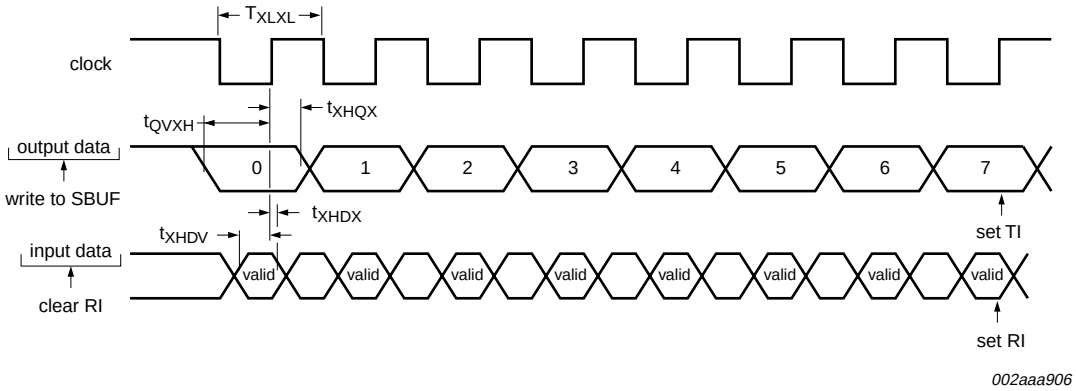

Fig 19. Shift register mode timing (P89LPC9103/9107)

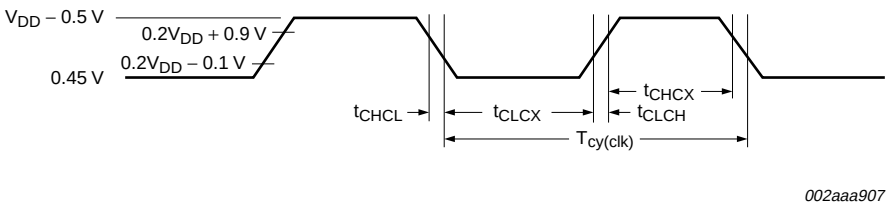

Fig 20. External clock timing

17. Legal information

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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