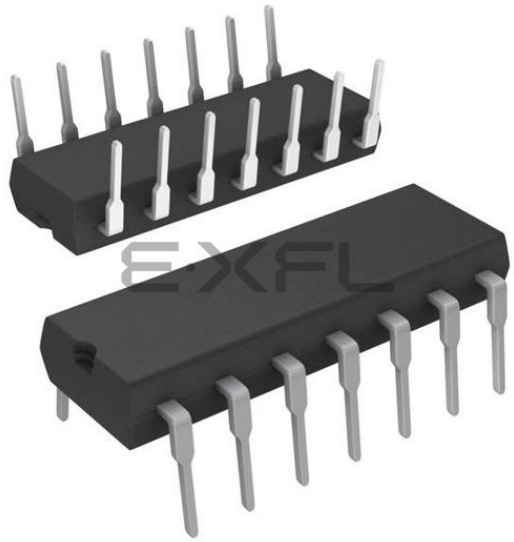

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	18MHz
Connectivity	UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	12
Program Memory Size	1KB (1K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	14-DIP (0.300", 7.62mm)
Supplier Device Package	14-DIP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p89lpc9107fn-112

- In-Application Programming (IAP-Lite) and byte erase allows code memory to be used for non-volatile data storage.
- Serial ßash ICP allows simple production coding with commercial EPROM programmers. Flash security bits prevent reading of sensitive application programs.
- Watchdog timer with separate on-chip oscillator, requiring no external components. The watchdog prescaler is selectable from eight values.
- Low voltage reset (Brownout detect) allows a graceful system shutdown when power fails. May optionally be conÞgured as an interrupt.
- Idle mode and two different reduced power Power-down modes. Improved wake-up from Power-down mode (a LOW interrupt input starts execution). Typical Power-down mode current is less than 1 mA (total Power-down mode with voltage comparators disabled).
- Active-LOW reset. On-chip power-on reset allows operation without external reset components. A reset counter and reset glitch suppression circuitry prevent spurious and incomplete resets. A software reset function is also available.
- Programmable port output conÞguration options: quasi-bidirectional, open drain, push-pull, input-only.
- Port Ôinput pattern matchÕ detect. Port 0 may generate an interrupt when the value of the pins match or do not match a programmable pattern.
- LED drive capability (20 mA) on all port pins. A maximum limit is speciÞed for the entire chip.
- Controlled slew rate port outputs to reduce EMI. Outputs have approximately 10 ns minimum ramp times.
- Only power and ground connections are required to operate the P89LPC9102/9103/9107 when internal reset option is selected.
- Four interrupt priority levels.
- Two keypad interrupt inputs.
- Second data pointer.
- External clock input.
- Clock output (P89LPC9102/9107).
- Schmitt trigger port inputs.
- Emulation support.

3. Product comparison overview

Table 1 highlights the differences between these two devices. For a complete list of device features, please see Section 2 ÒFeaturesÓ

Table 1. Product comparison overview

Type number	UART	T0 toggle/PWM	T1 toggle/PWM	CLKOUT
P89LPC9102	-	X	X	X
P89LPC9103	X	-	-	-
P89LPC9107	X	X	X	X

4. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
P89LPC9102FTK	HVSON10	plastic thermal enhanced very thin small outline package; no leads; 10 terminals; body 3 · 3 · 0.85 mm	SOT650-1
P89LPC9103FTK			
P89LPC9107FDH	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
P89LPC9107FN	DIP14	plastic dual in-line package; 14 leads (300 mil)	SOT27-1

4.1 Ordering options

Table 3. Ordering options

Type number	Temperature range	Frequency
P89LPC9102FTK	- 40 °C to +85 °C	internal RC or watchdog timer
P89LPC9103FTK		
P89LPC9107FDH		
P89LPC9107FN		

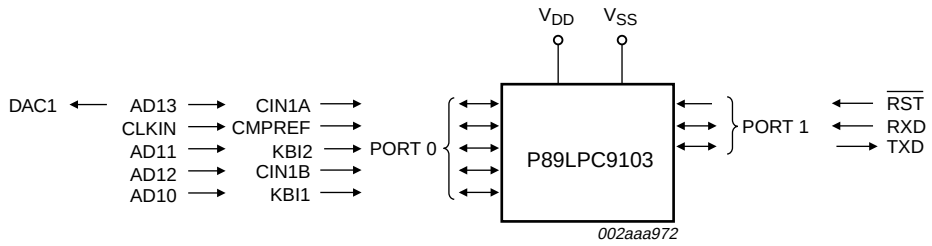

Fig 5. Functional diagram of P89LPC9103

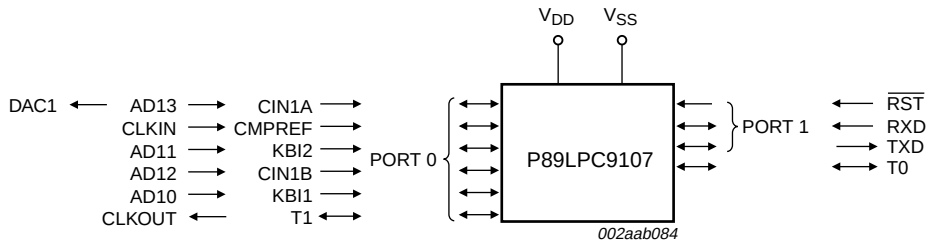

Fig 6. Functional diagram of P89LPC9107

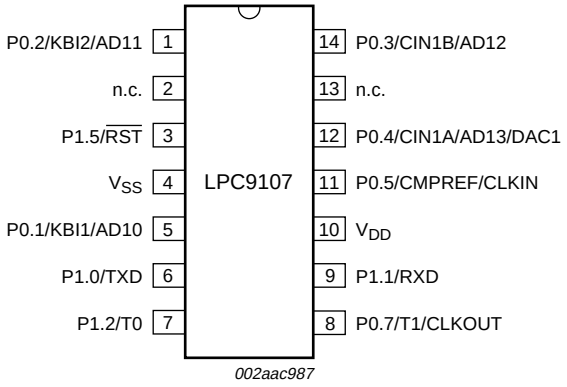

Fig 10. P89LPC9107 pinning (DIP14)

8. Functional description

Remark: Please refer to the *P89LPC9102/9103/9107 User manual UM10112* for a more detailed functional description.

8.1 Special function registers

Remark: Special Function Registers (SFRs) accesses are restricted in the following ways:

- User must not attempt to access any SFR locations not defined.
- Accesses to any defined SFR locations must be strictly for the functions for the SFRs.
- SFR bits labeled '-', '0' or '1' can only be written and read as follows:
  - '-' Unless otherwise specified, must be written with '0', but can return any value when read (even if it was written with '0'). It is a reserved bit and may be used in future derivatives.
  - '0' must be written with '0', and will return a '0' when read.
  - '1' must be written with '1', and will return a '1' when read.

Table 7. P89LPC9102 special function registers *Écontinued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
RSTSRC	Reset source register	DFH	-	-	BOF	POF	-	R_WD	R_SF	R_EX	[3]	
RTCCON	Real-time clock control	D1H	RTCF	RTCS1	RTCS0	-	-	-	ERTC	RTCEN	60[4]	011x xx00
RTCH	Real-time clock register high	D2H									00[4]	0000 0000
RTCL	Real-time clock register low	D3H									00[4]	0000 0000
SP	Stack pointer	81H									07	0000 0111
TAMOD	Timer 0 and 1 auxiliary mode	8FH	-	-	-	T1M2	-	-	-	T0M2	00	xxx0 xxx0
	Bit address		8F	8E	8D	8C	8B	8A	89	88		
TCON*	Timer 0 and 1 control	88H	TF1	TR1	TF0	TR0	-	-	-	-	00	0000 0000
TH0	Timer 0 high	8CH									00	0000 0000
TH1	Timer 1 high	8DH									00	0000 0000
TL0	Timer 0 low	8AH									00	0000 0000
TL1	Timer 1 low	8BH									00	0000 0000
TMOD	Timer 0 and 1 mode	89H	-	-	T1M1	T1M0	-	-	T0M1	T0M0	00	0000 0000
TRIM	Internal oscillator trim register	96H	RCCLK	ENCLK	TRIM.5	TRIM.4	TRIM.3	TRIM.2	TRIM.1	TRIM.0	[4][5]	
WDCON	Watchdog control register	A7H	PRE2	PRE1	PRE0	-	-	WDRUN	WDTOF	WDCLK	[4][6]	
WDL	Watchdog load	C1H									FF	1111 1111
WFEED1	Watchdog feed 1	C2H										
WFEED2	Watchdog feed 2	C3H										

[1] Unimplemented bits in SFRs (labeled Õ-Õ) are X (unknown) at all times. Unless otherwise speciÞed, ones should not be written to these bits since they may be used for other purposes in future derivatives. The reset values shown for these bits are logic 0s although they are unknown when read.

[2] All ports are in input-only (high-impedance) state after power-up.

[3] The RSTSRC register reßects the cause of the P89LPC9102/9103/9107 reset. Upon a power-up reset, all reset source ßags are cleared except POF and BOF; the power-on reset value is xx11 0000.

[4] The only reset source that affects these SFRs is power-on reset.

[5] On power-on reset, the TRIM SFR is initialized with a factory preprogrammed value. Other resets will not cause initialization of the TRIM register.

[6] After reset, the value is 1110 01x1, i.e., PRE2 to PRE0 are all logic 1s, WDRUN = 1 and WDCLK = 1. WDTOF bit is logic 1 after watchdog timer reset and is logic 0 after power-on reset. Other resets will not affect WDTOF.

Table 8. P89LPC9103 special function registers *Écontinued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
FMDATA	Program ßash data	E5H									00	0000 0000
IEN0*	Interrupt enable 0	A8H	EA	EWDRT	EBO	ES/ESR	ET1	-	ET0	-	00	0000 0000
		Bit address	EF	EE	ED	EC	EB	EA	E9	E8		
IEN1*	Interrupt enable 1	E8H	EAD	EST	-	-	-	EC	EKBI	-	00[1]	00x0 0000
		Bit address	BF	BE	BD	BC	BB	BA	B9	B8		
IP0*	Interrupt priority 0	B8H	-	PWDRT	PBO	PS/PSR	PT1	-	PT0	-	00[1]	x000 0000
IP0H	Interrupt priority 0 high	B7H	-	PWDRTH	PBOH	PSH /PSRH	PT1H	-	PT0H	-	00[1]	x000 0000
		Bit address	FF	FE	FD	FC	FB	FA	F9	F8		
IP1*	Interrupt priority 1	F8H	PAD	PST	-	-	-	PC	PKBI	-	00[1]	00x0 0000
IP1H	Interrupt priority 1 high	F7H	PADH	PSTH	-	-	-	PCH	PKBIH	-	00[1]	00x0 0000
KBCON	Keypad control register	94H	-	-	-	-	-	-	PATN_SEL	KBIF	00[1]	xxxx xx00
KBMASK	Keypad interrupt mask register	86H		-	-	-	-	KBMASK.2	KBMASK.1	-	00	xxxx x00x
KBPATN	Keypad pattern register	93H	-	-	-	-	-	KBPATN.2	KBPATN.1	-	FF	xxxx x11x
		Bit address	87	86	85	84	83	82	81	80		
P0*	Port 0	80H	-	-	CMPREF /CLKIN	CIN1A	CIN1B	KBI2	KBI1	-	[3]	
		Bit address	97	96	95	94	93	92	91	90		
P1*	Port 1	90H	-	-	$\overline{\text{RST}}$	-	-	-	RXD	TXD		
P0M1	Port 0 output mode 1	84H	-	-	(P0M1.5)	(P0M1.4)	(P0M1.3)	(P0M1.2)	(P0M1.1)	-	FF	1111 1111
P0M2	Port 0 output mode 2	85H	-	-	(P0M2.5)	(P0M2.4)	(P0M2.3)	(P0M2.2)	(P0M2.1)	-	00	0000 0000
P1M1	Port 1 output mode 1	91H	-	-	-	-	-	-	(P1M1.1)	(P1M1.0)	FF[1]	1111 1111
P1M2	Port 1 output mode 2	92H	-	-	-	-	-	-	(P1M2.1)	(P1M2.0)	00[1]	0000 0000
PCON	Power control register	87H	SMOD1	SMOD0	BOPD	BOI	GF1	GF0	PMOD1	PMOD0	00	0000 0000
PCONA	Power control register A	B5H	RTCPD		VCPD	ADPD		-	SPD		00[1]	0000 0000
PCONB	reserved for Power control register B	B6H	-	-	-	-	-	-	-	-	00[1]	xxxx xxxx

[3] All ports are in input-only (high-impedance) state after power-up.

[4] The RSTSRC register reßects the cause of the P89LPC9102/9103/9107 reset. Upon a power-up reset, all reset source ßags are cleared except POF and BOF; the power-on reset value is xx11 0000.

[5] The only reset source that affects these SFRs is power-on reset.

[6] On power-on reset, the TRIM SFR is initialized with a factory preprogrammed value. Other resets will not cause initialization of the TRIM register.

[7] After reset, the value is 1110 01x1, i.e., PRE2 to PRE0 are all logic 1s, WDRUN = 1 and WDCLK = 1. WDTOF bit is logic 1 after watchdog timer reset and is logic 0 after power-on reset. Other resets will not affect WDTOF.

8.5 Watchdog oscillator option

The watchdog timer has a separate oscillator which has a frequency of 400 kHz. This oscillator can be used to save power when a high clock frequency is not needed.

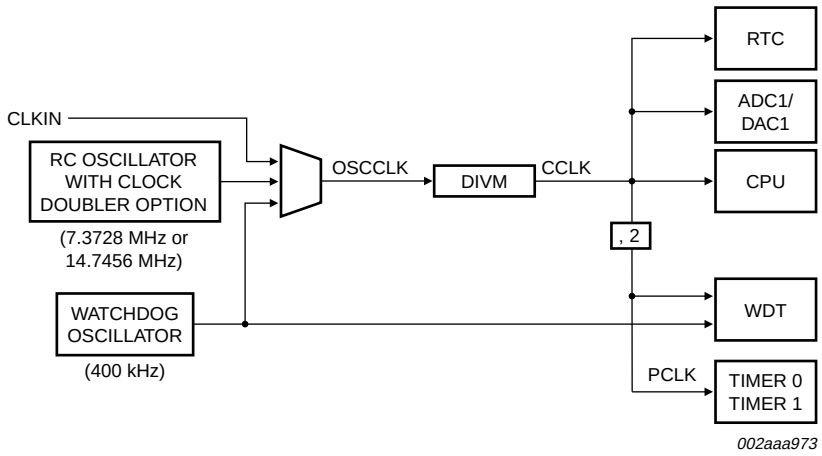

Fig 11. Block diagram of P89LPC9102 oscillator control

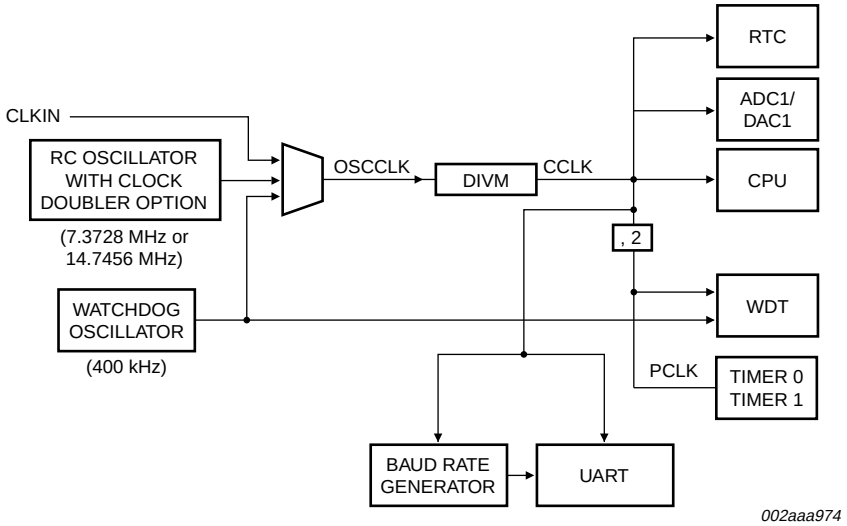

Fig 12. Block diagram of P89LPC9103/9107 oscillator control

8.6 External clock input option

In this conÞguration, the processor clock is derived from an external source driving the P0.5/CMPREF/CLKIN pin. The rate may be from 0 Hz up to 18 MHz. The P0.5/CMPREF/CLKIN pin may also be used as a standard port pin. When using an oscillator frequency above 12 MHz, the reset input function of P1.5 must be enabled. An external circuit is required to hold the device in reset at power-up until V_{DD} has reached its specified level. When system power is removed V_{DD} will fall below the minimum specified operating voltage. When using an oscillator

frequency above 12 MHz, in some applications, an external brownout detect circuit may be required to hold the device in reset when V_{DD} falls below the minimum specified operating voltage.

8.7 CCLK wake-up delay

The P89LPC9102/9103/9107 has an internal wake-up timer that delays the clock until it stabilizes depending to the clock source used.

8.8 CCLK modification: DIVM register

The OSCCLK frequency can be divided down up to 510 times by configuring a dividing register, DIVM, to generate CCLK. This feature makes it possible to temporarily run the CPU at a lower rate, reducing power consumption. By dividing the clock, the CPU can retain the ability to respond to events that would not exit Idle mode by executing its normal program at a lower rate. This can also allow bypassing the oscillator start-up time in cases where Power-down mode would otherwise be used. The value of DIVM may be changed by the program at any time without interrupting code execution.

8.9 Low power select

If CCLK is 8 MHz or slower, the CLKLP SFR bit (AUXR1.7) can be set to logic 1 to lower the power consumption further. On any reset, CLKLP is logic 0.

8.10 Memory organization

The various P89LPC9102/9103/9107 memory spaces are as follows:

- DATA

  128 bytes of internal data memory space (00H:7FH) accessed via direct or indirect addressing, using instruction other than MOVX and MOVC. All or part of the stack may be in this area.

- SFR

  Special Function Registers. Selected CPU registers and peripheral control and status registers, accessible only via direct addressing.

- CODE

  1 kB of Code memory space, accessed as part of program execution and via the MOVC instruction.

8.11 Interrupts

The P89LPC9102 supports nine interrupt sources: timers 0 and 1, brownout detect, watchdog timer/RTC, keyboard, comparator 1, and the A/D converter.

The P89LPC9103/9107 support nine interrupt sources: timers 0 and 1, serial port Tx, serial port Rx, combined serial port Rx/Tx, brownout detect, watchdog timer/RTC, keyboard, comparator, and the A/D converter.

Each interrupt source can be individually enabled or disabled by setting or clearing a bit in the interrupt enable registers IEN0 or IEN1. The IEN0 register also contains a global disable bit, EA, which disables all interrupts.

Each interrupt source can be individually programmed to one of four priority levels by setting or clearing bits in the interrupt priority registers IP0, IP0H, IP1, and IP1H. An interrupt service routine in progress can be interrupted by a higher priority interrupt, but not by another interrupt of the same or lower priority. The highest priority interrupt service cannot be interrupted by any other interrupt source. If two requests of different priority levels are pending at the start of an instruction, the request of higher priority level is serviced.

If requests of the same priority level are pending at the start of an instruction, an internal polling sequence determines which request is serviced. This is called the arbitration ranking. Note that the arbitration ranking is only used to resolve pending requests of the same priority level.

8.11.1 External interrupt inputs

The P89LPC9102/9103/9107 has a Keypad Interrupt function. This can be used as an external interrupt input.

If enabled when the P89LPC9102/9103/9107 is put into Power-down mode or Idle mode, the interrupt will cause the processor to wake-up and resume operation. Refer to Section 8.14 ÒPower reduction modesÓ for details.

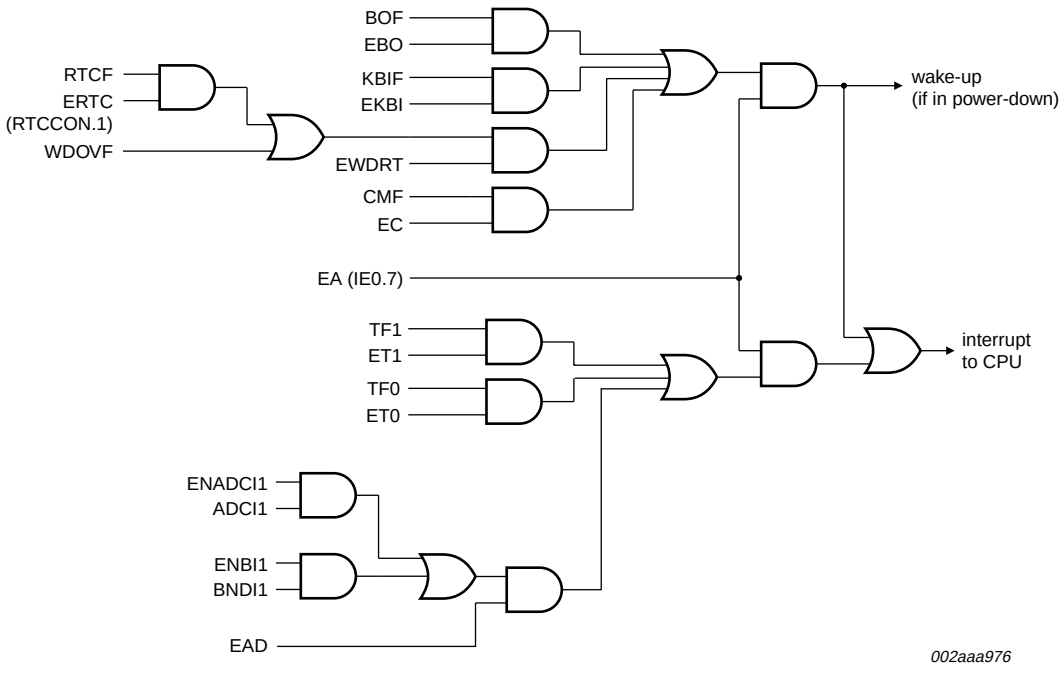

Fig 13. Interrupt sources, interrupt enables, and power-down wake-up sources (P89LPC9102)

8.14.2 Slow-down mode using the DIVM register

Slow-down mode is achieved by dividing down the OSCCLK frequency to generate CCLK. This division is accomplished by conÞguring the DIVM register to divide OSCCLK by up to 510 times. This feature makes it possible to temporarily run the CPU at a lower rate, reducing power consumption. By dividing the clock, the CPU can retain the ability to respond to events that would not exit Idle mode by executing its normal program at a lower rate. This can also allow bypassing the oscillator start-up time in cases where Power-down mode would otherwise be used. The value of DIVM may be changed by the program at any time without interrupting code execution.

8.14.3 Power-down mode

The Power-down mode stops the oscillator in order to minimize power consumption. The P89LPC9102/9103/9107 exits Power-down mode via any reset, or certain interrupts. In Power-down mode, the power supply voltage may be reduced to the data retention voltage V_{DDR}. This retains the RAM contents at the point where Power-down mode was entered. SFR contents are not guaranteed after V_{DD} has been lowered to V_{DDR}, therefore it is highly recommended to wake-up the processor via reset in this case. V_{DD} must be raised to within the operating range before the Power-down mode is exited.

Some chip functions continue to operate and draw power during Power-down mode, increasing the total power used during Power-down mode. These include: Brownout detect, watchdog timer, comparators (note that comparator can be powered-down separately), and RTC/system timer. The internal RC oscillator is disabled unless both the RC oscillator has been selected as the system clock and the RTC is enabled.

8.14.4 Total Power-down mode

This is the same as Power-down mode except that the brownout detection circuitry and the voltage comparators are also disabled to conserve additional power. The internal RC oscillator is disabled unless both the RC oscillator has been selected as the system clock and the RTC is enabled. If the internal RC oscillator is used to clock the RTC during Power-down mode, there will be high power consumption. Please use an external low frequency clock to achieve low power with the RTC running during Power-down mode.

8.15 Reset

The P1.5/$\overline{\text{RST}}$ pin can function as either an active-LOW reset input or as a digital input, P1.5. The RPE (Reset Pin Enable) bit in UCFG1, when set to logic 1, enables the external reset input function on P1.5. When cleared, P1.5 may be used as an input pin.

Remark: During a power-up sequence, the RPE selection is overridden and this pin will always function as a reset input. An external circuit connected to this pin should not hold this pin LOW during a power-on sequence as this will keep the device in reset. After power-up this input will function either as an external reset input or as a digital input as deÞned by the RPE bit. Only a power-up reset will temporarily override the selection deÞned by RPE bit. Other sources of reset will not override the RPE bit.

Remark: During a power cycle, V_{DD} must fall below V_{POR} (see Table 12 ÒStatic characteristicsÓ) before power is reapplied, in order to ensure a power-on reset.

Reset can be triggered from the following sources:

- External reset pin (during power-up or if user conÞgured via UCFG1)

- Power-on detect
- Brownout detect
- Watchdog timer
- Software reset
- UART break character detect reset (P89LPC9103/9107).

For every reset source, there is a flag in the Reset Register, RSTSRC. The user can read this register to determine the most recent reset source. These flag bits can be cleared in software by writing a logic 0 to the corresponding bit. More than one flag bit may be set:

- During a power-on reset, both POF and BOF are set but the other flag bits are cleared.
- For any other reset, previously set flag bits that have not been cleared will remain set.

8.16 Timers 0 and 1

The P89LPC9102 has two general purpose timer/counters which are similar to the standard 80C51 Timer 0 and Timer 1. These timers have five operating modes (modes 0, 1, 2, 3, and 6). Modes 0, 1, and 2 are the same for both Timers. Mode 3 is different.

The P89LPC9103/9107 has two general purpose timers which are similar to the standard 80C51 Timer 0 and Timer 1. These timers have four operating modes (modes 0, 1, 2, and 3). Modes 0, 1, and 2 are the same for both Timers. Mode 3 is different.

8.16.1 Mode 0

Putting either Timer into Mode 0 makes it look like an 8048 Timer, which is an 8-bit Counter with a divide-by-32 prescaler. In this mode, the Timer register is configured as a 13-bit register. Mode 0 operation is the same for Timer 0 and Timer 1.

8.16.2 Mode 1

Mode 1 is the same as Mode 0, except that all 16 bits of the timer register are used.

8.16.3 Mode 2

Mode 2 configures the Timer register as an 8-bit counter with automatic reload. Mode 2 operation is the same for Timer 0 and Timer 1.

8.16.4 Mode 3

When Timer 1 is in Mode 3 it is stopped. Timer 0 in Mode 3 forms two separate 8-bit counters and is provided for applications that require an extra 8-bit timer. When Timer 1 is in Mode 3 it can still be used by the serial port as a baud rate generator.

8.16.5 Mode 6 (P89LPC9102/9107)

In this mode, the corresponding timer can be changed to a PWM with a full period of 256 timer clocks.

8.18.4 Mode 3

11 bits are transmitted (through TXD) or received (through RXD): a start bit (logic 0), 8 data bits (LSB Þrst), a programmable 9th data bit, and a stop bit (logic 1). In fact, Mode 3 is the same as Mode 2 in all respects except baud rate. The baud rate in Mode 3 is variable and is determined by the Timer 1 overßow rate or the Baud Rate Generator (described in section Section 8.18.5 ÒBaud rate generator and selectionÓ).

8.18.5 Baud rate generator and selection

The P89LPC9103/9107 enhanced UART has an independent Baud Rate Generator. The baud rate is determined by a baud-rate preprogrammed into the BRGR1 and BRGR0 SFRs which together form a 16-bit baud rate divisor value that works in a similar manner as Timer 1. If the baud rate generator is used, Timer 1 can be used for other timing functions.

The UART can use either Timer 1 or the baud rate generator output (see Figure 15). Note that Timer T1 is further divided by 2 if the SMOD1 bit (PCON.7) is cleared. The independent Baud Rate Generator uses CCLK.

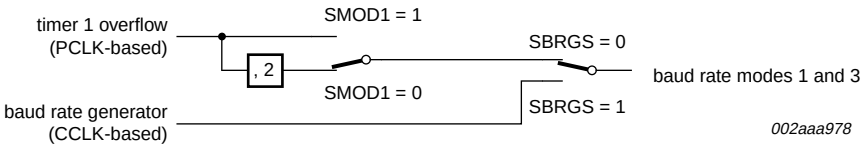

Fig 15. Baud rate sources for UART (Modes 1, 3)

8.18.6 Framing error

Framing error is reported in the status register (SSTAT). In addition, if SMOD0 (PCON.6) is logic 1, framing errors can be made available in SCON.7, respectively. If SMOD0 is logic 0, SCON.7 is SM0. It is recommended that SM0 and SM1 (SCON[7:6]) are set up when SMOD0 is logic 0.

8.18.7 Break detect

Break detect is reported in the status register (SSTAT). A break is detected when 11 consecutive bits are sensed LOW. The break detect can be used to reset the device.

8.18.8 Double buffering

The UART has a transmit double buffer that allows buffering of the next character to be written to SBUF while the Þrst character is being transmitted. Double buffering allows transmission of a string of characters with only one stop bit between any two characters, as long as the next character is written between the start bit and the stop bit of the previous character.

Double buffering can be disabled. If disabled (DBMOD, i.e., SSTAT.7 = 0), the UART is compatible with the conventional 80C51 UART. If enabled, the UART allows writing to SnBUF while the previous data is being shifted out. Double buffering is only allowed in Modes 1, 2 and 3. When operated in Mode 0, double buffering must be disabled (DBMOD = 0).

9.3 Block diagram

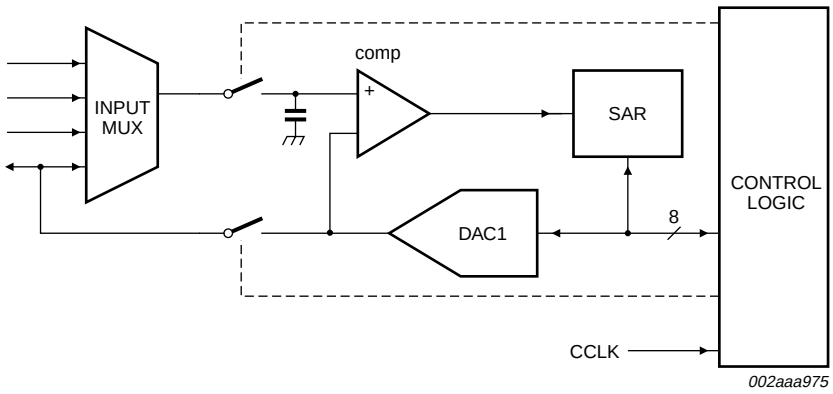

Fig 18. ADC block diagram

9.4 A/D operating modes

9.4.1 Fixed channel, single conversion mode

A single input channel can be selected for conversion. A single conversion will be performed and the result placed in the result register which corresponds to the selected input channel. An interrupt, if enabled, will be generated after the conversion completes.

9.4.2 Fixed channel, continuous conversion mode

A single input channel can be selected for continuous conversion. The results of the conversions will be sequentially placed in the four result registers. An interrupt, if enabled, will be generated after every four conversions. Additional conversion results will again cycle through the four result registers, overwriting the previous results. Continuous conversions continue until terminated by the user.

9.4.3 Auto scan, single conversion mode

Any combination of the four input channels can be selected for conversion. A single conversion of each selected input will be performed and the result placed in the result register which corresponds to the selected input channel. An interrupt, if enabled, will be generated after all selected channels have been converted. If only a single channel is selected this is equivalent to single channel, single conversion mode.

9.4.4 Auto scan, continuous conversion mode

Any combination of the four input channels can be selected for conversion. A conversion of each selected input will be performed and the result placed in the result register which corresponds to the selected input channel. An interrupt, if enabled, will be generated after all selected channels have been converted. The process will repeat starting with the Þrst selected channel. Additional conversion results will again cycle through the four result registers, overwriting the previous results. Continuous conversions continue until terminated by the user.

9.4.5 Dual channel, continuous conversion mode

This is a variation of the auto scan continuous conversion mode where conversion occurs on two user-selectable inputs. The result of the conversion of the Þrst channel is placed in result register, AD1DAT0. The result of the conversion of the second channel is placed in result register, AD1DAT1. The Þrst channel is again converted and its result stored in AD1DAT2. The second channel is again converted and its result placed in AD1DAT3. An interrupt is generated, if enabled, after every set of four conversions (two conversions per channel).

9.4.6 Single step mode

This special mode allows Ôsingle-steppingÕ in an auto scan conversion mode. Any combination of the four input channels can be selected for conversion. After each channel is converted, an interrupt is generated, if enabled, and the A/D waits for the next start condition. May be used with any of the start modes.

9.5 Conversion start modes

9.5.1 Timer triggered start

An A/D conversion is started by the overßow of Timer 0. Once a conversion has started, additional Timer 0 triggers are ignored until the conversion has completed. The Timer triggered start mode is available in all A/D operating modes.

9.5.2 Start immediately

Programming this mode immediately starts a conversion. This start mode is available in all A/D operating modes.

9.6 Boundary limits interrupt

The A/D converter has both a high and low boundary limit register. After the four MSBs have been converted, these four bits are compared with the four MSBs of the boundary high and low registers. If the four MSBs of the conversion are outside the limit an interrupt will be generated, if enabled. If the conversion result is within the limits, the boundary limits will again be compared after all 8 bits have been converted. An interrupt will be generated, if enabled, if the result is outside the boundary limits. The boundary limit may be disabled by clearing the boundary limit interrupt enable.

9.7 DAC output to a port pin with high output impedance

The A/D converterÕs DAC block can be output to a port pin. In this mode, the AD1DAT3 register is used to hold the value fed to the DAC. After a value has been written to the DAC (written to AD1DAT3), the DAC output will appear on the channel 3 pin.

9.8 Clock divider

The A/D converter requires that its internal clock source be in the range of 500 kHz to 3.3 MHz to maintain accuracy. A programmable clock divider that divides the clock from 1 to 8 is provided for this purpose.

10. Limiting values

Table 11. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions	Min	Max	Unit
$T_{amb(bias)}$	bias ambient temperature		- 55	+125	°C
T_{stg}	storage temperature		- 65	+150	°C
$I_{OH(I/O)}$	HIGH-level output current per input/output pin		-	8	mA
$I_{OL(I/O)}$	LOW-level output current per input/output pin		-	20	mA
$I_{I/Otot(max)}$	maximum total input/output current		-	120	mA
V_n	voltage on any other pin	except V_{SS}, with respect to V_{DD}	- 0.5	+5.5	V
$P_{tot(pack)}$	total power dissipation per package	based on package heat transfer, not device power consumption	-	1.5	W

[1] The following applies to Table 11 ÒLimiting valuesÓ

a) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in Table 12 ÒStatic characteristicsÓ and Table 13 ÒDynamic characteristics (12 MHz)Ósection of this speciÞcation are not implied.

b) This product includes circuitry speciÞcally designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

c) Parameters are valid over operating temperature range unless otherwise speciÞed. All voltages are with respect to V_{SS} unless otherwise noted.