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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	2560
Number of I/O	202
Number of Gates	54000
Voltage - Supply	3V ~ 3.6V, 4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TJ)
Package / Case	256-BFCQFP with Tie Bar
Supplier Device Package	256-CQFP (75x75)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/5962-9958501qxc

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Table 1 • Product profile

Device	A40MX02	A40MX04	A42MX09	A42MX16	A42MX24	A42MX36
Maximum Flip-Flops	147	273	516	928	1,410	1,822
Clocks	1	1	2	2	2	6
User I/O (maximum)	57	69	104	140	176	202
PCI	–	–	–	–	Yes	Yes
Boundary Scan Test (BST)	–	–	–	–	Yes	Yes
Packages (by pin count)						
PLCC	44, 68	44, 68, 84	84	84	84	–
PQFP	100	100	100, 144, 160	100, 160, 208	160, 208	208, 240
VQFP	80	80	100	100	–	–
TQFP	–	–	176	176	176	–
CQFP	–	–	–	172	–	208, 256
PBGA	–	–	–	–	–	272
CPGA	–	–	132	–	–	–

2.6 Temperature Grade Offerings

Table 4 • Temperature Grade Offerings

Package	A40MX02	A40MX04	A42MX09	A42MX16	A42MX24	A42MX36
PLCC 44	C, I, M	C, I, M				
PLCC 68	C, I, A, M	C, I, M				
PLCC 84		C, I, A, M	C, I, A, M	C, I, M	C, I, M	
PQFP 100	C, I, A, M	C, I, A, M	C, I, A, M	C, I, M		
PQFP 144			C			
PQFP 160			C, I, A, M	C, I, M	C, I, A, M	
PQFP 208				C, I, A, M	C, I, A, M	C, I, A, M
PQFP 240						C, I, A, M
VQFP 80	C, I, A, M	C, I, A, M				
VQFP 100			C, I, A, M	C, I, A, M		
TQFP 176			C, I, A, M	C, I, A, M	C, I, A, M	
PBGA 272						C, I, M
CQFP 172				C, M, B		
CQFP 208						C, M, B
CQFP 256						C, M, B
CPGA 132			C, M, B			

Note: C = Commercial
 I = Industrial
 A = Automotive
 M = Military
 B = MIL-STD-883 Class B

2.7 Speed Grade Offerings

Table 5 • Speed Grade Offerings

	– F	Std	–1	–2	–3
C	P	P	P	P	P
I		P	P	P	P
A		P			
M		P	P		
B		P	P		

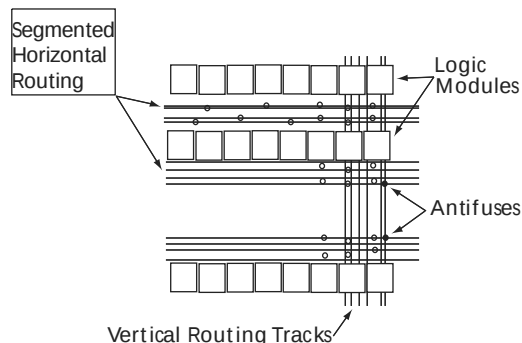
Note: See the 40MX and 42MX Automotive Family FPGAs datasheet for details on automotive-grade MX offerings.

Contact your local *Microsemi Sales representative* for device availability.

3.2.3.3 Antifuse Structures

An antifuse is a “normally open” structure. The use of antifuses to implement a programmable logic device results in highly testable structures as well as efficient programming algorithms. There are no pre-existing connections; temporary connections can be made using pass transistors. These temporary connections can isolate individual antifuses to be programmed and individual circuit structures to be tested, which can be done before and after programming. For instance, all metal tracks can be tested for continuity and shorts between adjacent tracks, and the functionality of all logic modules can be verified.

Figure 7 • MX Routing Structure



3.2.4 Clock Networks

The 40MX devices have one global clock distribution network (CLK). A signal can be put on the CLK network by being routed through the CLKBUF buffer.

In 42MX devices, there are two low-skew, high-fanout clock distribution networks, referred to as CLKA and CLKB. Each network has a clock module (CLKMOD) that can select the source of the clock signal from any of the following (Figure 8, page 11):

- Externally from the CLKA pad, using CLKBUF buffer
- Externally from the CLKB pad, using CLKBUF buffer
- Internally from the CLKINTA input, using CLKINT buffer
- Internally from the CLKINTB input, using CLKINT buffer

The clock modules are located in the top row of I/O modules. Clock drivers and a dedicated horizontal clock track are located in each horizontal routing channel.

Clock input pads in both 40MX and 42MX devices can also be used as normal I/Os, bypassing the clock networks.

The A42MX36 device has four additional register control resources, called quadrant clock networks (Figure 9, page 11). Each quadrant clock provides a local, high-fanout resource to the contiguous logic modules within its quadrant of the device. Quadrant clock signals can originate from specific I/O pins or from the internal array and can be used as a secondary register clock, register clear, or output enable.

3.3.7 Low Power Mode

42MX devices have been designed with a Low Power Mode. This feature, activated with setting the special LP pin to HIGH for a period longer than 800 ns, is particularly useful for battery-operated systems where battery life is a primary concern. In this mode, the core of the device is turned off and the device consumes minimal power with low standby current. In addition, all input buffers are turned off, and all outputs and bidirectional buffers are tristated. Since the core of the device is turned off, the states of the registers are lost. The device must be re-initialized when exiting Low Power Mode. I/Os can be driven during LP mode, and clock pins should be driven HIGH or LOW and should not float to avoid drawing current. To exit LP mode, the LP pin must be pulled LOW for over 200 μ s to allow for charge pumps to power up, and device initialization will begin.

3.4 Power Dissipation

The general power consumption of MX devices is made up of static and dynamic power and can be expressed with the following equation.

3.4.1 General Power Equation

$$P = [ICC_{standby} + ICC_{active}] * V_{CCI} + IOL * VOL * N + IOH * (V_{CCI} - VOH) * M$$

EQ 1

where:

- $ICC_{standby}$ is the current flowing when no inputs or outputs are changing.
- ICC_{active} is the current flowing due to CMOS switching.
- IOL , IOH are TTL sink/source currents.
- VOL , VOH are TTL level output voltages.
- N equals the number of outputs driving TTL loads to VOL .
- M equals the number of outputs driving TTL loads to VOH .

Accurate values for N and M are difficult to determine because they depend on the family type, on design details, and on the system I/O. The power can be divided into two components: static and active.

3.4.2 Static Power Component

The static power due to standby current is typically a small component of the overall power consumption. Standby power is calculated for commercial, worst-case conditions. The static power dissipation by TTL loads depends on the number of outputs driving, and on the DC load current. For instance, a 32-bit bus sinking 4mA at 0.33V will generate 42mW with all outputs driving LOW, and 140mW with all outputs driving HIGH. The actual dissipation will average somewhere in between, as I/Os switch states with time.

3.4.3 Active Power Component

Power dissipation in CMOS devices is usually dominated by the dynamic power dissipation. Dynamic power consumption is frequency-dependent and is a function of the logic and the external I/O. Active power dissipation results from charging internal chip capacitances of the interconnect, unprogrammed antifuses, module inputs, and module outputs, plus external capacitances due to PC board traces and load device inputs. An additional component of the active power dissipation is the totem pole current in the CMOS transistor pairs. The net effect can be associated with an equivalent capacitance that can be combined with frequency and voltage to represent active power dissipation.

The power dissipated by a CMOS circuit can be expressed by the equation:

$$\text{Power}(\mu\text{W}) = C_{EQ} * V_{CCA}^2 * F(1)$$

EQ 2

where:

- C_{EQ} = Equivalent capacitance expressed in picofarads (pF)

f_{q2} = Average second routed array clock rate in MHz)

Table 7 • Fixed Capacitance Values for MX FPGAs (pF)

Device Type	r1 routed_Clk1	r2 routed_Clk2
A40MX02	41.4	N/A
A40MX04	68.6	N/A
A42MX09	118	118
A42MX16	165	165
A42MX24	185	185
A42MX36	220	220

3.4.6 Test Circuitry and Silicon Explorer II Probe

MX devices contain probing circuitry that provides built-in access to every node in a design, via the use of Silicon Explorer II. Silicon Explorer II is an integrated hardware and software solution that, in conjunction with the Designer software, allow users to examine any of the internal nets of the device while it is operating in a prototyping or a production system. The user can probe into an MX device without changing the placement and routing of the design and without using any additional resources. Silicon Explorer II's noninvasive method does not alter timing or loading effects, thus shortening the debug cycle and providing a true representation of the device under actual functional situations.

Silicon Explorer II samples data at 100 MHz (asynchronous) or 66 MHz (synchronous). Silicon Explorer II attaches to a PC's standard COM port, turning the PC into a fully functional 18-channel logic analyzer. Silicon Explorer II allows designers to complete the design verification process at their desks and reduces verification time from several hours per cycle to a few seconds.

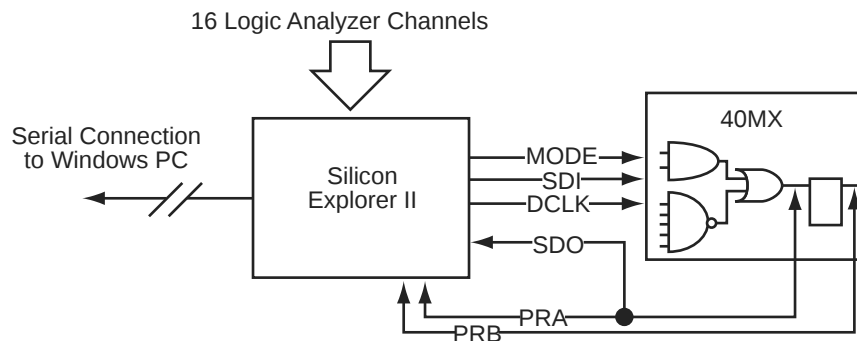
Silicon Explorer II is used to control the MODE, DCLK, SDI and SDO pins in MX devices to select the desired nets for debugging. The user simply assigns the selected internal nets in the Silicon Explorer II software to the PRA/PRB output pins for observation. Probing functionality is activated when the MODE pin is held HIGH.

Figure 12, page 16 illustrates the interconnection between Silicon Explorer II and 40MX devices, while Figure 13, page 17 illustrates the interconnection between Silicon Explorer II and 42MX devices

To allow for probing capabilities, the security fuses must not be programmed. (See User Security, page 12 for the security fuses of 40MX and 42MX devices). Table 8, page 17 summarizes the possible device configurations for probing.

PRA and PRB pins are dual-purpose pins. When the "Reserve Probe Pin" is checked in the Designer software, PRA and PRB pins are reserved as dedicated outputs for probing. If PRA and PRB pins are required as user I/Os to achieve successful layout and "Reserve Probe Pin" is checked, the layout tool will override the option and place user I/Os on PRA and PRB pins.

Figure 12 • Silicon Explorer II Setup with 40MX



3. All outputs unloaded. All inputs = VCC/VCCI or GND

3.8 3.3 V Operating Conditions

The following table shows 3.3 V operating conditions.

Table 16 • Absolute Maximum Ratings for 40MX Devices*

Symbol	Parameter	Limits	Units
VCC	DC Supply Voltage	–0.5 to +7.0	V
VI	Input Voltage	–0.5 to VCC + 0.5	V
VO	Output Voltage	–0.5 to VCC + 0.5	V
t _{STG}	Storage Temperature	–65 to +150	°C

Note: *Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the recommended operating conditions.

Table 17 • Absolute Maximum Ratings for 42MX Devices*

Symbol	Parameter	Limits	Units
VCCI	DC Supply Voltage for I/Os	–0.5 to +7.0	V
VCCA	DC Supply Voltage for Array	–0.5 to +7.0	V
VI	Input Voltage	–0.5 to VCCI+0.5	V
VO	Output Voltage	–0.5 to VCCI+0.5	V
t _{STG}	Storage Temperature	–65 to +150	°C

Note: *Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the recommended operating conditions.

Table 18 • Recommended Operating Conditions

Parameter	Commercial	Industrial	Military	Units
Temperature Range*	0 to +70	–40 to +85	–55 to +125	°C
VCC (40MX)	3.0 to 3.6	3.0 to 3.6	3.0 to 3.6	V
VCCA (42MX)	3.0 to 3.6	3.0 to 3.6	3.0 to 3.6	V
VCCI (42MX)	3.0 to 3.6	3.0 to 3.6	3.0 to 3.6	V

Note: *Ambient temperature (T_A) is used for commercial and industrial grades; case temperature (T_C) is used for military grades.

All the following tables show various specifications and operating conditions of 40MX and 42MX FPGAs.

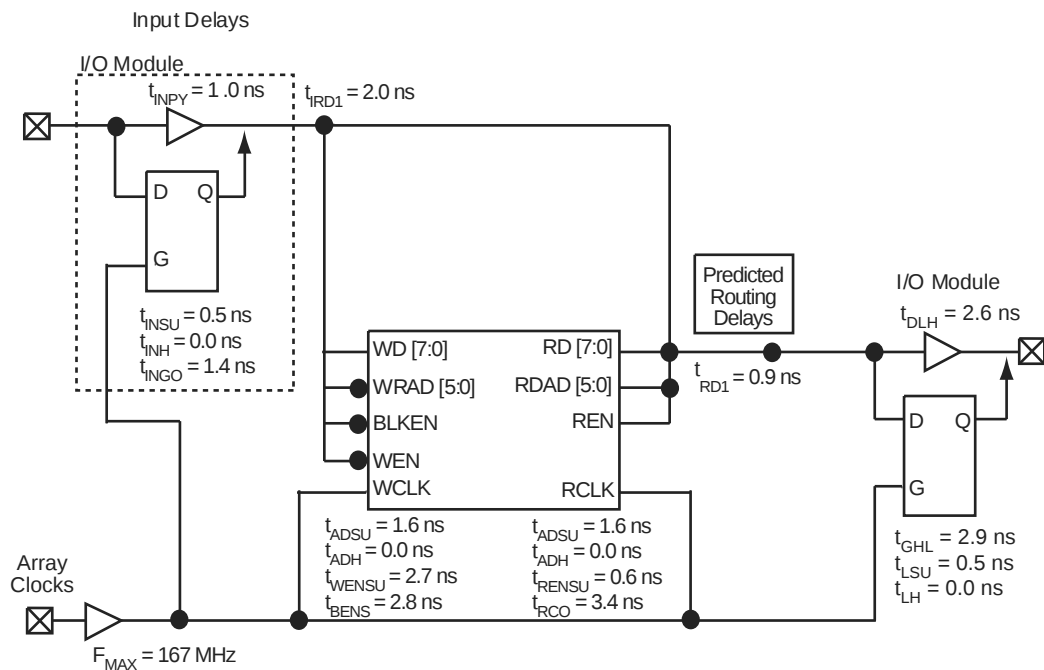
reliability. Devices should not be operated outside the recommended operating conditions.

Table 21 • Recommended Operating Conditions

Parameter	Commercial	Industrial	Military	Units
Temperature Range*	0 to +70	–40 to +85	–55 to +125	°C
VCCA	4.75 to 5.25	4.5 to 5.5	4.5 to 5.5	V
VCCI	3.14 to 3.47	3.0 to 3.6	3.0 to 3.6	V

Note: *Ambient temperature (T_A) is used for commercial and industrial grades; case temperature (T_C) is used for military grades.

Figure 20 • 42MX Timing Model (SRAM Functions)



Note: Values are shown for A42MX36 –3 at 5.0 V worst-case commercial conditions.

3.10.1 Parameter Measurement

The following figures show parameter measurement details.

Figure 21 • Output Buffer Delays

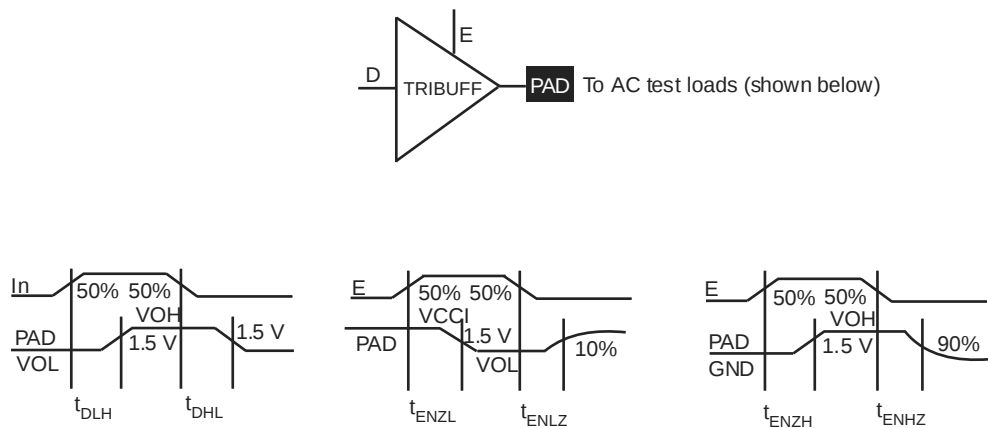


Table 38 • A42MX09 Timing Characteristics (Nominal 5.0 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description			–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Input Module Propagation Delays													
t _{INYH}	Pad-to-Y HIGH			1.0		1.2		1.3		1.6		2.2	ns
t _{INYL}	Pad-to-Y LOW			0.8		0.9		1.0		1.2		1.7	ns
t _{INGH}	G to Y HIGH			1.3		1.4		1.6		1.9		2.7	ns
t _{INGL}	G to Y LOW			1.3		1.4		1.6		1.9		2.7	ns
Input Module Predicted Routing Delays ²													
t _{IRD1}	FO = 1 Routing Delay			2.0		2.2		2.5		3.0		4.2	ns
t _{IRD2}	FO = 2 Routing Delay			2.3		2.5		2.9		3.4		4.7	ns
t _{IRD3}	FO = 3 Routing Delay			2.5		2.8		3.2		3.7		5.2	ns
t _{IRD4}	FO = 4 Routing Delay			2.8		3.1		3.5		4.1		5.7	ns
t _{IRD8}	FO = 8 Routing Delay			3.7		4.1		4.7		5.5		7.7	ns
Global Clock Network													
t _{CKH}	Input LOW to HIGH	FO = 32		2.4		2.7		3.0		3.6		5.0	ns
		FO = 256		2.7		3.0		3.4		4.0		5.5	ns
t _{CKL}	Input HIGH to LOW	FO = 32		3.5		3.9		4.4		5.2		7.3	ns
		FO = 256		3.9		4.3		4.9		5.7		8.0	ns
t _{PWH}	Minimum Pulse Width HIGH	FO = 32	1.2		1.4		1.5		1.8		2.5		ns
		FO = 256	1.3		1.5		1.7		2.0		2.7		ns
t _{PWL}	Minimum Pulse Width LOW	FO = 32	1.2		1.4		1.5		1.8		2.5		ns
		FO = 256	1.3		1.5		1.7		2.0		2.7		ns
t _{CKSW}	Maximum Skew	FO = 32		0.3		0.3		0.4		0.5		0.6	ns
		FO = 256		0.3		0.3		0.4		0.5		0.6	ns
t _{SUEXT}	Input Latch External Set-Up	FO = 32	0.0		0.0		0.0		0.0		0.0		ns
		FO = 256	0.0		0.0		0.0		0.0		0.0		ns
t _{HEXT}	Input Latch External Hold	FO = 32	2.3		2.6		3.0		3.5		4.9		ns
		FO = 256	2.2		2.4		3.3		3.9		5.5		ns
t _P	Minimum Period	FO = 32	3.4		3.7		4.0		4.7		7.8		ns
		FO = 256	3.7		4.1		4.5		5.2		8.6		ns
f _{MAX}	Maximum Frequency	FO = 32		296		269		247		215		129	MHz
		FO = 256		268		244		224		195		117	MHz

Table 40 • A42MX16 Timing Characteristics (Nominal 5.0 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
TTL Output Module Timing ⁴												
t _{DLH}	Data-to-Pad HIGH	2.5		2.8		3.2		3.7		5.2		ns
t _{DHL}	Data-to-Pad LOW	3.0		3.3		3.7		4.4		6.1		ns
t _{ENZH}	Enable Pad Z to HIGH	2.7		3.0		3.4		4.0		5.6		ns
t _{ENZL}	Enable Pad Z to LOW	3.0		3.3		3.8		4.4		6.2		ns
t _{ENHZ}	Enable Pad HIGH to Z	5.4		6.0		6.8		8.0		11.2		ns
t _{ENLZ}	Enable Pad LOW to Z	5.0		5.6		6.3		7.4		10.4		ns
t _{GLH}	G-to-Pad HIGH	2.9		3.2		3.6		4.3		6.0		ns
t _{GHL}	G-to-Pad LOW	2.9		3.2		3.6		4.3		6.0		ns
t _{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading	5.7		6.3		7.1		8.4		11.9		ns
t _{ACO}	Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading	8.0		8.9		10.1		11.9		16.7		ns
d _{TLH}	Capacitive Loading, LOW to HIGH	0.03		0.03		0.03		0.04		0.06		ns/pF
d _{THL}	Capacitive Loading, HIGH to LOW	0.04		0.04		0.04		0.05		0.07		ns/pF

Table 41 • A42MX16 Timing Characteristics (Nominal 3.3 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)

Parameter / Description			–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{PWL}	Minimum Pulse Width LOW	FO = 32	5.3		5.9		6.7		7.8		11.0		ns
		FO = 384	6.2		6.9		7.9		9.2		12.9		ns
t _{CKSW}	Maximum Skew	FO = 32		0.5		0.5		0.6		0.7		1.0	ns
		FO = 384		2.2		2.4		2.7		3.2		4.5	ns
t _{SUEXT}	Input Latch External Set-Up	FO = 32	0.0		0.0		0.0		0.0		0.0		ns
		FO = 384	0.0		0.0		0.0		0.0		0.0		ns
t _{HEXT}	Input Latch External Hold	FO = 32	3.9		4.3		4.9		5.7		8.0		ns
		FO = 384	4.5		4.9		5.6		6.6		9.2		ns
t _p	Minimum Period	FO = 32	7.0		7.8		8.4		9.7		16.2		ns
		FO = 384	7.7		8.6		9.3		10.7		17.8		ns
f _{MAX}	Maximum Frequency	FO = 32		142		129		119		103		62	MHz
		FO = 384		129		117		108		94		56	MHz
TTL Output Module Timing ⁵													
t _{DLH}	Data-to-Pad HIGH			3.5		3.9		4.4		5.2		7.3	ns
t _{DHL}	Data-to-Pad LOW			4.1		4.6		5.2		6.1		8.6	ns
t _{ENZH}	Enable Pad Z to HIGH			3.8		4.2		4.8		5.6		7.8	ns
t _{ENZL}	Enable Pad Z to LOW			4.2		4.6		5.3		6.2		8.7	ns
t _{ENHZ}	Enable Pad HIGH to Z			7.6		8.4		9.5		11.2		15.7	ns
t _{ENLZ}	Enable Pad LOW to Z			7.0		7.8		8.8		10.4		14.5	ns
t _{GLH}	G-to-Pad HIGH			4.8		5.3		6.0		7.2		10.0	ns
t _{GHL}	G-to-Pad LOW			4.8		5.3		6.0		7.2		10.0	ns
t _{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading			8.0		8.9		10.1		11.9		16.7	ns
t _{ACO}	Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading			11.3		12.5		14.2		16.7		23.3	ns
d _{TLH}	Capacitive Loading, LOW to HIGH			0.04		0.04		0.05		0.06		0.08	ns/pF
d _{THL}	Capacitive Loading, HIGH to LOW			0.05		0.05		0.06		0.07		0.10	ns/pF
CMOS Output Module Timing ⁵													
t _{DLH}	Data-to-Pad HIGH			4.5		5.0		5.6		6.6		9.3	ns
t _{DHL}	Data-to-Pad LOW			3.4		3.8		4.3		5.1		7.1	ns
t _{ENZH}	Enable Pad Z to HIGH			3.8		4.2		4.8		5.6		7.8	ns
t _{ENZL}	Enable Pad Z to LOW			4.2		4.6		5.3		6.2		8.7	ns
t _{ENHZ}	Enable Pad HIGH to Z			7.6		8.4		9.5		11.2		15.7	ns
t _{ENLZ}	Enable Pad LOW to Z			7.0		7.8		8.8		10.4		14.5	ns
t _{GLH}	G-to-Pad HIGH			7.1		7.9		8.9		10.5		14.7	ns
t _{GHL}	G-to-Pad LOW			7.1		7.9		8.9		10.5		14.7	ns
t _{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading			8.0		8.9		10.1		11.9		16.7	ns

Table 45 • A42MX36 Timing Characteristics (Nominal 3.3 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Synchronous SRAM Operations (continued)												
t _{ADH}	Address/Data Hold Time	0.0		0.0		0.0		0.0		0.0		ns
t _{RENSU}	Read Enable Set-Up	0.9		1.0		1.1		1.3		1.8		ns
t _{RENH}	Read Enable Hold	4.8		5.3		6.0		7.0		9.8		ns
t _{WENSU}	Write Enable Set-Up	3.8		4.2		4.8		5.6		7.8		ns
t _{WENH}	Write Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{BENS}	Block Enable Set-Up	3.9		4.3		4.9		5.7		8.0		ns
t _{BENH}	Block Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
Asynchronous SRAM Operations												
t _{RPD}	Asynchronous Access Time		11.3		12.6		14.3		16.8		23.5	ns
t _{RDADV}	Read Address Valid	12.3		13.7		15.5		18.2		25.5		ns
t _{ADSU}	Address/Data Set-Up Time	2.3		2.5		2.8		3.4		4.8		ns
t _{ADH}	Address/Data Hold Time	0.0		0.0		0.0		0.0		0.0		ns
t _{RENSUA}	Read Enable Set-Up to Address Valid	0.9		1.0		1.1		1.3		1.8		ns
t _{RENHA}	Read Enable Hold	4.8		5.3		6.0		7.0		9.8		ns
t _{WENSU}	Write Enable Set-Up	3.8		4.2		4.8		5.6		7.8		ns
t _{WENH}	Write Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{DOH}	Data Out Hold Time		1.8		2.0		2.1		2.5		3.5	ns
Input Module Propagation Delays												
t _{INPY}	Input Data Pad-to-Y		1.4		1.6		1.8		2.1		3.0	ns
t _{INGO}	Input Latch Gate-to-Output		2.0		2.2		2.5		2.9		4.1	ns
t _{INH}	Input Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{INSU}	Input Latch Set-Up	0.7		0.7		0.8		1.0		1.4		ns
t _{ILA}	Latch Active Pulse Width	6.5		7.3		8.2		9.7		13.5		ns

Table 48 • PL68

PL68		
Pin Number	A40MX02 Function	A40MX04 Function
61	I/O	I/O
62	I/O	I/O
63	I/O	I/O
64	I/O	I/O
65	I/O	I/O
66	GND	GND
67	I/O	I/O
68	I/O	I/O

Figure 40 • PL84

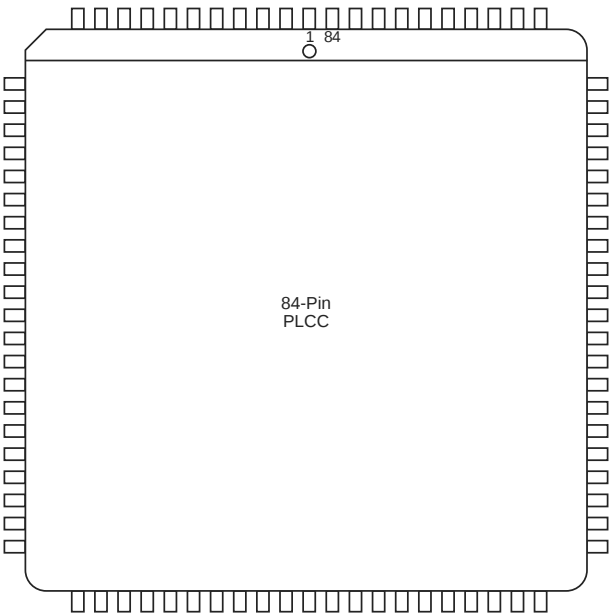


Table 49 • PL84

PL84				
Pin Number	A40MX04 Function	A42MX09 Function	A42MX16 Function	A42MX24 Function
1	I/O	I/O	I/O	I/O
2	I/O	CLKB, I/O	CLKB, I/O	CLKB, I/O
3	I/O	I/O	I/O	I/O
4	VCC	PRB, I/O	PRB, I/O	PRB, I/O
5	I/O	I/O	I/O	WD, I/O
6	I/O	GND	GND	GND
7	I/O	I/O	I/O	I/O
8	I/O	I/O	I/O	WD, I/O
9	I/O	I/O	I/O	WD, I/O

Table 49 • PL84

PL84				
Pin Number	A40MX04 Function	A42MX09 Function	A42MX16 Function	A42MX24 Function
47	I/O	I/O	I/O	WD, I/O
48	I/O	I/O	I/O	I/O
49	I/O	GND	GND	GND
50	I/O	I/O	I/O	WD, I/O
51	I/O	I/O	I/O	WD, I/O
52	I/O	SDO, I/O	SDO, I/O	SDO, TDO, I/O
53	I/O	I/O	I/O	I/O
54	I/O	I/O	I/O	I/O
55	I/O	I/O	I/O	I/O
56	I/O	I/O	I/O	I/O
57	I/O	I/O	I/O	I/O
58	I/O	I/O	I/O	I/O
59	I/O	I/O	I/O	I/O
60	GND	I/O	I/O	I/O
61	GND	I/O	I/O	I/O
62	I/O	I/O	I/O	TCK, I/O
63	I/O	LP	LP	LP
64	CLK, I/O	VCCA	VCCA	VCCA
65	I/O	VCCI	VCCI	VCCI
66	MODE	I/O	I/O	I/O
67	VCC	I/O	I/O	I/O
68	VCC	I/O	I/O	I/O
69	I/O	I/O	I/O	I/O
70	I/O	GND	GND	GND
71	I/O	I/O	I/O	I/O
72	SDI, I/O	I/O	I/O	I/O
73	DCLK, I/O	I/O	I/O	I/O
74	PRA, I/O	I/O	I/O	I/O
75	PRB, I/O	I/O	I/O	I/O
76	I/O	SDI, I/O	SDI, I/O	SDI, I/O
77	I/O	I/O	I/O	I/O
78	I/O	I/O	I/O	WD, I/O
79	I/O	I/O	I/O	WD, I/O
80	I/O	I/O	I/O	WD, I/O
81	I/O	PRA, I/O	PRA, I/O	PRA, I/O
82	GND	I/O	I/O	I/O
83	I/O	CLKA, I/O	CLKA, I/O	CLKA, I/O

Table 54 • PQ240

PQ240	
Pin Number	A42MX36 Function
89	VCCI
90	VCCA
91	LP
92	TCK, I/O
93	I/O
94	GND
95	I/O
96	I/O
97	I/O
98	I/O
99	I/O
100	I/O
101	I/O
102	I/O
103	I/O
104	I/O
105	I/O
106	I/O
107	I/O
108	VCCI
109	I/O
110	I/O
111	I/O
112	I/O
113	I/O
114	I/O
115	I/O
116	I/O
117	I/O
118	VCCA
119	GND
120	GND
121	GND
122	I/O
123	SDO, TDO, I/O
124	I/O
125	WD, I/O

Table 57 • TQ176

TQ176			
Pin Number	A42MX09 Function	A42MX16 Function	A42MX24 Function
84	I/O	I/O	WD, I/O
85	I/O	I/O	WD, I/O
86	NC	I/O	I/O
87	SDO, I/O	SDO, I/O	SDO, TDO, I/O
88	I/O	I/O	I/O
89	GND	GND	GND
90	I/O	I/O	I/O
91	I/O	I/O	I/O
92	I/O	I/O	I/O
93	I/O	I/O	I/O
94	I/O	I/O	I/O
95	I/O	I/O	I/O
96	NC	I/O	I/O
97	NC	I/O	I/O
98	I/O	I/O	I/O
99	I/O	I/O	I/O
100	I/O	I/O	I/O
101	NC	NC	I/O
102	I/O	I/O	I/O
103	NC	I/O	I/O
104	I/O	I/O	I/O
105	I/O	I/O	I/O
106	GND	GND	GND
107	NC	I/O	I/O
108	NC	I/O	TCK, I/O
109	LP	LP	LP
110	VCCA	VCCA	VCCA
111	GND	GND	GND
112	VCCI	VCCI	VCCI
113	VCCA	VCCA	VCCA
114	NC	I/O	I/O
115	NC	I/O	I/O
116	NC	VCCA	VCCA
117	I/O	I/O	I/O
118	I/O	I/O	I/O
119	I/O	I/O	I/O
120	I/O	I/O	I/O

Table 59 • CQ256

CQ256	
Pin Number	A42MX36 Function
59	I/O
60	VCCA
61	GND
62	GND
63	NC
64	NC
65	NC
66	I/O
67	SDO, TDO, I/O
68	I/O
69	WD, I/O
70	WD, I/O
71	I/O
72	VCCI
73	I/O
74	I/O
75	I/O
76	WD, I/O
77	GND
78	WD, I/O
79	I/O
80	QCLKB, I/O
81	I/O
82	I/O
83	I/O
84	I/O
85	I/O
86	I/O
87	WD, I/O
88	WD, I/O
89	I/O
90	I/O
91	I/O
92	I/O
93	I/O
94	I/O
95	VCCI

Table 60 • BG272

BG272	
Pin Number	A42MX36 Function
M10	GND
M11	GND
M12	GND
M17	I/O
M18	I/O
M19	I/O
M20	I/O
N1	I/O
N2	I/O
N3	I/O
N4	VCCI
N17	VCCI
N18	I/O
N19	I/O
N20	I/O
P1	I/O
P2	I/O
P3	I/O
P4	VCCA
P17	I/O
P18	I/O
P19	I/O
P20	I/O
R1	I/O
R2	I/O
R3	I/O
R4	VCCI
R17	VCCI
R18	I/O
R19	I/O
R20	I/O
T1	I/O
T2	I/O
T3	I/O
T4	I/O
T17	VCCA
T18	I/O

Table 60 • BG272

BG272	
Pin Number	A42MX36 Function
Y13	I/O
Y14	I/O
Y15	I/O
Y16	I/O
Y17	I/O
Y18	WD, I/O
Y19	GND
Y20	GND

Figure 52 • PG132

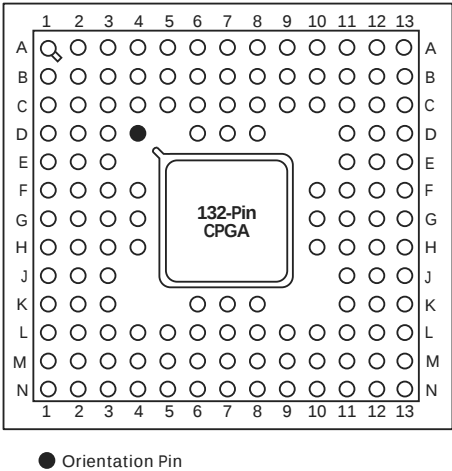


Table 61 • PG132

PG132	
Pin Number	A42MX09 Function
–	PMPOUT
B2	I/O
A1	MODE
B1	I/O
D3	I/O
C2	I/O
C1	I/O
D2	I/O
D1	I/O
E2	I/O
E1	I/O
F3	I/O