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### Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	34
Number of Gates	3000
Voltage - Supply	3V ~ 3.6V, 4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/a40mx02-1pl44i">https://www.e-xfl.com/product-detail/microchip-technology/a40mx02-1pl44i</a>

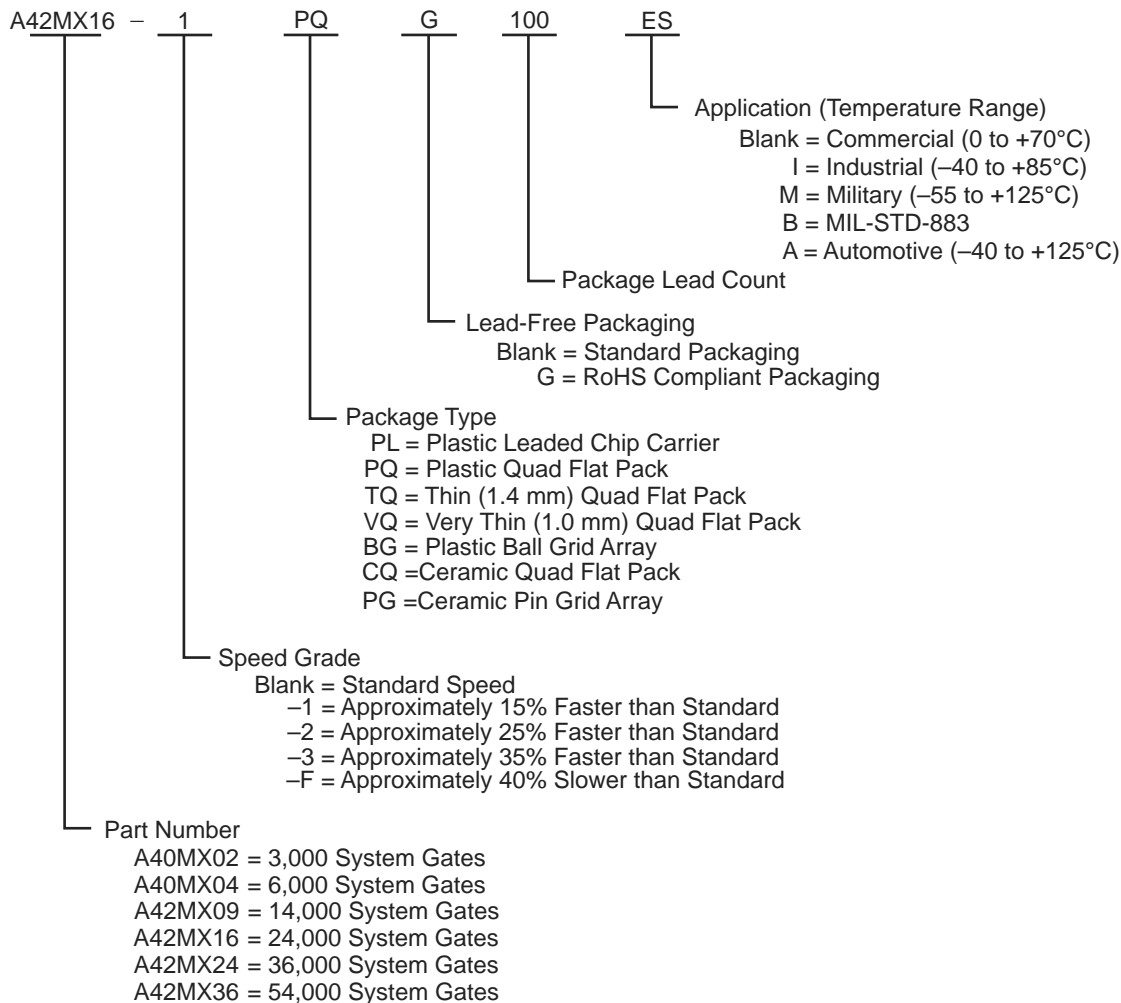
**Table 1 • Product profile**

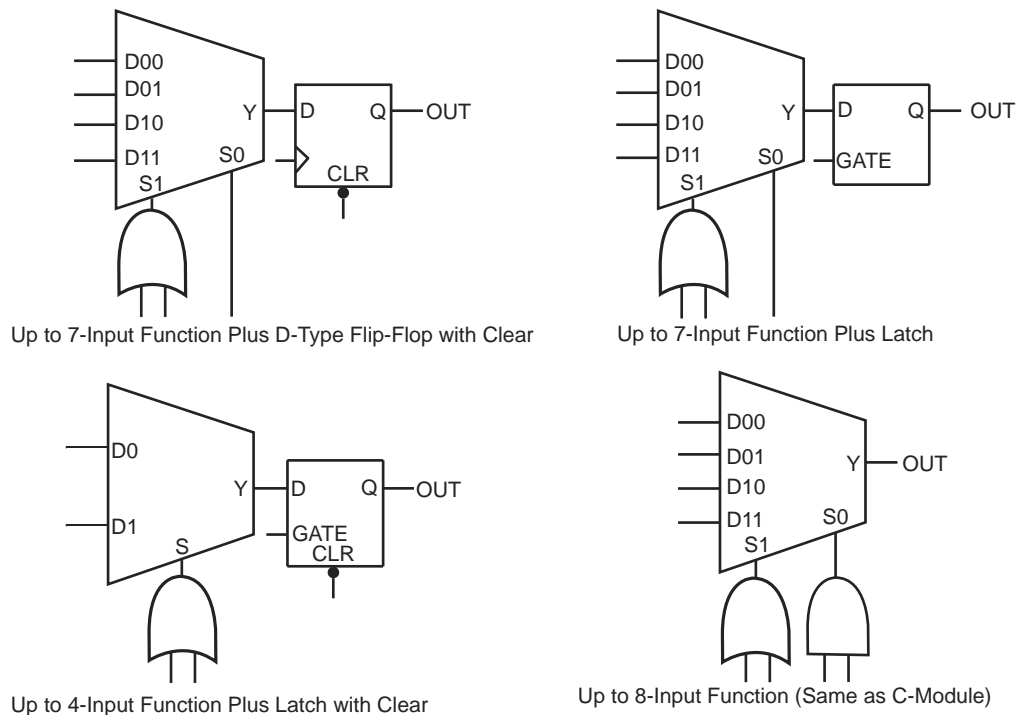
Device	A40MX02	A40MX04	A42MX09	A42MX16	A42MX24	A42MX36
<b>Maximum Flip-Flops</b>	147	273	516	928	1,410	1,822
<b>Clocks</b>	1	1	2	2	2	6
<b>User I/O (maximum)</b>	57	69	104	140	176	202
<b>PCI</b>	–	–	–	–	Yes	Yes
<b>Boundary Scan Test (BST)</b>	–	–	–	–	Yes	Yes
Packages (by pin count)						
PLCC	44, 68	44, 68, 84	84	84	84	–
PQFP	100	100	100, 144, 160	100, 160, 208	160, 208	208, 240
VQFP	80	80	100	100	–	–
TQFP	–	–	176	176	176	–
CQFP	–	–	–	172	–	208, 256
PBGA	–	–	–	–	–	272
CPGA	–	–	132	–	–	–

## 2.3 Ordering Information

The following figure shows ordering information. All the following tables show plastic and ceramic device resources, temperature and speed grade offerings.

**Figure 1 • Ordering Information**



**Figure 4 • 42MX S-Module Implementation**

A42MX24 and A42MX36 devices contain D-modules, which are arranged around the periphery of the device. D-modules contain wide-decode circuitry, providing a fast, wide-input AND function similar to that found in CPLD architectures (Figure 5, page 9). The D-module allows A42MX24 and A42MX36 devices to perform wide-decode functions at speeds comparable to CPLDs and PALs. The output of the D-module has a programmable inverter for active HIGH or LOW assertion. The D-module output is hardwired to an output pin, and can also be fed back into the array to be incorporated into other logic.

### 3.2.2 Dual-Port SRAM Modules

The A42MX36 device contains dual-port SRAM modules that have been optimized for synchronous or asynchronous applications. The SRAM modules are arranged in 256-bit blocks that can be configured as 32x8 or 64x4. SRAM modules can be cascaded together to form memory spaces of user-definable width and depth. A block diagram of the A42MX36 dual-port SRAM block is shown in Figure 6, page 9.

The A42MX36 SRAM modules are true dual-port structures containing independent read and write ports. Each SRAM module contains six bits of read and write addressing (RDAD[5:0] and WRAD[5:0], respectively) for 64x4-bit blocks. When configured in byte mode, the highest order address bits (RDAD5 and WRAD5) are not used. The read and write ports of the SRAM block contain independent clocks (RCLK and WCLK) with programmable polarities offering active HIGH or LOW implementation. The SRAM block contains eight data inputs (WD[7:0]), and eight outputs (RD[7:0]), which are connected to segmented vertical routing tracks.

The A42MX36 dual-port SRAM blocks provide an optimal solution for high-speed buffered applications requiring FIFO and LIFO queues. The ACTgen Macro Builder within Microsemi's designer software provides capability to quickly design memory functions with the SRAM blocks. Unused SRAM blocks can be used to implement registers for other user logic within the design.

### 3.3.7 Low Power Mode

42MX devices have been designed with a Low Power Mode. This feature, activated with setting the special LP pin to HIGH for a period longer than 800 ns, is particularly useful for battery-operated systems where battery life is a primary concern. In this mode, the core of the device is turned off and the device consumes minimal power with low standby current. In addition, all input buffers are turned off, and all outputs and bidirectional buffers are tristated. Since the core of the device is turned off, the states of the registers are lost. The device must be re-initialized when exiting Low Power Mode. I/Os can be driven during LP mode, and clock pins should be driven HIGH or LOW and should not float to avoid drawing current. To exit LP mode, the LP pin must be pulled LOW for over 200  $\mu$ s to allow for charge pumps to power up, and device initialization will begin.

## 3.4 Power Dissipation

The general power consumption of MX devices is made up of static and dynamic power and can be expressed with the following equation.

### 3.4.1 General Power Equation

$$P = [ICC_{\text{standby}} + ICC_{\text{active}}] \cdot V_{CCI} + I_{OL} \cdot V_{OL} \cdot N + I_{OH} \cdot (V_{CCI} - V_{OH}) \cdot M$$

EQ 1

where:

- $ICC_{\text{standby}}$  is the current flowing when no inputs or outputs are changing.
- $ICC_{\text{active}}$  is the current flowing due to CMOS switching.
- $I_{OL}$ ,  $I_{OH}$  are TTL sink/source currents.
- $V_{OL}$ ,  $V_{OH}$  are TTL level output voltages.
- $N$  equals the number of outputs driving TTL loads to  $V_{OL}$ .
- $M$  equals the number of outputs driving TTL loads to  $V_{OH}$ .

Accurate values for  $N$  and  $M$  are difficult to determine because they depend on the family type, on design details, and on the system I/O. The power can be divided into two components: static and active.

### 3.4.2 Static Power Component

The static power due to standby current is typically a small component of the overall power consumption. Standby power is calculated for commercial, worst-case conditions. The static power dissipation by TTL loads depends on the number of outputs driving, and on the DC load current. For instance, a 32-bit bus sinking 4mA at 0.33V will generate 42mW with all outputs driving LOW, and 140mW with all outputs driving HIGH. The actual dissipation will average somewhere in between, as I/Os switch states with time.

### 3.4.3 Active Power Component

Power dissipation in CMOS devices is usually dominated by the dynamic power dissipation. Dynamic power consumption is frequency-dependent and is a function of the logic and the external I/O. Active power dissipation results from charging internal chip capacitances of the interconnect, unprogrammed antifuses, module inputs, and module outputs, plus external capacitances due to PC board traces and load device inputs. An additional component of the active power dissipation is the totem pole current in the CMOS transistor pairs. The net effect can be associated with an equivalent capacitance that can be combined with frequency and voltage to represent active power dissipation.

The power dissipated by a CMOS circuit can be expressed by the equation:

$$\text{Power}(\mu\text{W}) = C_{EQ} \cdot V_{CCA}^2 \cdot F(1)$$

EQ 2

where:

- $C_{EQ}$  = Equivalent capacitance expressed in picofarads (pF)

**Note:** \*Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the recommended operating conditions.

**Table 14 • Recommended Operating Conditions**

Parameter	Commercial	Industrial	Military	Units
Temperature Range*	0 to +70	–40 to +85	–55 to +125	°C
VCC (40MX)	4.75 to 5.25	4.5 to 5.5	4.5 to 5.5	V
VCCA (42MX)	4.75 to 5.25	4.5 to 5.5	4.5 to 5.5	V
VCCI (42MX)	4.75 to 5.25	4.5 to 5.5	4.5 to 5.5	V

**Note:** \* Ambient temperature ( $T_A$ ) is used for commercial and industrial grades; case temperature ( $T_C$ ) is used for military grades.

### 3.7.1 5 V TTL Electrical Specifications

The following tables show 5 V TTL electrical specifications.

**Table 15 • 5V TTL Electrical Specifications**

Symbol	Parameter	Commercial		Commercial -F		Industrial		Military		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
VOH <sup>1</sup>	IOH = –10 mA	2.4		2.4						V
	IOH = –4 mA					3.7		3.7		V
VOL <sup>1</sup>	IOL = 10 mA		0.5		0.5					V
	IOL = 6 mA					0.4		0.4		V
VIL		–0.3	0.8	–0.3	0.8	–0.3	0.8	–0.3	0.8	V
VIH (40MX)		2.0	VCC + 0.3	2.0	VCC + 0.3	2.0	VCC + 0.3	2.0	VCC + 0.3	V
VIH (42MX) <sup>2</sup>		2.0	VCCI + 0.3	2.0	VCCI + 0.3	2.0	VCCI + 0.3	2.0	VCCI + 0.3	V
IIL	VIN = 0.5 V		–10		–10		–10		–10	μA
IIH	VIN = 2.7 V		–10		–10		–10		–10	μA
Input Transition Time, $T_R$ and $T_F$			500		500		500		500	ns
C <sub>IO</sub> I/O Capacitance			10		10		10		10	pF
Standby Current, ICC <sup>3</sup>	A40MX02, A40MX04		3		25		10		25	mA
	A42MX09		5		25		25		25	mA
	A42MX16		6		25		25		25	mA
	A42MX24, A42MX36		20		25		25		25	mA
Low power mode Standby Current	42MX devices only		0.5		ICC – 5.0		ICC – 5.0		ICC – 5.0	mA
IIO, I/O source sink current	Can be derived from the <i>IBIS model</i> ( <a href="http://www.microsemi.com/soc/techdocs/models/ibis.html">http://www.microsemi.com/soc/techdocs/models/ibis.html</a> )									

1. Only one output tested at a time. VCC/VCCI = min

2. VIH(Min) is 2.4V for A42MX36 family. This applies only to VCCI of 5V and is not applicable to VCCI of 3.3V

3. All outputs unloaded. All inputs = VCC/VCCI or GND

## 3.8 3.3 V Operating Conditions

The following table shows 3.3 V operating conditions.

**Table 16 • Absolute Maximum Ratings for 40MX Devices\***

Symbol	Parameter	Limits	Units
VCC	DC Supply Voltage	−0.5 to +7.0	V
VI	Input Voltage	−0.5 to VCC + 0.5	V
VO	Output Voltage	−0.5 to VCC + 0.5	V
t <sub>STG</sub>	Storage Temperature	−65 to + 150	°C

**Note:** \*Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the recommended operating conditions.

**Table 17 • Absolute Maximum Ratings for 42MX Devices\***

Symbol	Parameter	Limits	Units
VCCI	DC Supply Voltage for I/Os	−0.5 to +7.0	V
VCCA	DC Supply Voltage for Array	−0.5 to +7.0	V
VI	Input Voltage	−0.5 to VCCI+0.5	V
VO	Output Voltage	−0.5 to VCCI+0.5	V
t <sub>STG</sub>	Storage Temperature	−65 to +150	°C

**Note:** \*Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the recommended operating conditions.

**Table 18 • Recommended Operating Conditions**

Parameter	Commercial	Industrial	Military	Units
Temperature Range*	0 to +70	−40 to +85	−55 to +125	°C
VCC (40MX)	3.0 to 3.6	3.0 to 3.6	3.0 to 3.6	V
VCCA (42MX)	3.0 to 3.6	3.0 to 3.6	3.0 to 3.6	V
VCCI (42MX)	3.0 to 3.6	3.0 to 3.6	3.0 to 3.6	V

**Note:** \*Ambient temperature (T<sub>A</sub>) is used for commercial and industrial grades; case temperature (T<sub>C</sub>) is used for military grades.

All the following tables show various specifications and operating conditions of 40MX and 42MX FPGAs.

### 3.9.3 Output Drive Characteristics for 3.3 V PCI Signaling

**Table 25 • DC Specification (3.3 V PCI Signaling)<sup>1</sup>**

Symbol	Parameter	Condition	PCI		MX		Units
			Min.	Max.	Min.	Max.	
VCCI	Supply Voltage for I/Os		3.0	3.6	3.0	3.6 <sup>2</sup>	V
VIH	Input High Voltage		0.5	VCC + 0.5	0.5	VCCI + 0.3	V
VIL	Input Low Voltage		−0.5	0.8	−0.3	0.8	V
IIH	Input High Leakage Current	VIN = 2.7 V		70		10	μA
IIL	Input Leakage Current			−70		−10	μA
VOH	Output High Voltage	IOUT = −2 mA	0.9		3.3		V
VOL	Output Low Voltage	IOUT = 3 mA, 6 mA		0.1		0.1 VCCI	V
CIN	Input Pin Capacitance			10		10	pF
CLK	CLK Pin Capacitance		5	12		10	pF
L <sub>PIN</sub>	Pin Inductance			20		< 8 nH <sup>3</sup>	nH

1. PCI Local Bus Specification, Version 2.1, Section 4.2.2.1.

2. Maximum rating for VCCI −0.5 V to 7.0V.

3. Dependent upon the chosen package. PCI recommends QFP and BGA packaging to reduce pin inductance and capacitance.

**Table 26 • AC Specifications for (3.3 V PCI Signaling)\***

Symbol	Parameter	Condition	PCI		MX		Units
			Min.	Max.	Min.	Max.	
ICL	Low Clamp Current	−5 < VIN ≤ −1	−25 + (VIN + 1) / 0.015		−60	−10	mA
Slew (r)	Output Rise Slew Rate	0.2 V to 0.6 V load	1	4	1.8	2.8	V/ns
Slew (f)	Output Fall Slew Rate	0.6 V to 0.2 V load	1	4	2.8	4.0	V/ns

**Note:** \*PCI Local Bus Specification, Version 2.1, Section 4.2.2.2.

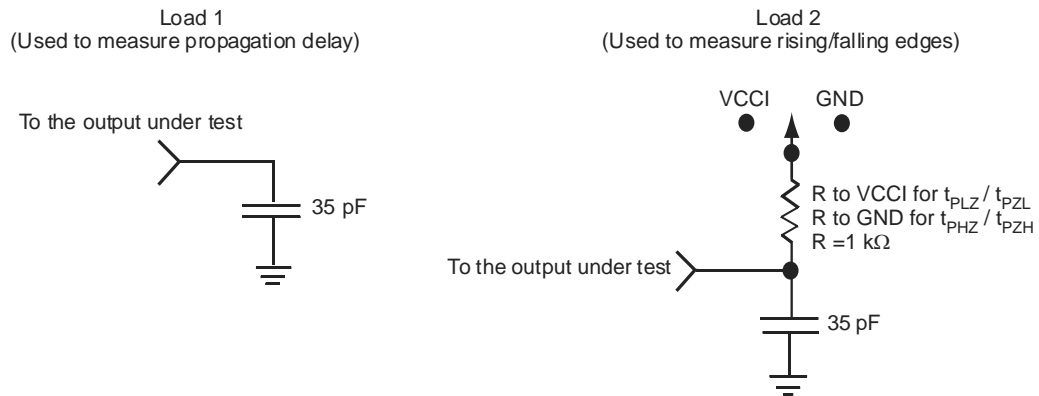
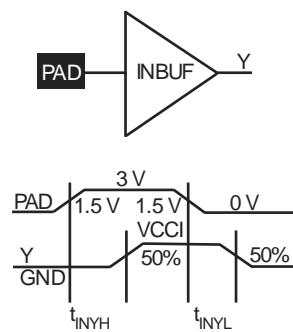
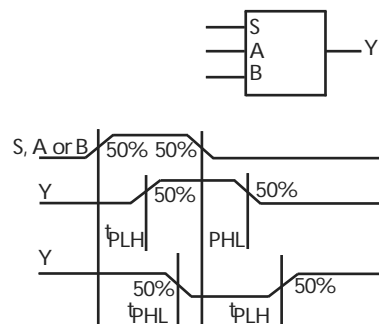
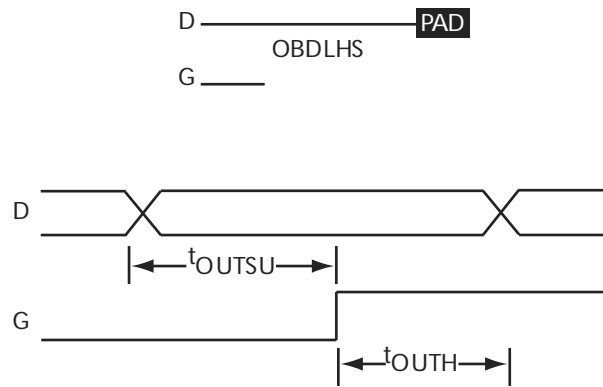
**Figure 22 • AC Test Loads****Figure 23 • Input Buffer Delays****Figure 24 • Module Delays**

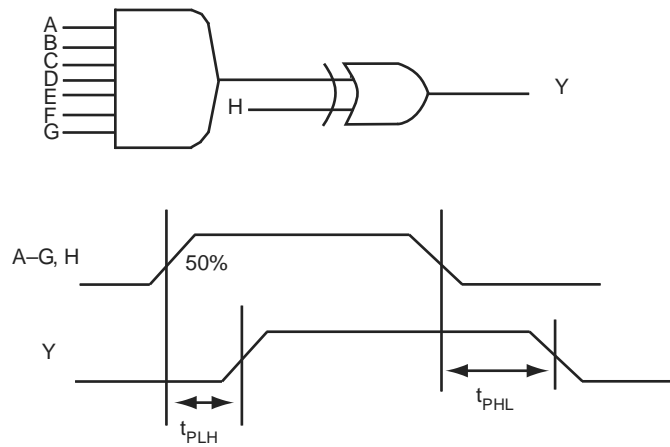
Figure 27 • Output Buffer Latches



3.10.4 Decode Module Timing

The following figure shows decode module timing.

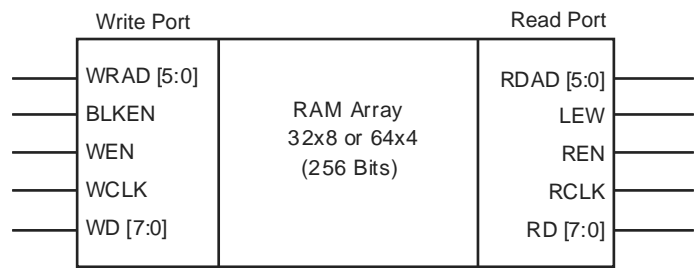
Figure 28 • Decode Module Timing



3.10.5 SRAM Timing Characteristics

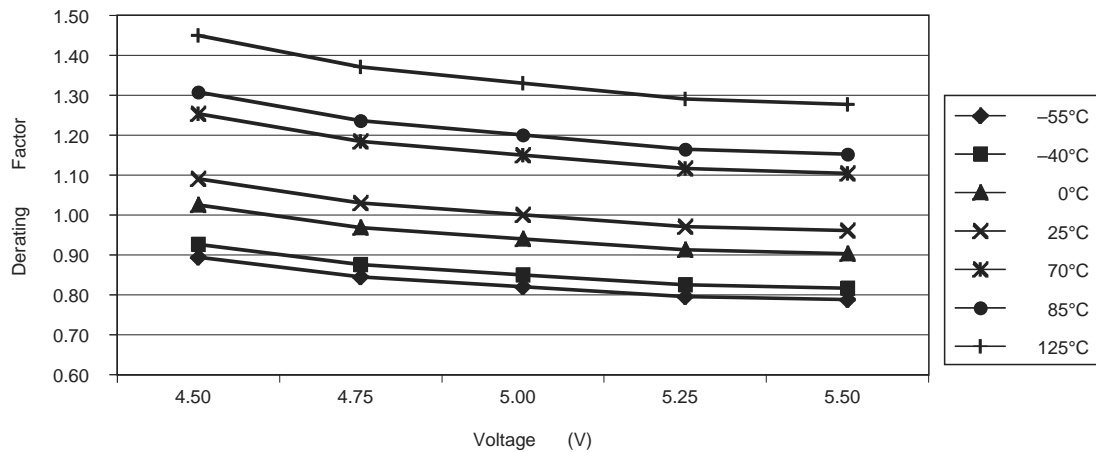
The following figure shows SRAM timing characteristics.

Figure 29 • SRAM Timing Characteristics



3.10.6 Dual-Port SRAM Timing Waveforms

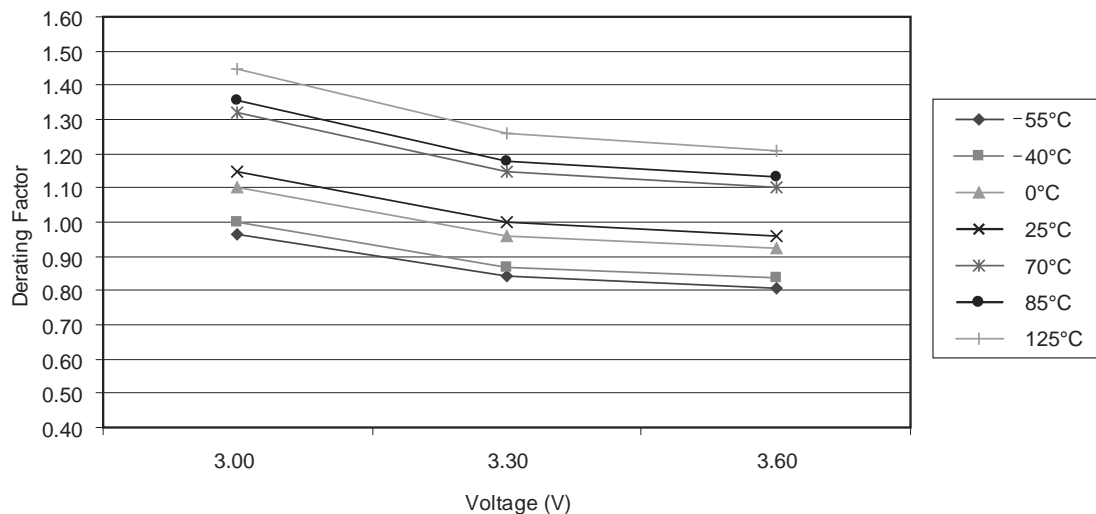
The following figures show dual-port SRAM timing waveforms.

**Figure 35 • 40MX Junction Temperature and Voltage Derating Curves (Normalized to  $T_J = 25^\circ\text{C}$ ,  $V_{CC} = 5.0\text{ V}$ )**

**Note:** This derating factor applies to all routing and propagation delays

**Table 30 • 42MX Temperature and Voltage Derating Factors (Normalized to  $T_J = 25^\circ\text{C}$ ,  $V_{CCA} = 3.3\text{ V}$ )**

42MX Voltage	Temperature						
	-55°C	-40°C	0°C	25°C	70°C	85°C	125°C
3.00	0.97	1.00	1.10	1.15	1.32	1.36	1.45
3.30	0.84	0.87	0.96	1.00	1.15	1.18	1.26
3.60	0.81	0.84	0.92	0.96	1.10	1.13	1.21

**Figure 36 • 42MX Junction Temperature and Voltage Derating Curves (Normalized to  $T_J = 25^\circ\text{C}$ ,  $V_{CCA} = 3.3\text{ V}$ )**

**Note:** This derating factor applies to all routing and propagation delays

**Table 31 • 40MX Temperature and Voltage Derating Factors (Normalized to  $T_J = 25^\circ\text{C}$ ,  $V_{CC} = 3.3\text{ V}$ )**

40MX Voltage	Temperature						
	-55°C	-40°C	0°C	25°C	70°C	85°C	125°C
3.00	1.08	1.12	1.21	1.26	1.50	1.64	2.00
3.30	0.86	0.89	0.96	1.00	1.19	1.30	1.59

**Table 36 • A40MX04 Timing Characteristics (Nominal 5.0 V Operation) (continued)(Worst-Case Commercial Conditions, VCC = 4.75 V, T<sub>J</sub> = 70°C)**

Parameter / Description			–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>HENA</sub>	Flip-Flop (Latch) Enable Hold		0.0		0.0		0.0		0.0		0.0		ns
t <sub>WCLKA</sub>	Flip-Flop (Latch) Clock Active Pulse Width		3.3		3.8		4.3		5.0		7.0		ns
t <sub>WASYN</sub>	Flip-Flop (Latch) Asynchronous Pulse Width		3.3		3.8		4.3		5.0		7.0		ns
t <sub>A</sub>	Flip-Flop Clock Input Period		4.8		5.6		6.3		7.5		10.4		ns
f <sub>MAX</sub>	Flip-Flop (Latch) Clock Frequency (FO = 128)			181		167		154		134		80	MHz
Input Module Propagation Delays													
t <sub>INYH</sub>	Pad-to-Y HIGH			0.7		0.8		0.9		1.1		1.5	ns
t <sub>INYL</sub>	Pad-to-Y LOW			0.6		0.7		0.8		1.0		1.3	ns
Input Module Predicted Routing Delays <sup>1</sup>													
t <sub>IRD1</sub>	FO = 1 Routing Delay			2.1		2.4		2.2		3.2		4.5	ns
t <sub>IRD2</sub>	FO = 2 Routing Delay			2.6		3.0		3.4		4.0		5.6	ns
t <sub>IRD3</sub>	FO = 3 Routing Delay			3.1		3.6		4.1		4.8		6.7	ns
t <sub>IRD4</sub>	FO = 4 Routing Delay			3.6		4.2		4.8		5.6		7.8	ns
t <sub>IRD8</sub>	FO = 8 Routing Delay			5.7		6.6		7.5		8.8		12.4	ns
Global Clock Network													
t <sub>CKH</sub>	Input Low to HIGH	FO = 16		4.6		5.3		6.0		7.0		9.8	ns
		FO = 128		4.6		5.3		6.0		7.0		9.8	
t <sub>CKL</sub>	Input High to LOW	FO = 16		4.8		5.6		6.3		7.4		10.4	ns
		FO = 128		4.8		5.6		6.3		7.4		10.4	
t <sub>PWH</sub>	Minimum Pulse Width HIGH	FO = 16	2.2		2.6		2.9		3.4		4.8		ns
		FO = 128	2.4		2.7		3.1		3.6		5.1		
t <sub>PWL</sub>	Minimum Pulse Width LOW	FO = 16	2.2		2.6		2.9		3.4		4.8		ns
		FO = 128	2.4		2.7		3.01		3.6		5.1		
t <sub>CKSW</sub>	Maximum Skew	FO = 16		0.4		0.5		0.5		0.6		0.8	ns
		FO = 128		0.5		0.6		0.7		0.8		1.2	
t <sub>P</sub>	Minimum Period	FO = 16	4.7		5.4		6.1		7.2		10.0		ns
		FO = 128	4.8		5.6		6.3		7.5		10.4		
f <sub>MAX</sub>	Maximum Frequency	FO = 16		188		175		160		139		83	MHz
		FO = 128		181		168		154		134		80	
TTL Output Module Timing <sup>4</sup>													
t <sub>DLH</sub>	Data-to-Pad HIGH			3.3		3.8		4.3		5.1		7.2	ns
t <sub>DHL</sub>	Data-to-Pad LOW			4.0		4.6		5.2		6.1		8.6	ns
t <sub>ENZH</sub>	Enable Pad Z to HIGH			3.7		4.3		4.9		5.8		8.0	ns
t <sub>ENZL</sub>	Enable Pad Z to LOW			4.7		5.4		6.1		7.2		10.1	ns
t <sub>ENHZ</sub>	Enable Pad HIGH to Z			7.9		9.1		10.4		12.2		17.1	ns

**Table 37 • A40MX04 Timing Characteristics (Nominal 3.3 V Operation) (continued)(Worst-Case Commercial Conditions, VCC = 3.0 V, T<sub>J</sub> = 70°C)**

Parameter / Description			–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Input Module Predicted Routing Delays <sup>1</sup>													
t <sub>IRD1</sub>	FO = 1 Routing Delay		2.9		3.3		3.8		4.5		6.3		ns
t <sub>IRD2</sub>	FO = 2 Routing Delay		3.6		4.2		4.8		5.6		7.8		ns
t <sub>IRD3</sub>	FO = 3 Routing Delay		4.4		5.0		5.7		6.7		9.4		ns
t <sub>IRD4</sub>	FO = 4 Routing Delay		5.1		5.9		6.7		7.8		11.0		ns
t <sub>IRD8</sub>	FO = 8 Routing Delay		8.0		9.3		10.5		12.4		17.2		ns
Global Clock Network													
t <sub>CKH</sub>	Input LOW to HIGH	FO = 16 FO = 128	6.4 6.4		7.4 7.4		8.4 8.4		9.9 9.9		13.8 13.8		ns
t <sub>CKL</sub>	Input HIGH to LOW	FO = 16 FO = 128	6.8 6.8		7.8 7.8		8.9 8.9		10.4 10.4		14.6 14.6		ns
t <sub>PWH</sub>	Minimum Pulse Width HIGH	FO = 16 FO = 128	3.1 3.3		3.6 3.8		4.1 4.3		4.8 5.1		6.7 7.1		ns
t <sub>PWL</sub>	Minimum Pulse Width LOW	FO = 16 FO = 128	3.1 3.3		3.6 3.8		4.1 4.3		4.8 5.1		6.7 7.1		ns
t <sub>CKSW</sub>	Maximum Skew	FO = 16 FO = 128	0.6 0.8		0.6 0.9		0.7 1.0		0.8 1.2		1.2 1.6		ns
t <sub>P</sub>	Minimum Period	FO = 16 FO = 128	6.5 6.8		7.5 7.8		8.5 8.9		10.1 10.4		14.1 14.6		ns
f <sub>MAX</sub>	Maximum Frequency	FO = 16 FO = 128	113 109		105 101		96 92		83 80		50 48		MHz
TTL Output Module Timing <sup>4</sup>													
t <sub>DLH</sub>	Data-to-Pad HIGH		4.7		5.4		6.1		7.2		10.0		ns
t <sub>DHL</sub>	Data-to-Pad LOW		5.6		6.4		7.3		8.6		12.0		ns
t <sub>ENZH</sub>	Enable Pad Z to HIGH		5.2		6.0		6.9		8.1		11.3		ns
t <sub>ENZL</sub>	Enable Pad Z to LOW		6.6		7.6		8.6		10.1		14.1		ns
t <sub>ENHZ</sub>	Enable Pad HIGH to Z		11.1		12.8		14.5		17.1		23.9		ns
t <sub>ENLZ</sub>	Enable Pad LOW to Z		8.2		9.5		10.7		12.6		17.7		ns
d <sub>TLH</sub>	Delta LOW to HIGH		0.03		0.03		0.04		0.04		0.06		ns/pF
d <sub>THL</sub>	Delta HIGH to LOW		0.04		0.04		0.05		0.06		0.08		ns/pF

**Table 44 • A42MX36 Timing Characteristics (Nominal 5.0 V Operation)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T<sub>J</sub> = 70°C)**

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
TTL Output Module Timing <sup>5</sup> (Continued)												
t <sub>ENLZ</sub>	Enable Pad LOW to Z		4.9		5.5		6.2		7.3		10.2	ns
t <sub>GLH</sub>	G-to-Pad HIGH		2.9		3.3		3.7		4.4		6.1	ns
t <sub>GHL</sub>	G-to-Pad LOW		2.9		3.3		3.7		4.4		6.1	ns
t <sub>LSU</sub>	I/O Latch Output Set-Up	0.5		0.5		0.6		0.7		1.0		ns
t <sub>LH</sub>	I/O Latch Output Hold	0.0		0.0		0.0		0.0		0.0		ns
t <sub>LCO</sub>	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		5.7		6.3		7.1		8.4		11.8	ns
t <sub>ACO</sub>	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O		7.8		8.6		9.8		11.5		16.1	ns
d <sub>TLH</sub>	Capacitive Loading, LOW to HIGH		0.07		0.08		0.09		0.10		0.14	ns/pF
d <sub>THL</sub>	Capacitive Loading, HIGH to LOW		0.07		0.08		0.09		0.10		0.14	ns/pF

**Table 53 • PQ208**

<b>PQ208</b>			
<b>Pin Number</b>	<b>A42MX16 Function</b>	<b>A42MX24 Function</b>	<b>A42MX36 Function</b>
21	I/O	I/O	I/O
22	GND	GND	GND
23	I/O	I/O	I/O
24	I/O	I/O	I/O
25	I/O	I/O	I/O
26	I/O	I/O	I/O
27	GND	GND	GND
28	VCCI	VCCI	VCCI
29	VCCA	VCCA	VCCA
30	I/O	I/O	I/O
31	I/O	I/O	I/O
32	VCCA	VCCA	VCCA
33	I/O	I/O	I/O
34	I/O	I/O	I/O
35	I/O	I/O	I/O
36	I/O	I/O	I/O
37	I/O	I/O	I/O
38	I/O	I/O	I/O
39	I/O	I/O	I/O
40	I/O	I/O	I/O
41	NC	I/O	I/O
42	NC	I/O	I/O
43	NC	I/O	I/O
44	I/O	I/O	I/O
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	I/O	I/O	I/O
48	I/O	I/O	I/O
49	I/O	I/O	I/O
50	NC	I/O	I/O
51	NC	I/O	I/O
52	GND	GND	GND
53	GND	GND	GND
54	I/O	TMS, I/O	TMS, I/O
55	I/O	TDI, I/O	TDI, I/O
56	I/O	I/O	I/O
57	I/O	WD, I/O	WD, I/O

**Table 54 • PQ240**

<b>PQ240</b>	
<b>Pin Number</b>	<b>A42MX36 Function</b>
15	QCLKC, I/O
16	I/O
17	WD, I/O
18	WD, I/O
19	I/O
20	I/O
21	WD, I/O
22	WD, I/O
23	I/O
24	PRB, I/O
25	I/O
26	CLKB, I/O
27	I/O
28	GND
29	VCCA
30	VCCI
31	I/O
32	CLKA, I/O
33	I/O
34	PRA, I/O
35	I/O
36	I/O
37	WD, I/O
38	WD, I/O
39	I/O
40	I/O
41	I/O
42	I/O
43	I/O
44	I/O
45	QCLKD, I/O
46	I/O
47	WD, I/O
48	WD, I/O
49	I/O
50	I/O
51	I/O

**Table 54 • PQ240**

<b>PQ240</b>	
<b>Pin Number</b>	<b>A42MX36 Function</b>
52	VCCI
53	I/O
54	WD, I/O
55	WD, I/O
56	I/O
57	SDI, I/O
58	I/O
59	VCCA
60	GND
61	GND
62	I/O
63	I/O
64	I/O
65	I/O
66	I/O
67	I/O
68	I/O
69	I/O
70	I/O
71	VCCI
72	I/O
73	I/O
74	I/O
75	I/O
76	I/O
77	I/O
78	I/O
79	I/O
80	I/O
81	I/O
82	I/O
83	I/O
84	I/O
85	VCCA
86	I/O
87	I/O
88	VCCA

Table 54 • PQ240

PQ240	
Pin Number	A42MX36 Function
237	GND
238	MODE
239	VCCA
240	GND

Figure 46 • VQ80

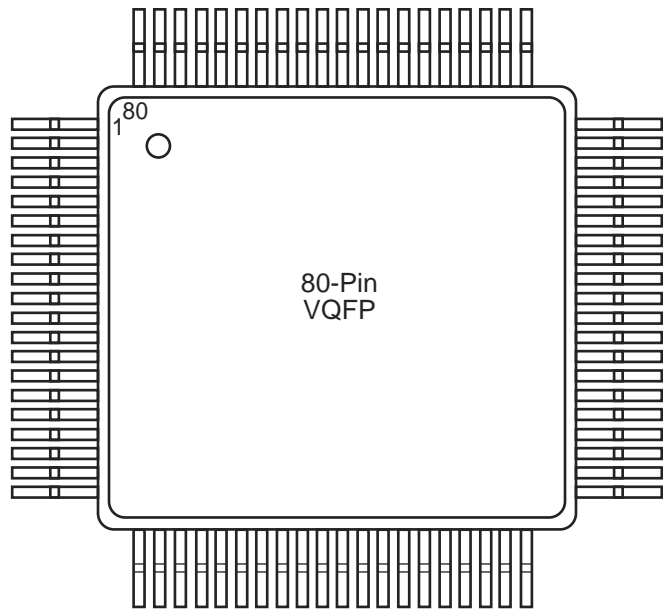


Table 55 • VQ80

VQ80		
Pin Number	A40MX02 Function	A40MX04 Function
1	I/O	I/O
2	NC	I/O
3	NC	I/O
4	NC	I/O
5	I/O	I/O
6	I/O	I/O
7	GND	GND
8	I/O	I/O
9	I/O	I/O
10	I/O	I/O
11	I/O	I/O
12	I/O	I/O

**Table 59 • CQ256**

<b>CQ256</b>	
<b>Pin Number</b>	<b>A42MX36 Function</b>
133	I/O
134	I/O
135	I/O
136	I/O
137	I/O
138	I/O
139	GND
140	I/O
141	I/O
142	I/O
143	I/O
144	I/O
145	I/O
146	I/O
147	I/O
148	I/O
149	I/O
150	I/O
151	I/O
152	I/O
153	I/O
154	I/O
155	VCCA
156	I/O
157	I/O
158	VCCA
159	VCCI
160	GND
161	I/O
162	I/O
163	I/O
164	I/O
165	GND
166	I/O
167	I/O
168	I/O
169	I/O

Table 59 • CQ256

CQ256	
Pin Number	A42MX36 Function
244	WD, I/O
245	I/O
246	I/O
247	I/O
248	VCCI
249	I/O
250	WD, I/O
251	WD, I/O
252	I/O
253	SDI, I/O
254	I/O
255	GND
256	NC

Figure 51 • BG272

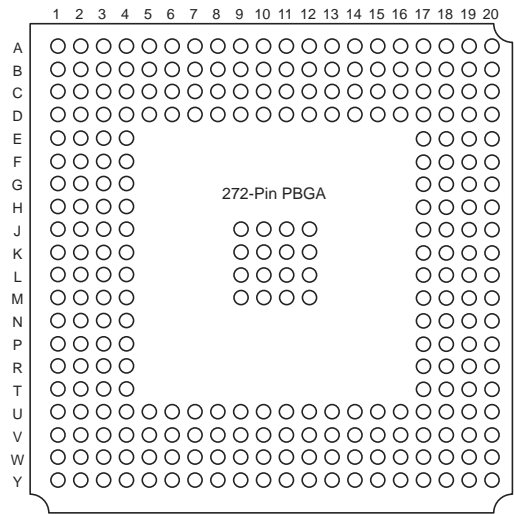


Table 60 • BG272

BG272	
Pin Number	A42MX36 Function
A1	GND
A2	GND
A3	I/O
A4	WD, I/O
A5	I/O

**Table 61 • PG132**

<b>PG132</b>	
<b>Pin Number</b>	<b>A42MX09 Function</b>
N10	I/O
M10	I/O
N11	I/O
L10	I/O
M11	I/O
N12	SDO
M12	I/O
L11	I/O
N13	I/O
M13	I/O
K11	I/O
L12	I/O
L13	I/O
K13	I/O
H10	I/O
J12	I/O
J13	I/O
H11	I/O
H12	I/O
H13	VKS
G13	VPP