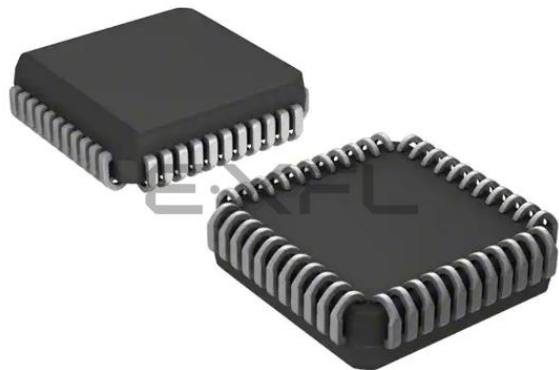




Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	34
Number of Gates	3000
Voltage - Supply	3V ~ 3.6V, 4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TC)
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a40mx02-1pl44m



Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Fax: +1 (949) 215-4996
Email: sales.support@microsemi.com
www.microsemi.com

© 2016 Microsemi Corporation. All rights reserved. Microsemi and the Microsemi logo are trademarks of Microsemi Corporation. All other trademarks and service marks are the property of their respective owners.

Microsemi makes no warranty, representation, or guarantee regarding the information contained herein or the suitability of its products and services for any particular purpose, nor does Microsemi assume any liability whatsoever arising out of the application or use of any product or circuit. The products sold hereunder and any other products sold by Microsemi have been subject to limited testing and should not be used in conjunction with mission-critical equipment or applications. Any performance specifications are believed to be reliable but are not verified, and Buyer must conduct and complete all performance and other testing of the products, alone and together with, or installed in, any end-products. Buyer shall not rely on any data and performance specifications or parameters provided by Microsemi. It is the Buyer's responsibility to independently determine suitability of any products and to test and verify the same. The information provided by Microsemi hereunder is provided "as is, where is" and with all faults, and the entire risk associated with such information is entirely with the Buyer. Microsemi does not grant, explicitly or implicitly, to any party any patent rights, licenses, or any other IP rights, whether with regard to such information itself or anything described by such information. Information provided in this document is proprietary to Microsemi, and Microsemi reserves the right to make any changes to the information in this document or to any products and services at any time without notice.

About Microsemi

Microsemi Corporation (Nasdaq: MSCC) offers a comprehensive portfolio of semiconductor and system solutions for aerospace & defense, communications, data center and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; enterprise storage and communication solutions, security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, California, and has approximately 4,800 employees globally. Learn more at www.microsemi.com.

3.4.11	Boundary Scan Description Language (BSDL) File	19
3.5	Development Tool Support	19
3.6	Related Documents	20
3.6.1	Application Notes	20
3.6.2	User Guides and Manuals	20
3.6.3	Miscellaneous	20
3.7	5.0 V Operating Conditions	20
3.7.1	5 V TTL Electrical Specifications	21
3.8	3.3 V Operating Conditions	22
3.8.1	3.3 V LVTTTL Electrical Specifications	23
3.9	Mixed 5.0 V / 3.3 V Operating Conditions (for 42MX Devices Only)	23
3.9.1	Mixed 5.0V/3.3V Electrical Specifications	25
3.9.2	Output Drive Characteristics for 5.0 V PCI Signaling	25
3.9.3	Output Drive Characteristics for 3.3 V PCI Signaling	27
3.9.4	Junction Temperature (T_J)	28
3.9.5	Package Thermal Characteristics	28
3.10	Timing Models	30
3.10.1	Parameter Measurement	32
3.10.2	Sequential Module Timing Characteristics	34
3.10.3	Sequential Timing Characteristics	34
3.10.4	Decode Module Timing	35
3.10.5	SRAM Timing Characteristics	35
3.10.6	Dual-Port SRAM Timing Waveforms	35
3.10.7	Predictable Performance: Tight Delay Distributions	37
3.11	Timing Characteristics	37
3.11.1	Critical Nets and Typical Nets	37
3.11.2	Long Tracks	37
3.11.3	Timing Derating	38
3.11.4	Temperature and Voltage Derating Factors	38
3.11.5	PCI System Timing Specification	40
3.11.6	PCI Models	40
3.12	Pin Descriptions	83
4	Package Pin Assignments	86

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 15.0

The following is a summary of the changes in revision 15.0 of this document.

- [Table 15](#), page 21 is edited to add the footnote, VIH(Min) is 2.4V for A42MX36 family. This applies only to VCCI of 5V and is not applicable to VCCI of 3.3V
- [Table 22](#), page 25 is edited to add the footnote, VIH(Min) is 2.4V for A42MX36 family. This applies only to VCCI of 5V and is not applicable to VCCI of 3.3V
- [Table 23](#), page 25 is edited to add the footnote, VIH(Min) is 2.4V for A42MX36 family. This applies only to VCCI of 5V and is not applicable to VCCI of 3.3V

1.2 Revision 14.0

The following is a summary of the changes in revision 14.0 of this document.

- Added CQFP package information for A42MX16 device in [Product Profile](#), page 1 and [Ceramic Device Resources](#), page 4 (SAR 79522).
- Added Military (M) and MIL-STD-883 Class B (B) grades for CPGA 132 Package and added Commercial (C), Military (M), and MIL-STD-883 Class B (B) grades for CQFP 172 Package in [Temperature Grade Offerings](#), page 5 (SAR 79519)
- Changed Silicon Sculptor II to Silicon Sculptor in [Programming](#), page 12 (SAR 38754)
- Added [Figure 53](#), page 158 CQ172 package (SAR 79522).

1.3 Revision 13.0

The following is a summary of the changes in revision 13.0 of this document.

- Added [Figure 42](#), page 97 PQ144 Package for A42MX09 device (SAR 69776)
- Added [Figure 52](#), page 153 PQ132 Package for A42MX09 device (SAR 69776)

1.4 Revision 12.0

The following is a summary of the changes in revision 12.0 of this document.

- Added information on power-up behavior for A42MX24 and A42MX36 devices to the [Power Supply](#), page 13 (SAR 42096)
- Corrected the inadvertent mistake in the naming of the PL68 pin assignment table (SARs 48999, 49793)

1.5 Revision 11.0

The following is a summary of the changes in revision 11.0 of this document.

- The FuseLock logo and accompanying text was removed from the [User Security](#), page 12. This marking is no longer used on Microsemi devices ([PCN 0915](#))
- The [Development Tool Support](#), page 19 was updated (SAR 38512)

1.6 Revision 10.0

The following is a summary of the changes in revision 10.0 of this document.

- [Ordering Information](#), page 3 was updated to include lead-free package ordering codes (SAR 21968)
- The [User Security](#), page 12 was revised to clarify that although no existing security measures can give an absolute guarantee, Microsemi FPGAs implement the best security available in the industry (SAR 34673)

Table 35 • A40MX02 Timing Characteristics (Nominal 3.3 V Operation) (continued)
 (Worst-Case Commercial Conditions, VCC = 3.0 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
CMOS Output Module Timing ⁴												
t _{DLH}	Data-to-Pad HIGH		5.5		6.4		7.2		8.5		11.9	ns
t _{DHL}	Data-to-Pad LOW		4.8		5.5		6.2		7.3		10.2	ns
t _{ENZH}	Enable Pad Z to HIGH		4.7		5.5		6.2		7.3		10.2	ns
t _{ENZL}	Enable Pad Z to LOW		6.8		7.9		8.9		10.5		14.7	ns
t _{ENHZ}	Enable Pad HIGH to Z		11.1		12.8		14.5		17.1		23.9	ns
t _{ENLZ}	Enable Pad LOW to Z		8.2		9.5		10.7		12.6		17.7	ns
d _{TLH}	Delta LOW to HIGH		0.05		0.05		0.06		0.07		0.10	ns/pF
d _{THL}	Delta HIGH to LOW		0.03		0.03		0.04		0.04		0.06	ns/pF

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
2. Set-up times assume fanout of 3. Further testing information can be obtained from the Timer utility.
3. The hold time for the DFME1A macro may be greater than 0 ns. Use the Timer tool from the Designer software to check the hold time for this macro
4. Delays based on 35 pF loading

Table 36 • A40MX04 Timing Characteristics (Nominal 5.0 V Operation) (Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C)

Parameter / Description		-3 Speed		-2 Speed		-1 Speed		Std Speed		-F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Logic Module Propagation Delays												
t _{PD1}	Single Module		1.2		1.4		1.6		1.9		2.7	ns
t _{PD2}	Dual-Module Macros		2.3		3.1		3.5		4.1		5.7	ns
t _{CO}	Sequential Clock-to-Q		1.2		1.4		1.6		1.9		2.7	ns
t _{GO}	Latch G-to-Q		1.2		1.4		1.6		1.9		2.7	ns
t _{RS}	Flip-Flop (Latch) Reset-to-Q		1.2		1.4		1.6		1.9		2.7	ns
Logic Module Predicted Routing Delays ¹												
t _{RD1}	FO = 1 Routing Delay		1.2		1.6		1.8		2.1		3.0	ns
t _{RD2}	FO = 2 Routing Delay		1.9		2.2		2.5		2.9		4.1	ns
t _{RD3}	FO = 3 Routing Delay		2.4		2.8		3.2		3.7		5.2	ns
t _{RD4}	FO = 4 Routing Delay		2.9		3.4		3.9		4.5		6.3	ns
t _{RD8}	FO = 8 Routing Delay		5.0		5.8		6.6		7.8		10.9	ns
Logic Module Sequential Timing ²												
t _{SUD}	Flip-Flop (Latch) Data Input Set-Up		3.1		3.5		4.0		4.7		6.6	ns
t _{HD} ³	Flip-Flop (Latch) Data Input Hold		0.0		0.0		0.0		0.0		0.0	ns
t _{SUENA}	Flip-Flop (Latch) Enable Set-Up		3.1		3.5		4.0		4.7		6.6	ns

Table 38 • A42MX09 Timing Characteristics (Nominal 5.0 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	4.5		4.9		5.6		6.6		9.2		ns
t _A	Flip-Flop Clock Input Period	3.5		3.8		4.3		5.1		7.1		ns
t _{INH}	Input Buffer Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{INSU}	Input Buffer Latch Set-Up	0.3		0.3		0.4		0.4		0.6		ns
t _{OUTH}	Output Buffer Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{OUTSU}	Output Buffer Latch Set-Up	0.3		0.3		0.4		0.4		0.6		ns
f _{MAX}	Flip-Flop (Latch) Clock Frequency		268		244		224		195		117	MHz

Table 39 • A42MX09 Timing Characteristics (Nominal 3.3 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)

Parameter / Description		-3 Speed		-2 Speed		-1 Speed		Std Speed		-F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{RD4}	FO = 4 Routing Delay	1.9		2.1		2.4		2.9		4.0		ns
t _{RD8}	FO = 8 Routing Delay	3.2		3.6		4.1		4.8		6.7		ns
Logic Module Sequential Timing ^{3, 4}												
t _{SUD}	Flip-Flop (Latch) Data Input Set-Up	0.5		0.5		0.6		0.7		0.9		ns
t _{HD}	Flip-Flop (Latch) Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{SUENA}	Flip-Flop (Latch) Enable Set-Up	0.6		0.6		0.7		0.8		1.2		ns
t _{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	4.7		5.3		6.0		7.0		9.8		ns
t _{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	6.2		6.9		7.8		9.2		12.9		ns
t _A	Flip-Flop Clock Input Period	5.0		5.6		6.2		7.1		9.9		ns
t _{INH}	Input Buffer Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{INSU}	Input Buffer Latch Set-Up	0.3		0.3		0.3		0.4		0.6		ns
t _{OUTH}	Output Buffer Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{OUTSU}	Output Buffer Latch Set-Up	0.3		0.3		0.3		0.4		0.6		ns
f _{MAX}	Flip-Flop (Latch) Clock Frequency	161		146		135		117		70		MHz

Table 42 • A42MX24 Timing Characteristics (Nominal 5.0 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
CMOS Output Module Timing ⁵												
t _{DLH}	Data-to-Pad HIGH		3.1		3.5		3.9		4.6		6.4	ns
t _{DHL}	Data-to-Pad LOW		2.4		2.6		3.0		3.5		4.9	ns
t _{ENZH}	Enable Pad Z to HIGH		2.5		2.8		3.2		3.8		5.3	ns
t _{ENZL}	Enable Pad Z to LOW		2.8		3.1		3.5		4.2		5.8	ns
t _{ENHZ}	Enable Pad HIGH to Z		5.2		5.7		6.5		7.6		10.7	ns
t _{ENLZ}	Enable Pad LOW to Z		4.8		5.3		6.0		7.1		9.9	ns
t _{GLH}	G-to-Pad HIGH		4.9		5.4		6.2		7.2		10.1	ns
t _{GHL}	G-to-Pad LOW		4.9		5.4		6.2		7.2		10.1	ns
t _{LSU}	I/O Latch Set-Up	0.5		0.5		0.6		0.7		1.0		ns
t _{LH}	I/O Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		5.5		6.1		6.9		8.1		11.3	ns
t _{ACO}	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O		10.6		11.8		13.4		15.7		22.0	ns
d _{TLH}	Capacitive Loading, LOW to HIGH		0.04		0.04		0.04		0.05		0.07	ns/pF
d _{THL}	Capacitive Loading, HIGH to LOW		0.03		0.03		0.03		0.04		0.06	ns/pF

1. For dual-module macros, use t_{PD1} + t_{RD1} + t_{PDn}, t_{CO} + t_{RD1} + t_{PDn}, or t_{PD1} + t_{RD1} + t_{SUD}, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
4. Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.
5. Delays based on 35 pF loading

Table 43 • A42MX24 Timing Characteristics (Nominal 3.3 V Operation) (Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)

Parameter / Description		-3 Speed		-2 Speed		-1 Speed		Std Speed		-F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Logic Module Combinatorial Functions ¹												
t _{PD}	Internal Array Module Delay		2.0		1.8		2.1		2.5		3.4	ns
t _{PDD}	Internal Decode Module Delay		1.1		2.2		2.5		3.0		4.2	ns
Logic Module Predicted Routing Delays ²												
t _{RD1}	FO = 1 Routing Delay		1.7		1.3		1.4		1.7		2.3	ns
t _{RD2}	FO = 2 Routing Delay		2.0		1.6		1.8		2.1		3.0	ns
t _{RD3}	FO = 3 Routing Delay		1.1		2.0		2.2		2.6		3.7	ns
t _{RD4}	FO = 4 Routing Delay		1.5		2.3		2.6		3.1		4.3	ns
t _{RD5}	FO = 8 Routing Delay		1.8		3.7		4.2		5.0		7.0	ns

Table 44 • A42MX36 Timing Characteristics (Nominal 5.0 V Operation)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description		-3 Speed		-2 Speed		-1 Speed		Std Speed		-F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Logic Module Combinatorial Functions ¹												
t _{PD}	Internal Array Module Delay	1.3		1.5		1.7		2.0		2.7		ns
t _{PDD}	Internal Decode Module Delay	1.6		1.8		2.0		2.4		3.3		ns
Logic Module Predicted Routing Delays ²												
t _{RD1}	FO = 1 Routing Delay	0.9		1.0		1.2		1.4		2.0		ns
t _{RD2}	FO = 2 Routing Delay	1.3		1.4		1.6		1.9		2.7		ns
t _{RD3}	FO =3 Routing Delay	1.6		1.8		2.0		2.4		3.4		ns
t _{RD4}	FO = 4 Routing Delay	2.0		2.2		2.5		2.9		4.1		ns
t _{RD5}	FO = 8 Routing Delay	3.3		3.7		4.2		4.9		6.9		ns
t _{RDD}	Decode-to-Output Routing Delay	0.3		0.4		0.4		0.5		0.7		ns
Logic Module Sequential Timing ^{3, 4}												
t _{CO}	Flip-Flop Clock-to-Output	1.3		1.4		1.6		1.9		2.7		ns
t _{GO}	Latch Gate-to-Output	1.3		1.4		1.6		1.9		2.7		ns
t _{SUD}	Flip-Flop (Latch) Set-Up Time	0.3		0.3		0.4		0.5		0.7		ns
t _{HD}	Flip-Flop (Latch) Hold Time	0.0		0.0		0.0		0.0		0.0		ns
t _{RO}	Flip-Flop (Latch) Reset-to-Output	1.6		1.7		2.0		2.3		3.2		ns
t _{SUENA}	Flip-Flop (Latch) Enable Set-Up	0.7		0.8		0.9		1.0		1.4		ns
t _{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	3.3		3.7		4.2		4.9		6.9		ns
t _{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	4.4		4.8		5.5		6.4		9.0		ns
Synchronous SRAM Operations												
t _{RC}	Read Cycle Time	6.8		7.5		8.5		10.0		14.0		ns
t _{WC}	Write Cycle Time	6.8		7.5		8.5		10.0		14.0		ns
t _{RCKHL}	Clock HIGH/LOW Time	3.4		3.8		4.3		5.0		7.0		ns
t _{RCO}	Data Valid After Clock HIGH/LOW	3.4		3.8		4.3		5.0		7.0		ns
t _{ADSU}	Address/Data Set-Up Time	1.6		1.8		2.0		2.4		3.4		ns
Synchronous SRAM Operations (continued)												
t _{ADH}	Address/Data Hold Time	0.0		0.0		0.0		0.0		0.0		ns
t _{RENSU}	Read Enable Set-Up	0.6		0.7		0.8		0.9		1.3		ns
t _{RENH}	Read Enable Hold	3.4		3.8		4.3		5.0		7.0		ns
t _{WENSU}	Write Enable Set-Up	2.7		3.0		3.4		4.0		5.6		ns
t _{WENH}	Write Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{BENS}	Block Enable Set-Up	2.8		3.1		3.5		4.1		5.7		ns
t _{BENH}	Block Enable Hold	0.0		0.0		0.0		0.0		0.0		ns

Table 44 • A42MX36 Timing Characteristics (Nominal 5.0 V Operation)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

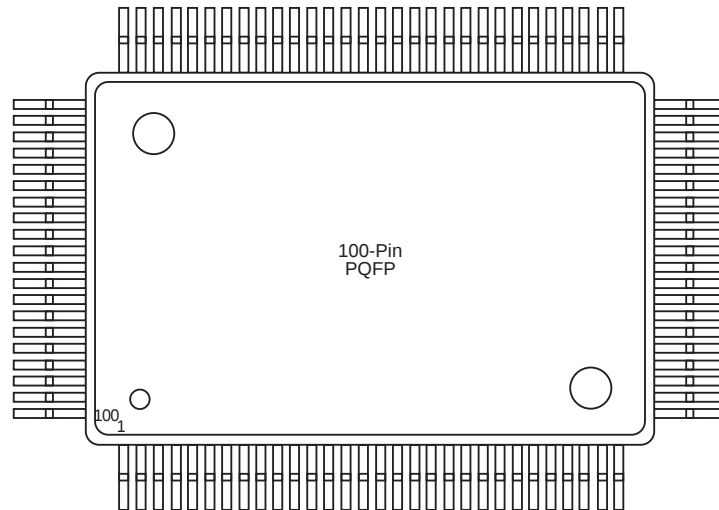
Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
TTL Output Module Timing ⁵ (Continued)												
t _{ENLZ}	Enable Pad LOW to Z		4.9		5.5		6.2		7.3		10.2	ns
t _{GLH}	G-to-Pad HIGH		2.9		3.3		3.7		4.4		6.1	ns
t _{GHL}	G-to-Pad LOW		2.9		3.3		3.7		4.4		6.1	ns
t _{LSU}	I/O Latch Output Set-Up	0.5		0.5		0.6		0.7		1.0		ns
t _{LH}	I/O Latch Output Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		5.7		6.3		7.1		8.4		11.8	ns
t _{ACO}	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O		7.8		8.6		9.8		11.5		16.1	ns
d _{TLH}	Capacitive Loading, LOW to HIGH		0.07		0.08		0.09		0.10		0.14	ns/pF
d _{THL}	Capacitive Loading, HIGH to LOW		0.07		0.08		0.09		0.10		0.14	ns/pF

Table 48 • PL68

PL68		
Pin Number	A40MX02 Function	A40MX04 Function
24	I/O	I/O
25	VCC	VCC
26	I/O	I/O
27	I/O	I/O
28	I/O	I/O
29	I/O	I/O
30	I/O	I/O
31	I/O	I/O
32	GND	GND
33	I/O	I/O
34	I/O	I/O
35	I/O	I/O
36	I/O	I/O
37	I/O	I/O
38	VCC	VCC
39	I/O	I/O
40	I/O	I/O
41	I/O	I/O
42	I/O	I/O
43	I/O	I/O
44	I/O	I/O
45	I/O	I/O
46	I/O	I/O
47	I/O	I/O
48	I/O	I/O
49	GND	GND
50	I/O	I/O
51	I/O	I/O
52	CLK, I/O	CLK, I/O
53	I/O	I/O
54	MODE	MODE
55	VCC	VCC
56	SDI, I/O	SDI, I/O
57	DCLK, I/O	DCLK, I/O
58	PRA, I/O	PRA, I/O
59	PRB, I/O	PRB, I/O
60	I/O	I/O

Table 49 • PL84

PL84				
Pin Number	A40MX04 Function	A42MX09 Function	A42MX16 Function	A42MX24 Function
84	I/O	VCCA	VCCA	VCCA

Figure 41 • PQ100**Table 50 • PQ 100**

PQ100				
Pin Number	A40MX02 Function	A40MX04 Function	A42MX09 Function	A42MX16 Function
1	NC	NC	I/O	I/O
2	NC	NC	DCLK, I/O	DCLK, I/O
3	NC	NC	I/O	I/O
4	NC	NC	MODE	MODE
5	NC	NC	I/O	I/O
6	PRB, I/O	PRB, I/O	I/O	I/O
7	I/O	I/O	I/O	I/O
8	I/O	I/O	I/O	I/O
9	I/O	I/O	GND	GND
10	I/O	I/O	I/O	I/O
11	I/O	I/O	I/O	I/O
12	I/O	I/O	I/O	I/O
13	GND	GND	I/O	I/O
14	I/O	I/O	I/O	I/O
15	I/O	I/O	I/O	I/O
16	I/O	I/O	VCCA	VCCA
17	I/O	I/O	VCCI	VCCA
18	I/O	I/O	I/O	I/O

Table 51 • PQ144

PQ144	
Pin Number	A42MX09 Function
117	GNDI
118	NC
119	I/O
120	I/O
121	I/O
122	I/O
123	PROBA
124	I/O
125	CLKA
126	VCC
127	VCCI
128	NC
129	I/O
130	CLKB
131	I/O
132	PROBB
133	I/O
134	I/O
135	I/O
136	GND
137	GNDI
138	NC
139	I/O
140	I/O
141	I/O
142	I/O
143	I/O
144	DCLK

Table 52 • PQ160

PQ160			
Pin Number	A42MX09 Function	A42MX16 Function	A42MX24 Function
132	I/O	I/O	I/O
133	I/O	I/O	I/O
134	I/O	I/O	I/O
135	NC	VCCA	VCCA
136	I/O	I/O	I/O
137	I/O	I/O	I/O
138	NC	VCCA	VCCA
139	VCCI	VCCI	VCCI
140	GND	GND	GND
141	NC	I/O	I/O
142	I/O	I/O	I/O
143	I/O	I/O	I/O
144	I/O	I/O	I/O
145	GND	GND	GND
146	NC	I/O	I/O
147	I/O	I/O	I/O
148	I/O	I/O	I/O
149	I/O	I/O	I/O
150	NC	VCCA	VCCA
151	NC	I/O	I/O
152	NC	I/O	I/O
153	NC	I/O	I/O
154	NC	I/O	I/O
155	GND	GND	GND
156	I/O	I/O	I/O
157	I/O	I/O	I/O
158	I/O	I/O	I/O
159	MODE	MODE	MODE
160	GND	GND	GND

Table 53 • PQ208

PQ208			
Pin Number	A42MX16 Function	A42MX24 Function	A42MX36 Function
58	I/O	WD, I/O	WD, I/O
59	I/O	I/O	I/O
60	VCCI	VCCI	VCCI
61	NC	I/O	I/O
62	NC	I/O	I/O
63	I/O	I/O	I/O
64	I/O	I/O	I/O
65	I/O	I/O	QCLKA, I/O
66	I/O	WD, I/O	WD, I/O
67	NC	WD, I/O	WD, I/O
68	NC	I/O	I/O
69	I/O	I/O	I/O
70	I/O	WD, I/O	WD, I/O
71	I/O	WD, I/O	WD, I/O
72	I/O	I/O	I/O
73	I/O	I/O	I/O
74	I/O	I/O	I/O
75	I/O	I/O	I/O
76	I/O	I/O	I/O
77	I/O	I/O	I/O
78	GND	GND	GND
79	VCCA	VCCA	VCCA
80	NC	VCCI	VCCI
81	I/O	I/O	I/O
82	I/O	I/O	I/O
83	I/O	I/O	I/O
84	I/O	I/O	I/O
85	I/O	WD, I/O	WD, I/O
86	I/O	WD, I/O	WD, I/O
87	I/O	I/O	I/O
88	I/O	I/O	I/O
89	NC	I/O	I/O
90	NC	I/O	I/O
91	I/O	I/O	QCLKB, I/O
92	I/O	I/O	I/O
93	I/O	WD, I/O	WD, I/O
94	I/O	WD, I/O	WD, I/O

Table 54 • PQ240

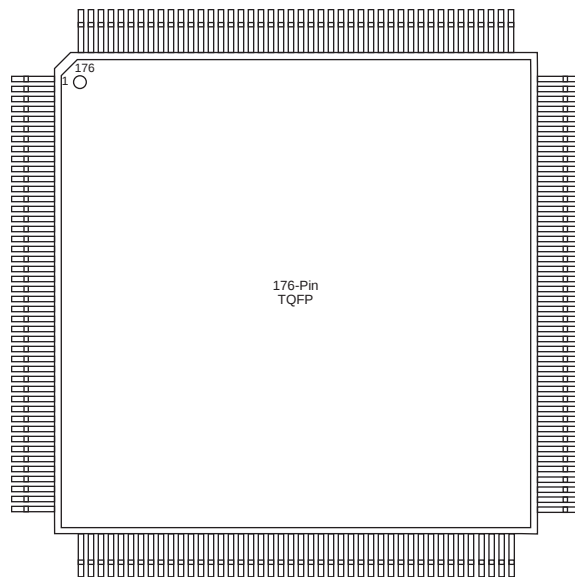
PQ240	
Pin Number	A42MX36 Function
15	QCLKC, I/O
16	I/O
17	WD, I/O
18	WD, I/O
19	I/O
20	I/O
21	WD, I/O
22	WD, I/O
23	I/O
24	PRB, I/O
25	I/O
26	CLKB, I/O
27	I/O
28	GND
29	VCCA
30	VCCI
31	I/O
32	CLKA, I/O
33	I/O
34	PRA, I/O
35	I/O
36	I/O
37	WD, I/O
38	WD, I/O
39	I/O
40	I/O
41	I/O
42	I/O
43	I/O
44	I/O
45	QCLKD, I/O
46	I/O
47	WD, I/O
48	WD, I/O
49	I/O
50	I/O
51	I/O

Table 56 • VQ100

VQ100		
Pin Number	A42MX09 Function	A42MX16 Function
21	I/O	I/O
22	I/O	I/O
23	I/O	I/O
24	I/O	I/O
25	I/O	I/O
26	I/O	I/O
27	I/O	I/O
28	I/O	I/O
29	I/O	I/O
30	I/O	I/O
31	I/O	I/O
32	GND	GND
33	I/O	I/O
34	I/O	I/O
35	I/O	I/O
36	I/O	I/O
37	I/O	I/O
38	VCCA	VCCA
39	I/O	I/O
40	I/O	I/O
41	I/O	I/O
42	I/O	I/O
43	I/O	I/O
44	GND	GND
45	I/O	I/O
46	I/O	I/O
47	I/O	I/O
48	I/O	I/O
49	I/O	I/O
50	SDO, I/O	SDO, I/O
51	I/O	I/O
52	I/O	I/O
53	I/O	I/O
54	I/O	I/O
55	GND	GND
56	I/O	I/O

Table 56 • VQ100

VQ100		
Pin Number	A42MX09 Function	A42MX16 Function
93	I/O	I/O
94	GND	GND
95	I/O	I/O
96	I/O	I/O
97	I/O	I/O
98	I/O	I/O
99	I/O	I/O
100	DCLK, I/O	DCLK, I/O

Figure 48 • TQ176**Table 57 • TQ176**

TQ176			
Pin Number	A42MX09 Function	A42MX16 Function	A42MX24 Function
1	GND	GND	GND
2	MODE	MODE	MODE
3	I/O	I/O	I/O
4	I/O	I/O	I/O
5	I/O	I/O	I/O
6	I/O	I/O	I/O
7	I/O	I/O	I/O
8	NC	NC	I/O
9	I/O	I/O	I/O

Table 58 • CQ208

CQ208	
Pin Number	A42MX36 Function
111	I/O
112	I/O
113	I/O
114	I/O
115	I/O
116	I/O
117	I/O
118	I/O
119	I/O
120	I/O
121	I/O
122	I/O
123	I/O
124	I/O
125	I/O
126	GND
127	I/O
128	TCK, I/O
129	LP
130	VCCA
131	GND
132	VCCI
133	VCCA
134	I/O
135	I/O
136	VCCA
137	I/O
138	I/O
139	I/O
140	I/O
141	I/O
142	I/O
143	I/O
144	I/O
145	I/O
146	I/O
147	I/O

Table 60 • BG272

BG272	
Pin Number	A42MX36 Function
A6	I/O
A7	WD, I/O
A8	WD, I/O
A9	I/O
A10	I/O
A11	CLKA
A12	I/O
A13	I/O
A14	I/O
A15	I/O
A16	WD, I/O
A17	I/O
A18	I/O
A19	GND
A20	GND
B1	GND
B2	GND
B3	DCLK, I/O
B4	I/O
B5	I/O
B6	I/O
B7	WD, I/O
B8	I/O
B9	PRB, I/O
B10	I/O
B11	I/O
B12	WD, I/O
B13	I/O
B14	I/O
B15	WD, I/O
B16	I/O
B17	WD, I/O
B18	I/O
B19	GND
B20	GND
C1	I/O
C2	MODE

Figure 53 • CQ172

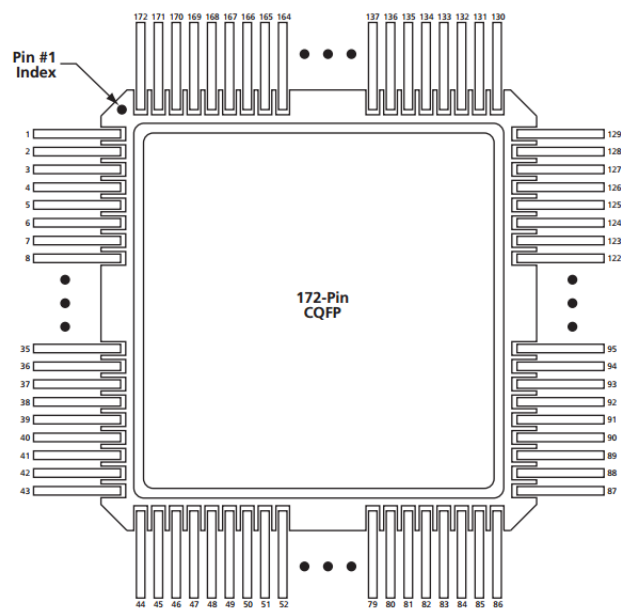


Table 62 • CQ172

CQ172	
Pin Number	A42MX16 Function
1	MODE
2	I/O
3	I/O
4	I/O
5	I/O
6	I/O
7	GND
8	I/O
9	I/O
10	I/O
11	I/O
12	VCC
13	I/O
14	I/O
15	I/O
16	I/O
17	GND
18	I/O
19	I/O
20	I/O