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Understanding **Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

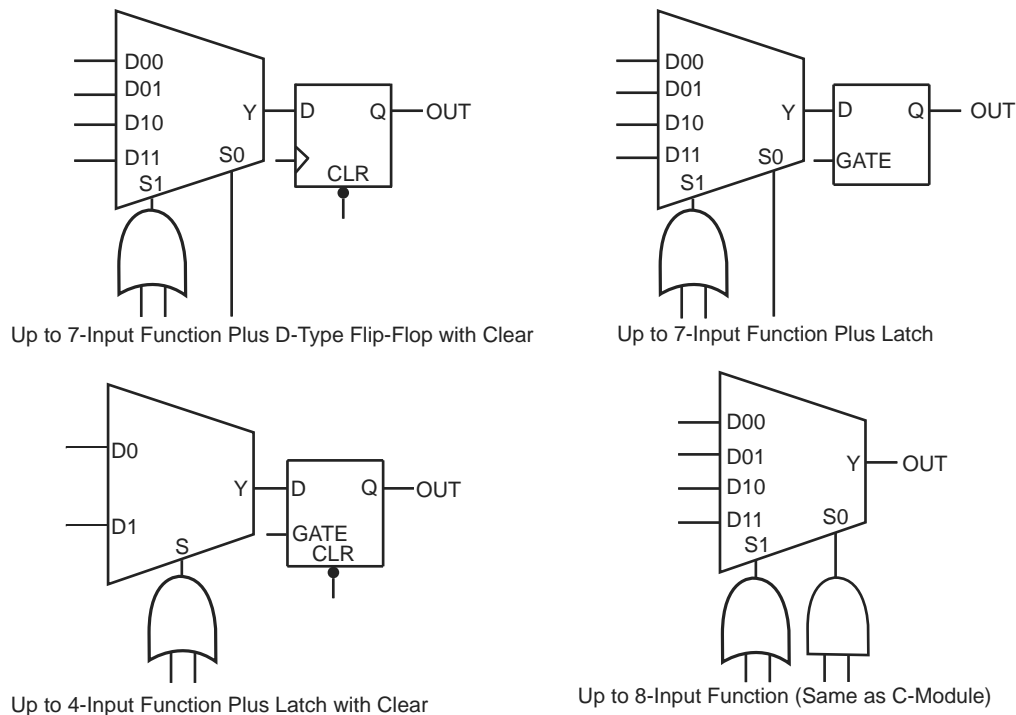
Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	34
Number of Gates	3000
Voltage - Supply	3V ~ 3.6V, 4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a40mx02-1plg44

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Figure 4 • 42MX S-Module Implementation

A42MX24 and A42MX36 devices contain D-modules, which are arranged around the periphery of the device. D-modules contain wide-decode circuitry, providing a fast, wide-input AND function similar to that found in CPLD architectures (Figure 5, page 9). The D-module allows A42MX24 and A42MX36 devices to perform wide-decode functions at speeds comparable to CPLDs and PALs. The output of the D-module has a programmable inverter for active HIGH or LOW assertion. The D-module output is hardwired to an output pin, and can also be fed back into the array to be incorporated into other logic.

3.2.2 Dual-Port SRAM Modules

The A42MX36 device contains dual-port SRAM modules that have been optimized for synchronous or asynchronous applications. The SRAM modules are arranged in 256-bit blocks that can be configured as 32x8 or 64x4. SRAM modules can be cascaded together to form memory spaces of user-definable width and depth. A block diagram of the A42MX36 dual-port SRAM block is shown in Figure 6, page 9.

The A42MX36 SRAM modules are true dual-port structures containing independent read and write ports. Each SRAM module contains six bits of read and write addressing (RDAD[5:0] and WRAD[5:0], respectively) for 64x4-bit blocks. When configured in byte mode, the highest order address bits (RDAD5 and WRAD5) are not used. The read and write ports of the SRAM block contain independent clocks (RCLK and WCLK) with programmable polarities offering active HIGH or LOW implementation. The SRAM block contains eight data inputs (WD[7:0]), and eight outputs (RD[7:0]), which are connected to segmented vertical routing tracks.

The A42MX36 dual-port SRAM blocks provide an optimal solution for high-speed buffered applications requiring FIFO and LIFO queues. The ACTgen Macro Builder within Microsemi's designer software provides capability to quickly design memory functions with the SRAM blocks. Unused SRAM blocks can be used to implement registers for other user logic within the design.

- VCCA = Power supply in volts (V)
- F = Switching frequency in megahertz (MHz)

3.4.4 Equivalent Capacitance

Equivalent capacitance is calculated by measuring ICC_{active} at a specified frequency and voltage for each circuit component of interest. Measurements have been made over a range of frequencies at a fixed value of VCC. Equivalent capacitance is frequency-independent, so the results can be used over a wide range of operating conditions. Equivalent capacitance values are shown below.

3.4.5 C_{EQ} Values for Microsemi MX FPGAs

Modules (C_{EQM}) 3.5

Input Buffers (C_{EQI}) 6.9

Output Buffers (C_{EQO}) 18.2

Routed Array Clock Buffer Loads (C_{EQCR}) 1.4

To calculate the active power dissipated from the complete design, the switching frequency of each part of the logic must be known. The equation below shows a piece-wise linear summation over all components.

$$\text{Power} = VCCA^2 * [(m \times C_{EQM} * f_m)_{\text{modules}} + (n * C_{EQI} * f_n)_{\text{inputs}} + (p * (C_{EQO} + C_L) * f_p)_{\text{outputs}} + 0.5 * (q_1 * C_{EQCR} * f_{q1})_{\text{routed_clk1}} + (r_1 * f_{q1})_{\text{routed_clk1}} + 0.5 * (q_2 * C_{EQCR} * f_{q2})_{\text{routed_clk2}} + (r_2 * f_{q2})_{\text{routed_clk2}}] \quad (2)$$

EQ 3

where:

m = Number of logic modules switching at frequency f_m

n = Number of input buffers switching at frequency f_n

p = Number of output buffers switching at frequency f_p

q₁ = Number of clock loads on the first routed array clock

q₂ = Number of clock loads on the second routed array clock

r₁ = Fixed capacitance due to first routed array clock

r₂ = Fixed capacitance due to second routed array clock

C_{EQM} = Equivalent capacitance of logic modules in pF

C_{EQI} = Equivalent capacitance of input buffers in pF

C_{EQO} = Equivalent capacitance of output buffers in pF

C_{EQCR} = Equivalent capacitance of routed array clock in pF

C_L = Output load capacitance in pF

f_m = Average logic module switching rate in MHz

f_n = Average input buffer switching rate in MHz

f_p = Average output buffer switching rate in MHz

f_{q1} = Average first routed array clock rate in MHz

f_{q2} = Average second routed array clock rate in MHz)

Table 7 • Fixed Capacitance Values for MX FPGAs (pF)

Device Type	r1 routed_Clk1	r2 routed_Clk2
A40MX02	41.4	N/A
A40MX04	68.6	N/A
A42MX09	118	118
A42MX16	165	165
A42MX24	185	185
A42MX36	220	220

3.4.6 Test Circuitry and Silicon Explorer II Probe

MX devices contain probing circuitry that provides built-in access to every node in a design, via the use of Silicon Explorer II. Silicon Explorer II is an integrated hardware and software solution that, in conjunction with the Designer software, allow users to examine any of the internal nets of the device while it is operating in a prototyping or a production system. The user can probe into an MX device without changing the placement and routing of the design and without using any additional resources. Silicon Explorer II's noninvasive method does not alter timing or loading effects, thus shortening the debug cycle and providing a true representation of the device under actual functional situations.

Silicon Explorer II samples data at 100 MHz (asynchronous) or 66 MHz (synchronous). Silicon Explorer II attaches to a PC's standard COM port, turning the PC into a fully functional 18-channel logic analyzer. Silicon Explorer II allows designers to complete the design verification process at their desks and reduces verification time from several hours per cycle to a few seconds.

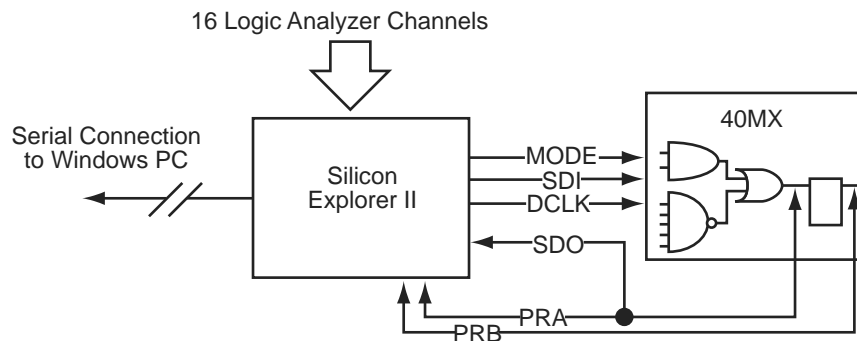
Silicon Explorer II is used to control the MODE, DCLK, SDI and SDO pins in MX devices to select the desired nets for debugging. The user simply assigns the selected internal nets in the Silicon Explorer II software to the PRA/PRB output pins for observation. Probing functionality is activated when the MODE pin is held HIGH.

Figure 12, page 16 illustrates the interconnection between Silicon Explorer II and 40MX devices, while Figure 13, page 17 illustrates the interconnection between Silicon Explorer II and 42MX devices

To allow for probing capabilities, the security fuses must not be programmed. (See User Security, page 12 for the security fuses of 40MX and 42MX devices). Table 8, page 17 summarizes the possible device configurations for probing.

PRA and PRB pins are dual-purpose pins. When the "Reserve Probe Pin" is checked in the Designer software, PRA and PRB pins are reserved as dedicated outputs for probing. If PRA and PRB pins are required as user I/Os to achieve successful layout and "Reserve Probe Pin" is checked, the layout tool will override the option and place user I/Os on PRA and PRB pins.

Figure 12 • Silicon Explorer II Setup with 40MX



Note: *Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the recommended operating conditions.

Table 14 • Recommended Operating Conditions

Parameter	Commercial	Industrial	Military	Units
Temperature Range*	0 to +70	−40 to +85	−55 to +125	°C
VCC (40MX)	4.75 to 5.25	4.5 to 5.5	4.5 to 5.5	V
VCCA (42MX)	4.75 to 5.25	4.5 to 5.5	4.5 to 5.5	V
VCCI (42MX)	4.75 to 5.25	4.5 to 5.5	4.5 to 5.5	V

Note: * Ambient temperature (T_A) is used for commercial and industrial grades; case temperature (T_C) is used for military grades.

3.7.1 5 V TTL Electrical Specifications

The following tables show 5 V TTL electrical specifications.

Table 15 • 5V TTL Electrical Specifications

Symbol	Parameter	Commercial		Commercial -F		Industrial		Military		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
VOH ¹	IOH = −10 mA	2.4		2.4						V
	IOH = −4 mA					3.7		3.7		V
VOL ¹	IOL = 10 mA		0.5		0.5					V
	IOL = 6 mA						0.4		0.4	V
VIL		−0.3	0.8	−0.3	0.8	−0.3	0.8	−0.3	0.8	V
VIH (40MX)		2.0	VCC + 0.3	2.0	VCC + 0.3	2.0	VCC + 0.3	2.0	VCC + 0.3	V
VIH (42MX) ²		2.0	VCCI + 0.3	2.0	VCCI + 0.3	2.0	VCCI + 0.3	2.0	VCCI + 0.3	V
IIL	VIN = 0.5 V		−10		−10		−10		−10	μA
IIH	VIN = 2.7 V		−10		−10		−10		−10	μA
Input Transition Time, T_R and T_F			500		500		500		500	ns
C_{IO} I/O Capacitance			10		10		10		10	pF
Standby Current, ICC ³	A40MX02, A40MX04		3		25		10		25	mA
	A42MX09		5		25		25		25	mA
	A42MX16		6		25		25		25	mA
	A42MX24, A42MX36		20		25		25		25	mA
Low power mode Standby Current	42MX devices only		0.5		ICC − 5.0		ICC − 5.0		ICC − 5.0	mA
IIO, I/O source sink current	Can be derived from the <i>IBIS model</i> (http://www.microsemi.com/soc/techdocs/models/ibis.html)									

1. Only one output tested at a time. VCC/VCCI = min

2. VIH(Min) is 2.4V for A42MX36 family. This applies only to VCCI of 5V and is not applicable to VCCI of 3.3V

3.9.3 Output Drive Characteristics for 3.3 V PCI Signaling

Table 25 • DC Specification (3.3 V PCI Signaling)¹

Symbol	Parameter	Condition	PCI		MX		Units
			Min.	Max.	Min.	Max.	
VCCI	Supply Voltage for I/Os		3.0	3.6	3.0	3.6 ²	V
VIH	Input High Voltage		0.5	VCC + 0.5	0.5	VCCI + 0.3	V
VIL	Input Low Voltage		-0.5	0.8	-0.3	0.8	V
IIH	Input High Leakage Current	VIN = 2.7 V		70		10	μA
IIL	Input Leakage Current			-70		-10	μA
VOH	Output High Voltage	IOUT = -2 mA	0.9		3.3		V
VOL	Output Low Voltage	IOUT = 3 mA, 6 mA		0.1		0.1 VCCI	V
CIN	Input Pin Capacitance			10		10	pF
CCLK	CLK Pin Capacitance		5	12		10	pF
LPIN	Pin Inductance			20		< 8 nH ³	nH

1. PCI Local Bus Specification, Version 2.1, Section 4.2.2.1.

2. Maximum rating for VCCI -0.5 V to 7.0V.

3. Dependent upon the chosen package. PCI recommends QFP and BGA packaging to reduce pin inductance and capacitance.

Table 26 • AC Specifications for (3.3 V PCI Signaling)*

Symbol	Parameter	Condition	PCI		MX		Units
			Min.	Max.	Min.	Max.	
ICL	Low Clamp Current	-5 < VIN ≤ -1	-25 + (VIN + 1) / 0.015		-60	-10	mA
Slew (r)	Output Rise Slew Rate	0.2 V to 0.6 V load	1	4	1.8	2.8	V/ns
Slew (f)	Output Fall Slew Rate	0.6 V to 0.2 V load	1	4	2.8	4.0	V/ns

Note: *PCI Local Bus Specification, Version 2.1, Section 4.2.2.2.

approximately a 3 ns to a 6 ns delay, which is represented statistically in higher fanout (FO=8) routing delays in the data sheet specifications section, shown in Table 34, page 41.

3.11.3 Timing Derating

MX devices are manufactured with a CMOS process. Therefore, device performance varies according to temperature, voltage, and process changes. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature and best-case processing. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature and worst-case processing.

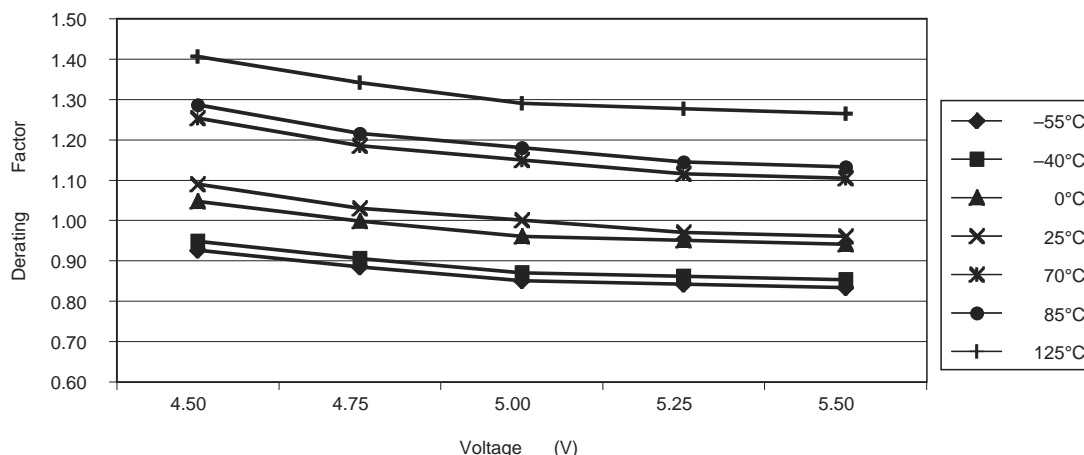
3.11.4 Temperature and Voltage Derating Factors

The following tables and figures show temperature and voltage derating factors for 40MX and 42MX FPGAs.

Table 28 • 42MX Temperature and Voltage Derating Factors (Normalized to $T_J = 25^\circ\text{C}$, $V_{CCA} = 5.0\text{ V}$)

42MX Voltage	Temperature						
	-55°C	-40°C	0°C	25°C	70°C	85°C	125°C
4.50	0.93	0.95	1.05	1.09	1.25	1.29	1.41
4.75	0.88	0.90	1.00	1.03	1.18	1.22	1.34
5.00	0.85	0.87	0.96	1.00	1.15	1.18	1.29
5.25	0.84	0.86	0.95	0.97	1.12	1.14	1.28
5.50	0.83	0.85	0.94	0.96	1.10	1.13	1.26

Figure 34 • 42MX Junction Temperature and Voltage Derating Curves (Normalized to $T_J = 25^\circ\text{C}$, $V_{CCA} = 5.0\text{ V}$)



Note: This derating factor applies to all routing and propagation delays

Table 29 • 40MX Temperature and Voltage Derating Factors (Normalized to $T_J = 25^\circ\text{C}$, $V_{CC} = 5.0\text{ V}$)

40MX Voltage	Temperature						
	-55°C	-40°C	0°C	25°C	70°C	85°C	125°C
4.50	0.89	0.93	1.02	1.09	1.25	1.31	1.45
4.75	0.84	0.88	0.97	1.03	1.18	1.24	1.37
5.00	0.82	0.85	0.94	1.00	1.15	1.20	1.33
5.25	0.80	0.82	0.91	0.97	1.12	1.16	1.29
5.50	0.79	0.82	0.90	0.96	1.10	1.15	1.28

Table 38 • A42MX09 Timing Characteristics (Nominal 5.0 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description	-3 Speed		-2 Speed		-1 Speed		Std Speed		-F Speed		Units
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{WASYN} Flip-Flop (Latch) Asynchronous Pulse Width	4.5		4.9		5.6		6.6		9.2		ns
t _A Flip-Flop Clock Input Period	3.5		3.8		4.3		5.1		7.1		ns
t _{INH} Input Buffer Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{INSU} Input Buffer Latch Set-Up	0.3		0.3		0.4		0.4		0.6		ns
t _{OUTH} Output Buffer Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{OUTSU} Output Buffer Latch Set-Up	0.3		0.3		0.4		0.4		0.6		ns
f _{MAX} Flip-Flop (Latch) Clock Frequency		268		244		224		195		117	MHz

Table 40 • A42MX16 Timing Characteristics (Nominal 5.0 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description		-3 Speed		-2 Speed		-1 Speed		Std Speed		-F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{RD3}	FO = 3 Routing Delay		1.3		1.4		1.6		1.9		2.7	ns
t _{RD4}	FO = 4 Routing Delay		1.6		1.7		2.0		2.3		3.2	ns
t _{RD8}	FO = 8 Routing Delay		2.6		2.9		3.2		3.8		5.3	ns
Logic Module Sequential Timing^{3,4}												
t _{SUD}	Flip-Flop (Latch) Data Input Set-Up		0.3		0.4		0.4		0.5		0.7	ns
t _{HD}	Flip-Flop (Latch) Data Input Hold		0.0		0.0		0.0		0.0		0.0	ns
t _{SUENA}	Flip-Flop (Latch) Enable Set-Up		0.7		0.8		0.9		1.0		1.4	ns
t _{HENA}	Flip-Flop (Latch) Enable Hold		0.0		0.0		0.0		0.0		0.0	ns
t _{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width		3.4		3.8		4.3		5.0		7.1	ns
t _{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width		4.5		5.0		5.6		6.6		9.2	ns
t _A	Flip-Flop Clock Input Period		6.8		7.6		8.6		10.1		14.1	ns
t _{INH}	Input Buffer Latch Hold		0.0		0.0		0.0		0.0		0.0	ns
t _{INSU}	Input Buffer Latch Set-Up		0.5		0.5		0.6		0.7		1.0	ns
t _{OUTH}	Output Buffer Latch Hold		0.0		0.0		0.0		0.0		0.0	ns
t _{OUTSU}	Output Buffer Latch Set-Up		0.5		0.5		0.6		0.7		1.0	ns
f _{MAX}	Flip-Flop (Latch) Clock Frequency		215		195		179		156		94	MHz
Input Module Propagation Delays												
t _{INYH}	Pad-to-Y HIGH		1.1		1.2		1.3		1.6		2.2	ns
t _{INYL}	Pad-to-Y LOW		0.8		0.9		1.0		1.2		1.7	ns
t _{INGH}	G to Y HIGH		1.4		1.6		1.8		2.1		2.9	ns
t _{INGL}	G to Y LOW		1.4		1.6		1.8		2.1		2.9	ns
Input Module Predicted Routing Delays²												
t _{IRD1}	FO = 1 Routing Delay		1.8		2.0		2.3		2.7		4.0	ns
t _{IRD2}	FO = 2 Routing Delay		2.1		2.3		2.6		3.1		4.3	ns
t _{IRD3}	FO = 3 Routing Delay		2.3		2.6		3.0		3.5		4.9	ns
t _{IRD4}	FO = 4 Routing Delay		2.6		3.0		3.3		3.9		5.4	ns
t _{IRD8}	FO = 8 Routing Delay		3.6		4.0		4.6		5.4		7.5	ns
Global Clock Network												
t _{CKH}	Input LOW to HIGH	FO = 32	2.6		2.9		3.3		3.9		5.4	ns
		FO = 384	2.9		3.2		3.6		4.3		6.0	ns
t _{CKL}	Input HIGH to LOW	FO = 32	3.8		4.2		4.8		5.6		7.8	ns
		FO = 384	4.5		5.0		5.6		6.6		9.2	ns
t _{PWH}	Minimum Pulse Width HIGH	FO = 32	3.2		3.5		4.0		4.7		6.6	ns
		FO = 384	3.7		4.1		4.6		5.4		7.6	ns

Table 40 • A42MX16 Timing Characteristics (Nominal 5.0 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description	-3 Speed		-2 Speed		-1 Speed		Std Speed		-F Speed		Units
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
TTL Output Module Timing⁴											
t _{DLH}	Data-to-Pad HIGH	2.5	2.8	3.2	3.7	5.2	ns				
t _{DHL}	Data-to-Pad LOW	3.0	3.3	3.7	4.4	6.1	ns				
t _{ENZH}	Enable Pad Z to HIGH	2.7	3.0	3.4	4.0	5.6	ns				
t _{ENZL}	Enable Pad Z to LOW	3.0	3.3	3.8	4.4	6.2	ns				
t _{ENHZ}	Enable Pad HIGH to Z	5.4	6.0	6.8	8.0	11.2	ns				
t _{ENLZ}	Enable Pad LOW to Z	5.0	5.6	6.3	7.4	10.4	ns				
t _{GLH}	G-to-Pad HIGH	2.9	3.2	3.6	4.3	6.0	ns				
t _{GHL}	G-to-Pad LOW	2.9	3.2	3.6	4.3	6.0	ns				
t _{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading	5.7	6.3	7.1	8.4	11.9	ns				
t _{ACO}	Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading	8.0	8.9	10.1	11.9	16.7	ns				
d _{TLH}	Capacitive Loading, LOW to HIGH	0.03	0.03	0.03	0.04	0.06	ns/pF				
d _{THL}	Capacitive Loading, HIGH to LOW	0.04	0.04	0.04	0.05	0.07	ns/pF				

Table 41 • A42MX16 Timing Characteristics (Nominal 3.3 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)

Parameter / Description			-3 Speed		-2 Speed		-1 Speed		Std Speed		-F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{PWL}	Minimum Pulse Width LOW	FO = 32	5.3	5.9	6.7	7.8	11.0	ns					
		FO = 384	6.2	6.9	7.9	9.2	12.9	ns					
t _{CKSW}	Maximum Skew	FO = 32	0.5	0.5	0.6	0.7	1.0	ns					
		FO = 384	2.2	2.4	2.7	3.2	4.5	ns					
t _{SUEXT}	Input Latch External Set-Up	FO = 32	0.0	0.0	0.0	0.0	0.0	ns					
		FO = 384	0.0	0.0	0.0	0.0	0.0	ns					
t _{HEXT}	Input Latch External Hold	FO = 32	3.9	4.3	4.9	5.7	8.0	ns					
		FO = 384	4.5	4.9	5.6	6.6	9.2	ns					
t _P	Minimum Period	FO = 32	7.0	7.8	8.4	9.7	16.2	ns					
		FO = 384	7.7	8.6	9.3	10.7	17.8	ns					
f _{MAX}	Maximum Frequency	FO = 32	142	129	119	103	62	MHz					
		FO = 384	129	117	108	94	56	MHz					
TTL Output Module Timing⁵													
t _{DLH}	Data-to-Pad HIGH		3.5	3.9	4.4	5.2	7.3	ns					
t _{DHL}	Data-to-Pad LOW		4.1	4.6	5.2	6.1	8.6	ns					
t _{ENZH}	Enable Pad Z to HIGH		3.8	4.2	4.8	5.6	7.8	ns					
t _{ENZL}	Enable Pad Z to LOW		4.2	4.6	5.3	6.2	8.7	ns					
t _{ENHZ}	Enable Pad HIGH to Z		7.6	8.4	9.5	11.2	15.7	ns					
t _{ENLZ}	Enable Pad LOW to Z		7.0	7.8	8.8	10.4	14.5	ns					
t _{GLH}	G-to-Pad HIGH		4.8	5.3	6.0	7.2	10.0	ns					
t _{GHL}	G-to-Pad LOW		4.8	5.3	6.0	7.2	10.0	ns					
t _{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading		8.0	8.9	10.1	11.9	16.7	ns					
t _{ACO}	Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading		11.3	12.5	14.2	16.7	23.3	ns					
d _{TLH}	Capacitive Loading, LOW to HIGH		0.04	0.04	0.05	0.06	0.08	ns/pF					
d _{THL}	Capacitive Loading, HIGH to LOW		0.05	0.05	0.06	0.07	0.10	ns/pF					
CMOS Output Module Timing⁵													
t _{DLH}	Data-to-Pad HIGH		4.5	5.0	5.6	6.6	9.3	ns					
t _{DHL}	Data-to-Pad LOW		3.4	3.8	4.3	5.1	7.1	ns					
t _{ENZH}	Enable Pad Z to HIGH		3.8	4.2	4.8	5.6	7.8	ns					
t _{ENZL}	Enable Pad Z to LOW		4.2	4.6	5.3	6.2	8.7	ns					
t _{ENHZ}	Enable Pad HIGH to Z		7.6	8.4	9.5	11.2	15.7	ns					
t _{ENLZ}	Enable Pad LOW to Z		7.0	7.8	8.8	10.4	14.5	ns					
t _{GLH}	G-to-Pad HIGH		7.1	7.9	8.9	10.5	14.7	ns					
t _{GHL}	G-to-Pad LOW		7.1	7.9	8.9	10.5	14.7	ns					
t _{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading		8.0	8.9	10.1	11.9	16.7	ns					

Table 44 • A42MX36 Timing Characteristics (Nominal 5.0 V Operation)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description	-3 Speed		-2 Speed		-1 Speed		Std Speed		-F Speed		Units
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Logic Module Combinatorial Functions¹											
t _{PD}	Internal Array Module Delay	1.3	1.5	1.7	2.0	2.7	ns				
t _{PDD}	Internal Decode Module Delay	1.6	1.8	2.0	2.4	3.3	ns				
Logic Module Predicted Routing Delays²											
t _{RD1}	FO = 1 Routing Delay	0.9	1.0	1.2	1.4	2.0	ns				
t _{RD2}	FO = 2 Routing Delay	1.3	1.4	1.6	1.9	2.7	ns				
t _{RD3}	FO = 3 Routing Delay	1.6	1.8	2.0	2.4	3.4	ns				
t _{RD4}	FO = 4 Routing Delay	2.0	2.2	2.5	2.9	4.1	ns				
t _{RD5}	FO = 8 Routing Delay	3.3	3.7	4.2	4.9	6.9	ns				
t _{RDD}	Decode-to-Output Routing Delay	0.3	0.4	0.4	0.5	0.7	ns				
Logic Module Sequential Timing^{3, 4}											
t _{CO}	Flip-Flop Clock-to-Output	1.3	1.4	1.6	1.9	2.7	ns				
t _{GO}	Latch Gate-to-Output	1.3	1.4	1.6	1.9	2.7	ns				
t _{SUD}	Flip-Flop (Latch) Set-Up Time	0.3	0.3	0.4	0.5	0.7	ns				
t _{HD}	Flip-Flop (Latch) Hold Time	0.0	0.0	0.0	0.0	0.0	ns				
t _{RO}	Flip-Flop (Latch) Reset-to-Output	1.6	1.7	2.0	2.3	3.2	ns				
t _{SUENA}	Flip-Flop (Latch) Enable Set-Up	0.7	0.8	0.9	1.0	1.4	ns				
t _{HENA}	Flip-Flop (Latch) Enable Hold	0.0	0.0	0.0	0.0	0.0	ns				
t _{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	3.3	3.7	4.2	4.9	6.9	ns				
t _{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	4.4	4.8	5.5	6.4	9.0	ns				
Synchronous SRAM Operations											
t _{RC}	Read Cycle Time	6.8	7.5	8.5	10.0	14.0	ns				
t _{WC}	Write Cycle Time	6.8	7.5	8.5	10.0	14.0	ns				
t _{RCKHL}	Clock HIGH/LOW Time	3.4	3.8	4.3	5.0	7.0	ns				
t _{RCO}	Data Valid After Clock HIGH/LOW	3.4	3.8	4.3	5.0	7.0	ns				
t _{ADSU}	Address/Data Set-Up Time	1.6	1.8	2.0	2.4	3.4	ns				
Synchronous SRAM Operations (continued)											
t _{ADH}	Address/Data Hold Time	0.0	0.0	0.0	0.0	0.0	ns				
t _{RENSU}	Read Enable Set-Up	0.6	0.7	0.8	0.9	1.3	ns				
t _{RENH}	Read Enable Hold	3.4	3.8	4.3	5.0	7.0	ns				
t _{WENSU}	Write Enable Set-Up	2.7	3.0	3.4	4.0	5.6	ns				
t _{WENH}	Write Enable Hold	0.0	0.0	0.0	0.0	0.0	ns				
t _{BENS}	Block Enable Set-Up	2.8	3.1	3.5	4.1	5.7	ns				
t _{BENH}	Block Enable Hold	0.0	0.0	0.0	0.0	0.0	ns				

Table 44 • A42MX36 Timing Characteristics (Nominal 5.0 V Operation)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description			-3 Speed		-2 Speed		-1 Speed		Std Speed		-F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{SUEXT}	Input Latch External Set-Up	FO = 32	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	ns	
		FO = 635	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	ns	
t _{HEXT}	Input Latch External Hold	FO = 32	2.8	3.2	3.6	4.2	4.2	4.9	5.9	6.9	ns	ns	
		FO = 635	3.3	3.7	4.2	4.9	5.9	6.9	ns	ns			
t _P	Minimum Period (1/f _{MAX})	FO = 32	5.5	6.1	6.6	7.6	12.7	ns	ns				
		FO = 635	6.0	6.6	7.2	8.3	13.8	ns	ns				
f _{MAX}	Maximum Datapath Frequency	FO = 32	180	164	151	131	79	MHz					
		FO = 635	166	151	139	121	73	MHz					
TTL Output Module Timing⁵													
t _{DLH}	Data-to-Pad HIGH		2.6	2.8	3.2	3.8	5.3	ns					
t _{DHL}	Data-to-Pad LOW		3.0	3.3	3.7	4.4	6.2	ns					
t _{ENZH}	Enable Pad Z to HIGH		2.7	3.0	3.3	3.9	5.5	ns					
t _{ENZL}	Enable Pad Z to LOW		3.0	3.3	3.7	4.3	6.1	ns					
t _{ENHZ}	Enable Pad HIGH to Z		5.3	5.8	6.6	7.8	10.9	ns					

Table 45 • A42MX36 Timing Characteristics (Nominal 3.3 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)

Parameter / Description	-3 Speed		-2 Speed		-1 Speed		Std Speed		-F Speed		Units
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{ACO} Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O		10.9		12.1		13.7		16.1		22.5	ns
d _{TLH} Capacitive Loading, LOW to HIGH		0.10		0.11		0.12		0.14		0.20	ns/pF
d _{THL} Capacitive Loading, HIGH to LOW		0.10		0.11		0.12		0.14		0.20	ns/pF
CMOS Output Module Timing⁵											
t _{DLH} Data-to-Pad HIGH		4.9		5.5		6.2		7.3		10.3	ns
t _{DHL} Data-to-Pad LOW		3.4		3.8		4.3		5.1		7.1	ns
t _{ENZH} Enable Pad Z to HIGH		3.7		4.1		4.7		5.5		7.7	ns
t _{ENZL} Enable Pad Z to LOW		4.1		4.6		5.2		6.1		8.5	ns
t _{ENHZ} Enable Pad HIGH to Z		7.4		8.2		9.3		10.9		15.3	ns
t _{ENLZ} Enable Pad LOW to Z		6.9		7.6		8.7		10.2		14.3	ns
t _{GLH} G-to-Pad HIGH		7.0		7.8		8.9		10.4		14.6	ns
t _{GHL} G-to-Pad LOW		7.0		7.8		8.9		10.4		14.6	ns
t _{LSU} I/O Latch Set-Up	0.7		0.7		0.8		1.0		1.4		ns
t _{LH} I/O Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{LCO} I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		7.9		8.8		10.0		11.8		16.5	ns

1. For dual-module macros, use t_{PD1} + t_{RD1} + t_{PDn}, t_{CO} + t_{RD1} + t_{PDn}, or t_{PD1} + t_{RD1} + t_{SUD}, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
4. *Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*
5. Delays based on 35 pF loading.

3.12 Pin Descriptions

This section lists the pin descriptions for 40MX and 42MX series FPGAs.

CLK/A/B, I/O Global Clock

Clock inputs for clock distribution networks. CLK is for 40MX while CLKA and CLKB are for 42MX devices. The clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

DCLK, I/O Diagnostic Clock

Clock input for diagnostic probe and device programming. DCLK is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

GND, Ground

Input LOW supply voltage.

I/O, Input/Output

Table 51 • PQ144

PQ144	
Pin Number	A42MX09 Function
43	I/O
44	GNDQ
45	GNDI
46	NC
47	I/O
48	I/O
49	I/O
50	I/O
51	I/O
52	I/O
53	I/O
54	VCC
55	VCCI
56	NC
57	I/O
58	I/O
59	I/O
60	I/O
61	I/O
62	I/O
63	I/O
64	GND
65	GNDI
66	I/O
67	I/O
68	I/O
69	I/O
70	I/O
71	SDO
72	I/O
73	I/O
74	I/O
75	I/O
76	I/O
77	I/O
78	I/O
79	GNDQ

Table 53 • PQ208

PQ208			
Pin Number	A42MX16 Function	A42MX24 Function	A42MX36 Function
95	NC	I/O	I/O
96	NC	I/O	I/O
97	NC	I/O	I/O
98	VCCI	VCCI	VCCI
99	I/O	I/O	I/O
100	I/O	WD, I/O	WD, I/O
101	I/O	WD, I/O	WD, I/O
102	I/O	I/O	I/O
103	SDO, I/O	SDO, TDO, I/O	SDO, TDO, I/O
104	I/O	I/O	I/O
105	GND	GND	GND
106	NC	VCCA	VCCA
107	I/O	I/O	I/O
108	I/O	I/O	I/O
109	I/O	I/O	I/O
110	I/O	I/O	I/O
111	I/O	I/O	I/O
112	NC	I/O	I/O
113	NC	I/O	I/O
114	NC	I/O	I/O
115	NC	I/O	I/O
116	I/O	I/O	I/O
117	I/O	I/O	I/O
118	I/O	I/O	I/O
119	I/O	I/O	I/O
120	I/O	I/O	I/O
121	I/O	I/O	I/O
122	I/O	I/O	I/O
123	I/O	I/O	I/O
124	I/O	I/O	I/O
125	I/O	I/O	I/O
126	GND	GND	GND
127	I/O	I/O	I/O
128	I/O	TCK, I/O	TCK, I/O
129	LP	LP	LP
130	VCCA	VCCA	VCCA
131	GND	GND	GND

Table 56 • VQ100

VQ100		
Pin Number	A42MX09 Function	A42MX16 Function
21	I/O	I/O
22	I/O	I/O
23	I/O	I/O
24	I/O	I/O
25	I/O	I/O
26	I/O	I/O
27	I/O	I/O
28	I/O	I/O
29	I/O	I/O
30	I/O	I/O
31	I/O	I/O
32	GND	GND
33	I/O	I/O
34	I/O	I/O
35	I/O	I/O
36	I/O	I/O
37	I/O	I/O
38	VCCA	VCCA
39	I/O	I/O
40	I/O	I/O
41	I/O	I/O
42	I/O	I/O
43	I/O	I/O
44	GND	GND
45	I/O	I/O
46	I/O	I/O
47	I/O	I/O
48	I/O	I/O
49	I/O	I/O
50	SDO, I/O	SDO, I/O
51	I/O	I/O
52	I/O	I/O
53	I/O	I/O
54	I/O	I/O
55	GND	GND
56	I/O	I/O

Table 57 • TQ176

TQ176			
Pin Number	A42MX09 Function	A42MX16 Function	A42MX24 Function
158	CLKB, I/O	CLKB, I/O	CLKB, I/O
159	I/O	I/O	I/O
160	PRB, I/O	PRB, I/O	PRB, I/O
161	NC	I/O	WD, I/O
162	I/O	I/O	WD, I/O
163	I/O	I/O	I/O
164	I/O	I/O	I/O
165	NC	NC	WD, I/O
166	NC	I/O	WD, I/O
167	I/O	I/O	I/O
168	NC	I/O	I/O
169	I/O	I/O	I/O
170	NC	VCCI	VCCI
171	I/O	I/O	WD, I/O
172	I/O	I/O	WD, I/O
173	NC	I/O	I/O
174	I/O	I/O	I/O
175	DCLK, I/O	DCLK, I/O	DCLK, I/O
176	I/O	I/O	I/O

Figure 49 • CQ208

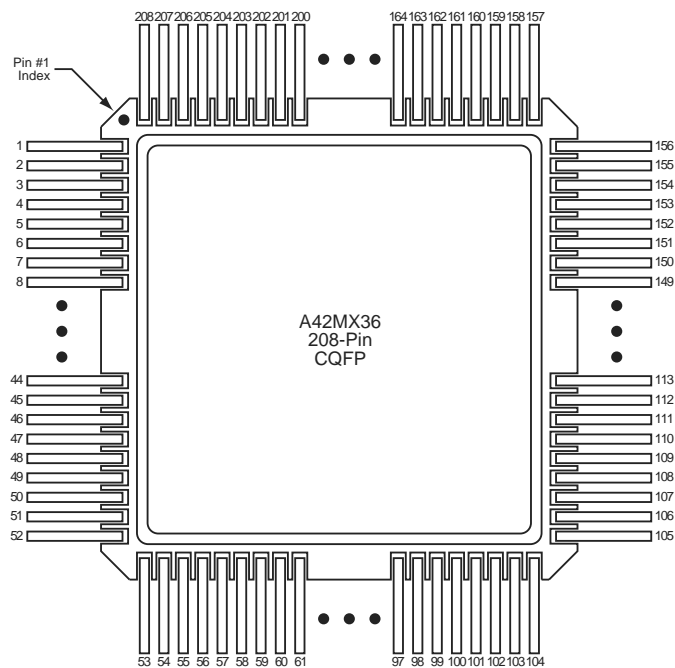


Table 62 • CQ172

60	I/O
61	I/O
62	I/O
63	I/O
64	I/O
65	GND
66	VCC
67	I/O
68	I/O
69	I/O
70	I/O
71	I/O
72	I/O
73	I/O
74	I/O
75	GND
76	I/O
77	I/O
78	I/O
79	I/O
80	VCCI
81	I/O
82	I/O
83	I/O
84	I/O
85	SDO
86	I/O
87	I/O
88	I/O
89	I/O
90	I/O
91	I/O
92	I/O
93	I/O
94	I/O
95	I/O
96	I/O
97	I/O
98	GND