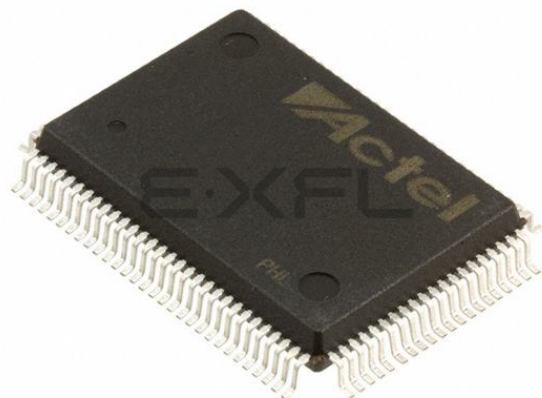




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	57
Number of Gates	3000
Voltage - Supply	3V ~ 3.6V, 4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TC)
Package / Case	100-BQFP
Supplier Device Package	100-PQFP (20x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a40mx02-1pq100m

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3 40MX and 42MX FPGAs

3.1 General Description

Microsemi's 40MX and 42MX families offer a cost-effective design solution at 5V. The MX devices are single-chip solutions and provide high performance while shortening the system design and development cycle. MX devices can integrate and consolidate logic implemented in multiple PALs, CPLDs, and FPGAs. Example applications include high-speed controllers and address decoding, peripheral bus interfaces, DSP, and co-processor functions.

The MX device architecture is based on Microsemi's patented antifuse technology implemented in a 0.45µm triple-metal CMOS process. With capacities ranging from 3,000 to 54,000 system gates, the MX devices provide performance up to 250 MHz, are live on power-up and have one-fifth the standby power consumption of comparable FPGAs. MX FPGAs provide up to 202 user I/Os and are available in a wide variety of packages and speed grades.

A42MX24 and A42MX36 devices also feature multiPlex I/Os, which support mixed-voltage systems, enable programmable PCI, deliver high-performance operation at both 5.0V and 3.3V, and provide a low-power mode. The devices are fully compliant with the PCI local bus specification (version 2.1). They deliver 200 MHz on-chip operation and 6.1 ns clock-to-output performance.

The 42MX24 and 42MX36 devices include system-level features such as IEEE Standard 1149.1 (JTAG) Boundary Scan Testing and fast wide-decode modules. In addition, the A42MX36 device offers dual-port SRAM for implementing fast FIFOs, LIFOs, and temporary data storage. The storage elements can efficiently address applications requiring wide data path manipulation and can perform transformation functions such as those required for telecommunications, networking, and DSP.

All MX devices are fully tested over automotive and military temperature ranges. In addition, the largest member of the family, the A42MX36, is available in both CQ208 and CQ256 ceramic packages screened to MIL-STD-883 levels. For easy prototyping and conversion from plastic to ceramic, the CQ208 and PQ208 devices are pin-compatible.

3.2 MX Architectural Overview

The MX devices are composed of fine-grained building blocks that enable fast, efficient logic designs. All devices within these families are composed of logic modules, I/O modules, routing resources and clock networks, which are the building blocks for fast logic designs. In addition, the A42MX36 device contains embedded dual-port SRAM modules, which are optimized for high-speed data path functions such as FIFOs, LIFOs and scratch pad memory. A42MX24 and A42MX36 also contain wide-decode modules.

3.2.1 Logic Modules

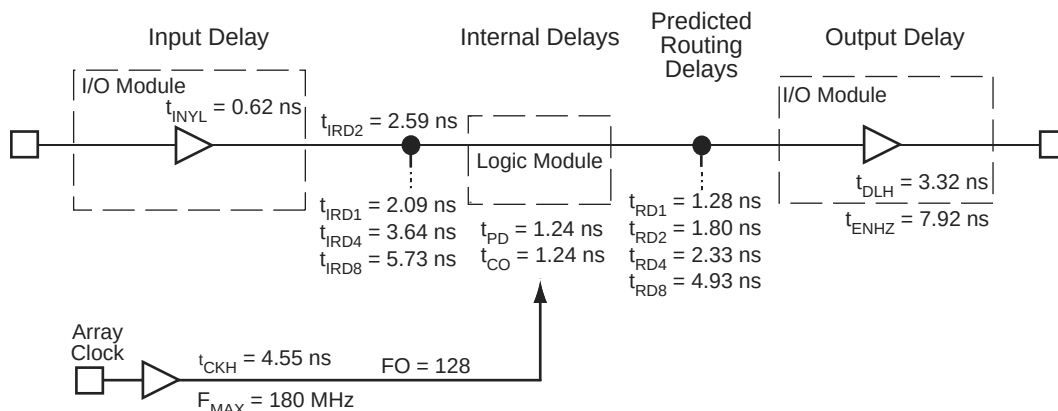
The 40MX logic module is an eight-input, one-output logic circuit designed to implement a wide range of logic functions with efficient use of interconnect routing resources.(see the following figure).

The logic module can implement the four basic logic functions (NAND, AND, OR and NOR) in gates of two, three, or four inputs. The logic module can also implement a variety of D-latches, exclusivity functions, AND-ORs and OR-ANDs. No dedicated hard-wired latches or flip-flops are required in the array; latches and flip-flops can be constructed from logic modules whenever required in the application.

3.10 Timing Models

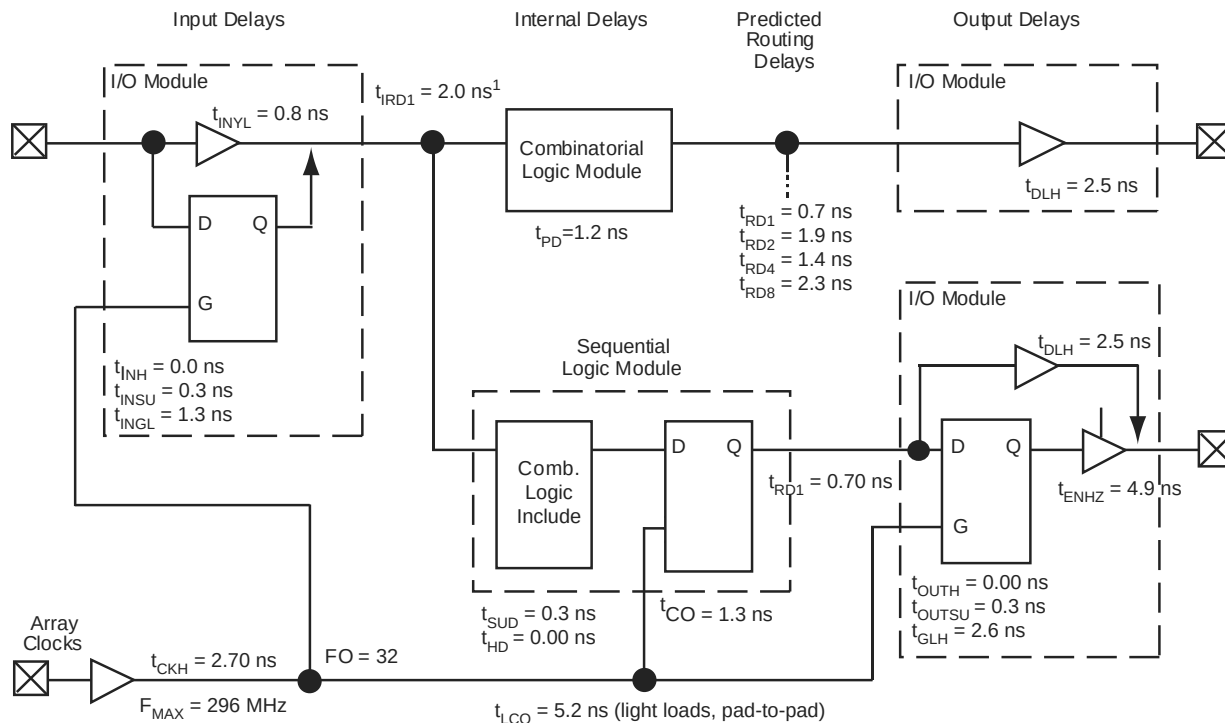
The following figures show various timing models.

Figure 17 • 40MX Timing Model*



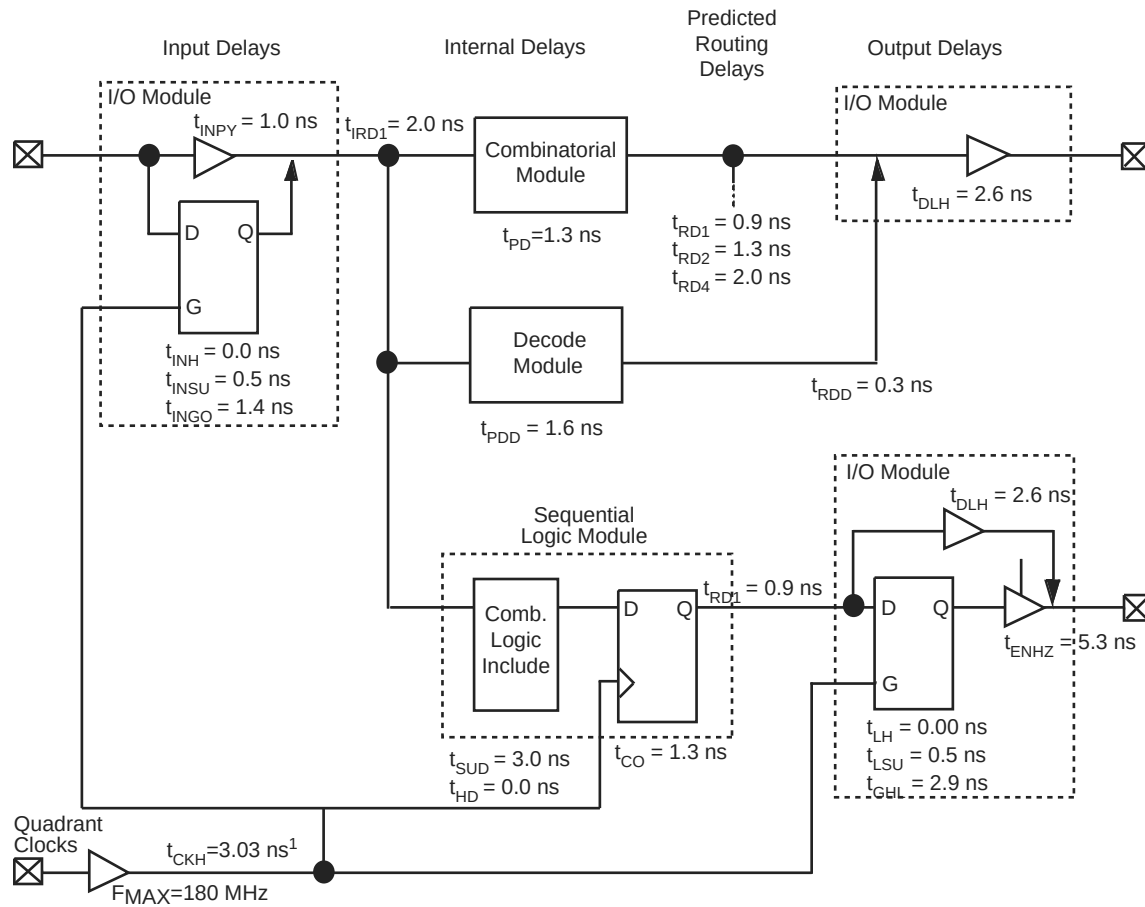
Note: Values are shown for 40MX –3 speed devices at 5.0 V worst-case commercial conditions.

Figure 18 • 42MX Timing Model



Note: 1. Input module predicted routing delay

Note: 2. Values are shown for A42MX09 –3 at 5.0 V worst-case commercial conditions.

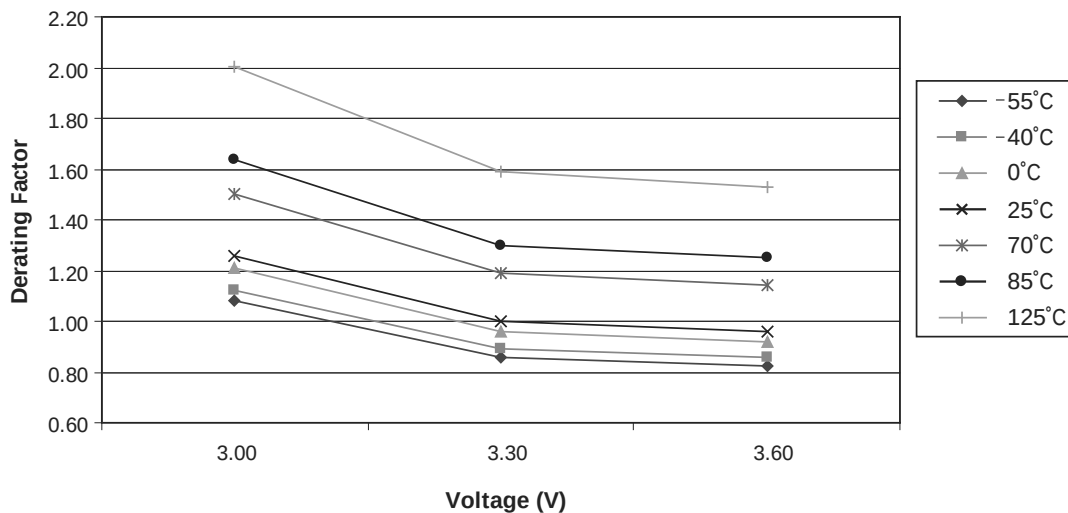
Figure 19 • 42MX Timing Model (Logic Functions Using Quadrant Clocks)

Note: 1. Load-dependent

Note: 2. Values are shown for A42MX36 –3 at 5.0 V worst-case commercial conditions

Table 31 • 40MX Temperature and Voltage Derating Factors (Normalized to $T_J = 25^\circ\text{C}$, $V_{CC} = 3.3\text{ V}$)

40MX Voltage	Temperature						
	-55°C	-40°C	0°C	25°C	70°C	85°C	125°C
3.60	0.83	0.85	0.92	0.96	1.14	1.25	1.53

Figure 37 • 40MX Junction Temperature and Voltage Derating Curves (Normalized to $T_J = 25^\circ\text{C}$, $V_{CC} = 3.3\text{ V}$)

Note: This derating factor applies to all routing and propagation delays

3.11.5 PCI System Timing Specification

The following tables list the critical PCI timing parameters and the corresponding timing parameters for the MX PCI-compliant devices.

3.11.6 PCI Models

Microsemi provides synthesizable VHDL and Verilog-HDL models for a PCI Target interface, a PCI Target and Target+DMA Master interface. Contact the Microsemi sales representative for more details.

Table 32 • Clock Specification for 33 MHz PCI

Symbol	Parameter	PCI		A42MX24		A42MX36		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYC}	CLK Cycle Time	30	–	4.0	–	4.0	–	ns
t_{HIGH}	CLK High Time	11	–	1.9	–	1.9	–	ns
t_{LOW}	CLK Low Time	11	–	1.9	–	1.9	–	ns

Table 33 • Timing Parameters for 33 MHz PCI

Symbol	Parameter	PCI		A42MX24		A42MX36		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{VAL}	CLK to Signal Valid—Bused Signals	2	11	2.0	9.0	2.0	9.0	ns
$t_{VAL(PTP)}$	CLK to Signal Valid—Point-to-Point	2 ²	12	2.0	9.0	2.0	9.0	ns
t_{ON}	Float to Active	2	–	2.0	4.0	2.0	4.0	ns
t_{OFF}	Active to Float	–	28	–	8.3 ¹	–	8.3 ¹	ns
t_{SU}	Input Set-Up Time to CLK—Bused Signals	7	–	1.5	–	1.5	–	ns

Table 34 • A40MX02 Timing Characteristics (Nominal 5.0 V Operation) (continued)
(Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
TTL Output Module Timing ⁴												
t _{DLH}	Data-to-Pad HIGH		3.3		3.8		4.3		5.1		7.2	ns
t _{DHL}	Data-to-Pad LOW		4.0		4.6		5.2		6.1		8.6	ns
t _{ENZH}	Enable Pad Z to HIGH		3.7		4.3		4.9		5.8		8.0	ns
t _{ENZL}	Enable Pad Z to LOW		4.7		5.4		6.1		7.2		10.1	ns
t _{ENHZ}	Enable Pad HIGH to Z		7.9		9.1		10.4		12.2		17.1	ns
t _{ENLZ}	Enable Pad LOW to Z		5.9		6.8		7.7		9.0		12.6	ns
d _{TLH}	Delta LOW to HIGH		0.02		0.02		0.03		0.03		0.04	ns/pF
d _{THL}	Delta HIGH to LOW		0.03		0.03		0.03		0.04		0.06	ns/pF
CMOS Output Module Timing ⁴												
t _{DLH}	Data-to-Pad HIGH		3.9		4.5		5.1		6.05		8.5	ns
t _{DHL}	Data-to-Pad LOW		3.4		3.9		4.4		5.2		7.3	ns
t _{ENZH}	Enable Pad Z to HIGH		3.4		3.9		4.4		5.2		7.3	ns
t _{ENZL}	Enable Pad Z to LOW		4.9		5.6		6.4		7.5		10.5	ns
t _{ENHZ}	Enable Pad HIGH to Z		7.9		9.1		10.4		12.2		17.0	ns
t _{ENLZ}	Enable Pad LOW to Z		5.9		6.8		7.7		9.0		12.6	ns
d _{TLH}	Delta LOW to HIGH		0.03		0.04		0.04		0.05		0.07	ns/pF
d _{THL}	Delta HIGH to LOW		0.02		0.02		0.03		0.03		0.04	ns/pF

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance
2. Set-up times assume fanout of 3. Further testing information can be obtained from the Timer utility
3. The hold time for the DFME1A macro may be greater than 0 ns. Use the Timer tool from the Designer software to check the hold time for this macro.
4. Delays based on 35pF loading

Table 35 • A40MX02 Timing Characteristics (Nominal 3.3 V Operation)
(Worst-Case Commercial Conditions, VCC = 3.0 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Logic Module Propagation Delays												
t _{PD1}	Single Module		1.7		2.0		2.3		2.7		3.7	ns
t _{PD2}	Dual-Module Macros		3.7		4.3		4.9		5.7		8.0	ns
t _{CO}	Sequential Clock-to-Q		1.7		2.0		2.3		2.7		3.7	ns
t _{GO}	Latch G-to-Q		1.7		2.0		2.3		2.7		3.7	ns
t _{RS}	Flip-Flop (Latch) Reset-to-Q		1.7		2.0		2.3		2.7		3.7	ns
Logic Module Predicted Routing Delays ¹												

Table 40 • A42MX16 Timing Characteristics (Nominal 5.0 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
TTL Output Module Timing ⁴												
t _{DLH}	Data-to-Pad HIGH	2.5		2.8		3.2		3.7		5.2		ns
t _{DHL}	Data-to-Pad LOW	3.0		3.3		3.7		4.4		6.1		ns
t _{ENZH}	Enable Pad Z to HIGH	2.7		3.0		3.4		4.0		5.6		ns
t _{ENZL}	Enable Pad Z to LOW	3.0		3.3		3.8		4.4		6.2		ns
t _{ENHZ}	Enable Pad HIGH to Z	5.4		6.0		6.8		8.0		11.2		ns
t _{ENLZ}	Enable Pad LOW to Z	5.0		5.6		6.3		7.4		10.4		ns
t _{GLH}	G-to-Pad HIGH	2.9		3.2		3.6		4.3		6.0		ns
t _{GHL}	G-to-Pad LOW	2.9		3.2		3.6		4.3		6.0		ns
t _{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading	5.7		6.3		7.1		8.4		11.9		ns
t _{ACO}	Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading	8.0		8.9		10.1		11.9		16.7		ns
d _{TLH}	Capacitive Loading, LOW to HIGH	0.03		0.03		0.03		0.04		0.06		ns/pF
d _{THL}	Capacitive Loading, HIGH to LOW	0.04		0.04		0.04		0.05		0.07		ns/pF

Table 43 • A42MX24 Timing Characteristics (Nominal 3.3 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)

Parameter / Description			–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
TTL Output Module Timing ⁵ (continued)													
t _{LH}	I/O Latch Output Hold		0.0		0.0		0.0		0.0		0.0		ns
t _{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O			7.7		8.5		9.6		11.3		15.9	ns
t _{ACO}	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O			14.8		16.5		18.7		22.0		30.8	ns
d _{TLH}	Capacitive Loading, LOW to HIGH			0.05		0.05		0.06		0.07		0.10	ns/pF
d _{THL}	Capacitive Loading, HIGH to LOW			0.04		0.04		0.05		0.06		0.08	ns/pF
CMOS Output Module Timing ⁵													
t _{DLH}	Data-to-Pad HIGH			4.8		5.3		5.5		6.4		9.0	ns
t _{DHL}	Data-to-Pad LOW			3.5		3.9		4.1		4.9		6.8	ns
t _{ENZH}	Enable Pad Z to HIGH			3.6		4.0		4.5		5.3		7.4	ns
t _{ENZL}	Enable Pad Z to LOW			3.4		4.0		5.0		5.8		8.2	ns
t _{ENHZ}	Enable Pad HIGH to Z			7.2		8.0		9.0		10.7		14.9	ns
t _{ENLZ}	Enable Pad LOW to Z			6.7		7.5		8.5		9.9		13.9	ns
t _{GLH}	G-to-Pad HIGH			6.8		7.6		8.6		10.1		14.2	ns
t _{GHL}	G-to-Pad LOW			6.8		7.6		8.6		10.1		14.2	ns
t _{LSU}	I/O Latch Set-Up		0.7		0.7		0.8		1.0		1.4		ns
t _{LH}	I/O Latch Hold		0.0		0.0		0.0		0.0		0.0		ns
t _{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O			7.7		8.5		9.6		11.3		15.9	ns
t _{ACO}	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O			14.8		16.5		18.7		22.0		30.8	ns
d _{TLH}	Capacitive Loading, LOW to HIGH			0.05		0.05		0.06		0.07		0.10	ns/pF
d _{THL}	Capacitive Loading, HIGH to LOW			0.04		0.04		0.05		0.06		0.08	ns/pF
t _{HEXT}	Input Latch External Hold	FO = 32	3.9		4.3		4.9		5.7		8.1		ns
		FO = 486	4.6		5.2		5.8		6.9		9.6		ns
t _P	Minimum Period (1/f _{MAX})	FO = 32	7.8		8.7		9.5		10.8		18.2		ns
		FO = 486	8.6		9.5		10.4		11.9		19.9		ns

1. For dual-module macros, use t_{PD1} + t_{RD1} + t_{PDn}, t_{CO} + t_{RD1} + t_{PDn}, or t_{PD1} + t_{RD1} + t_{SUD}, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
4. Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.
5. Delays based on 35 pF loading.

Table 45 • A42MX36 Timing Characteristics (Nominal 3.3 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)

Parameter / Description			–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Input Module Predicted Routing Delays ²													
t _{IRD1}	FO = 1 Routing Delay		2.8		3.1		3.5		4.1		5.7		ns
t _{IRD2}	FO = 2 Routing Delay		3.2		3.5		4.1		4.8		6.7		ns
t _{IRD3}	FO = 3 Routing Delay		3.7		4.1		4.7		5.5		7.7		ns
t _{IRD4}	FO = 4 Routing Delay		4.2		4.6		5.3		6.2		8.7		ns
t _{IRD8}	FO = 8 Routing Delay		6.1		6.8		7.7		9.0		12.6		ns
Global Clock Network													
t _{CKH}	Input LOW to HIGH	FO = 32	4.6		5.1		5.7		6.7		9.3		ns
		FO = 635	5.0		5.6		6.3		7.4		10.3		ns
t _{CKL}	Input HIGH to LOW	FO = 32	5.3		5.9		6.7		7.8		11.0		ns
		FO = 635	6.8		7.6		8.6		10.1		14.1		ns
t _{PWH}	Minimum Pulse Width HIGH	FO = 32	2.5		2.7		3.1		3.6		5.1		ns
		FO = 635	2.8		3.1		3.5		4.1		5.7		ns
t _{PWL}	Minimum Pulse Width LOW	FO = 32	2.5		2.7		3.1		3.6		5.1		ns
		FO = 635	2.8		3.1		3.5		4.1		5.7		ns
t _{CKSW}	Maximum Skew	FO = 32	1.0		1.2		1.3		1.5		2.2		ns
		FO = 635	1.0		1.2		1.3		1.5		2.2		ns
t _{SUEXT}	Input Latch External Set-Up	FO = 32	0.0		0.0		0.0		0.0		0.0		ns
		FO = 635	0.0		0.0		0.0		0.0		0.0		ns
t _{HEXT}	Input Latch External Hold	FO = 32	4.0		4.4		5.0		5.9		8.2		ns
		FO = 635	4.6		5.2		5.9		6.9		9.6		ns
t _P	Minimum Period (1/f _{MAX})	FO = 32	9.2		10.2		11.1		12.7		21.2		ns
		FO = 635	9.9		11.0		12.0		13.8		23.0		ns
f _{MAX}	Maximum Datapath Frequency	FO = 32	108		98		90		79		47		MHz
		FO = 635	100		91		83		73		44		MHz
TTL Output Module Timing ⁵													
t _{DLH}	Data-to-Pad HIGH		3.6		4.0		4.5		5.3		7.4		ns
t _{DHL}	Data-to-Pad LOW		4.2		4.6		5.2		6.2		8.6		ns
t _{ENZH}	Enable Pad Z to HIGH		3.7		4.2		4.7		5.5		7.7		ns
t _{ENZL}	Enable Pad Z to LOW		4.1		4.6		5.2		6.1		8.5		ns
t _{ENHZ}	Enable Pad HIGH to Z		7.34		8.2		9.3		10.9		15.3		ns
TTL Output Module Timing ⁵													
t _{ENLZ}	Enable Pad LOW to Z		6.9		7.6		8.7		10.2		14.3		ns
t _{GLH}	G-to-Pad HIGH		4.9		5.5		6.2		7.3		10.2		ns
t _{GHL}	G-to-Pad LOW		4.9		5.5		6.2		7.3		10.2		ns
t _{LSU}	I/O Latch Output Set-Up		0.7		0.7		0.8		1.0		1.4		ns
t _{LH}	I/O Latch Output Hold		0.0		0.0		0.0		0.0		0.0		ns
t _{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		7.9		8.8		10.0		11.8		16.5		ns

Table 51 • PQ144

PQ144	
Pin Number	A42MX09 Function
117	GNDI
118	NC
119	I/O
120	I/O
121	I/O
122	I/O
123	PROBA
124	I/O
125	CLKA
126	VCC
127	VCCI
128	NC
129	I/O
130	CLKB
131	I/O
132	PROBB
133	I/O
134	I/O
135	I/O
136	GND
137	GNDI
138	NC
139	I/O
140	I/O
141	I/O
142	I/O
143	I/O
144	DCLK

Figure 44 • PQ208

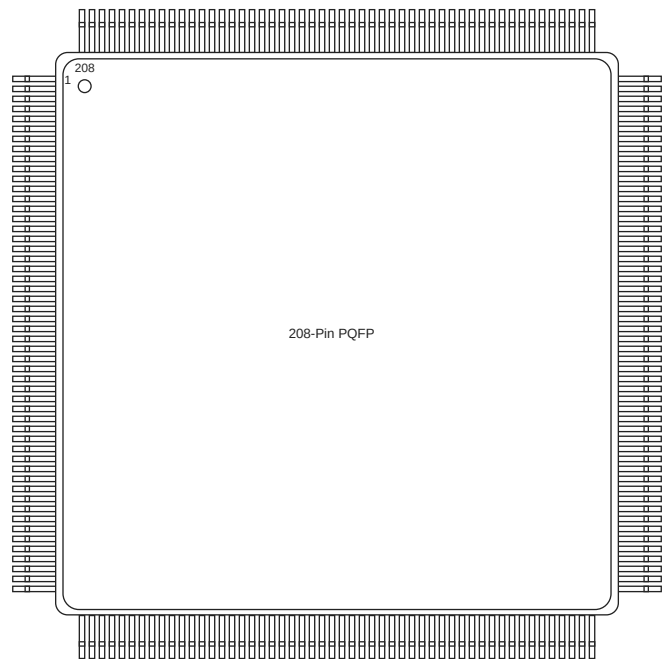


Table 53 • PQ208

PQ208			
Pin Number	A42MX16 Function	A42MX24 Function	A42MX36 Function
1	GND	GND	GND
2	NC	VCCA	VCCA
3	MODE	MODE	MODE
4	I/O	I/O	I/O
5	I/O	I/O	I/O
6	I/O	I/O	I/O
7	I/O	I/O	I/O
8	I/O	I/O	I/O
9	NC	I/O	I/O
10	NC	I/O	I/O
11	NC	I/O	I/O
12	I/O	I/O	I/O
13	I/O	I/O	I/O
14	I/O	I/O	I/O
15	I/O	I/O	I/O
16	NC	I/O	I/O
17	VCCA	VCCA	VCCA
18	I/O	I/O	I/O
19	I/O	I/O	I/O
20	I/O	I/O	I/O

Table 56 • VQ100

VQ100		
Pin Number	A42MX09 Function	A42MX16 Function
21	I/O	I/O
22	I/O	I/O
23	I/O	I/O
24	I/O	I/O
25	I/O	I/O
26	I/O	I/O
27	I/O	I/O
28	I/O	I/O
29	I/O	I/O
30	I/O	I/O
31	I/O	I/O
32	GND	GND
33	I/O	I/O
34	I/O	I/O
35	I/O	I/O
36	I/O	I/O
37	I/O	I/O
38	VCCA	VCCA
39	I/O	I/O
40	I/O	I/O
41	I/O	I/O
42	I/O	I/O
43	I/O	I/O
44	GND	GND
45	I/O	I/O
46	I/O	I/O
47	I/O	I/O
48	I/O	I/O
49	I/O	I/O
50	SDO, I/O	SDO, I/O
51	I/O	I/O
52	I/O	I/O
53	I/O	I/O
54	I/O	I/O
55	GND	GND
56	I/O	I/O

Table 56 • VQ100

VQ100		
Pin Number	A42MX09 Function	A42MX16 Function
57	I/O	I/O
58	I/O	I/O
59	I/O	I/O
60	I/O	I/O
61	I/O	I/O
62	LP	LP
63	VCCA	VCCA
64	VCCI	VCCI
65	VCCA	VCCA
66	I/O	I/O
67	I/O	I/O
68	I/O	I/O
69	I/O	I/O
70	GND	GND
71	I/O	I/O
72	I/O	I/O
73	I/O	I/O
74	I/O	I/O
75	I/O	I/O
76	I/O	I/O
77	SDI, I/O	SDI, I/O
78	I/O	I/O
79	I/O	I/O
80	I/O	I/O
81	I/O	I/O
82	GND	GND
83	I/O	I/O
84	I/O	I/O
85	PRA, I/O	PRA, I/O
86	I/O	I/O
87	CLKA, I/O	CLKA, I/O
88	VCCA	VCCA
89	I/O	I/O
90	CLKB, I/O	CLKB, I/O
91	I/O	I/O
92	PRB, I/O	PRB, I/O

Table 58 • CQ208

CQ208	
Pin Number	A42MX36 Function
148	I/O
149	I/O
150	GND
151	I/O
152	I/O
153	I/O
154	I/O
155	I/O
156	I/O
157	GND
158	I/O
159	SDI, I/O
160	I/O
161	WD, I/O
162	WD, I/O
163	I/O
164	VCCI
165	I/O
166	I/O
167	I/O
168	WD, I/O
169	WD, I/O
170	I/O
171	QCLKD, I/O
172	I/O
173	I/O
174	I/O
175	I/O
176	WD, I/O
177	WD, I/O
178	PRA, I/O
179	I/O
180	CLKA, I/O
181	I/O
182	VCCI
183	VCCA
184	GND

Table 59 • CQ256

CQ256	
Pin Number	A42MX36 Function
22	I/O
23	I/O
24	I/O
25	I/O
26	VCCA
27	I/O
28	I/O
29	VCCA
30	VCCI
31	GND
32	VCCA
33	LP
34	TCK, I/O
35	I/O
36	GND
37	I/O
38	I/O
39	I/O
40	I/O
41	I/O
42	I/O
43	I/O
44	I/O
45	I/O
46	I/O
47	I/O
48	GND
49	I/O
50	I/O
51	I/O
52	I/O
53	I/O
54	I/O
55	I/O
56	I/O
57	I/O
58	I/O

Table 59 • CQ256

CQ256	
Pin Number	A42MX36 Function
170	VCCA
171	I/O
172	I/O
173	I/O
174	I/O
175	I/O
176	I/O
177	I/O
178	I/O
179	I/O
180	GND
181	I/O
182	I/O
183	I/O
184	I/O
185	I/O
186	I/O
187	I/O
188	MODE
189	VCCA
190	GND
191	NC
192	NC
193	NC
194	I/O
195	DCLK, I/O
196	I/O
197	I/O
198	I/O
199	WD, I/O
200	WD, I/O
201	VCCI
202	I/O
203	I/O
204	I/O
205	I/O
206	GND

Table 60 • BG272

BG272	
Pin Number	A42MX36 Function
D20	I/O
E1	I/O
E2	I/O
E3	I/O
E4	VCCA
E17	VCCI
E18	I/O
E19	I/O
E20	I/O
F1	I/O
F2	I/O
F3	I/O
F4	VCCI
F17	I/O
F18	I/O
F19	I/O
F20	I/O
G1	I/O
G2	I/O
G3	I/O
G4	VCCI
G17	VCCI
G18	I/O
G19	I/O
G20	I/O
H1	I/O
H2	I/O
H3	I/O
H4	VCCA
H17	I/O
H18	I/O
H19	I/O
H20	I/O
J1	I/O
J2	I/O
J3	I/O
J4	VCCI

Table 60 • BG272

BG272	
Pin Number	A42MX36 Function
M10	GND
M11	GND
M12	GND
M17	I/O
M18	I/O
M19	I/O
M20	I/O
N1	I/O
N2	I/O
N3	I/O
N4	VCCI
N17	VCCI
N18	I/O
N19	I/O
N20	I/O
P1	I/O
P2	I/O
P3	I/O
P4	VCCA
P17	I/O
P18	I/O
P19	I/O
P20	I/O
R1	I/O
R2	I/O
R3	I/O
R4	VCCI
R17	VCCI
R18	I/O
R19	I/O
R20	I/O
T1	I/O
T2	I/O
T3	I/O
T4	I/O
T17	VCCA
T18	I/O

Table 60 • BG272

BG272	
Pin Number	A42MX36 Function
V16	I/O
V17	I/O
V18	SDO, TDO, I/O
V19	I/O
V20	I/O
W1	GND
W2	GND
W3	I/O
W4	TMS, I/O
W5	I/O
W6	I/O
W7	I/O
W8	WD, I/O
W9	WD, I/O
W10	I/O
W11	I/O
W12	I/O
W13	WD, I/O
W14	I/O
W15	I/O
W16	WD, I/O
W17	I/O
W18	WD, I/O
W19	GND
W20	GND
Y1	GND
Y2	GND
Y3	I/O
Y4	TDI, I/O
Y5	WD, I/O
Y6	I/O
Y7	QCLKA, I/O
Y8	I/O
Y9	I/O
Y10	I/O
Y11	I/O
Y12	I/O

Table 62 • CQ172

138	I/O
139	I/O
140	I/O
141	GND
142	I/O
143	I/O
144	I/O
145	I/O
146	I/O
147	I/O
148	PROBA
149	I/O
150	CLKA
151	VCC
152	GND
153	I/O
154	CLKB
155	I/O
156	PROBB
157	I/O
158	I/O
159	I/O
160	I/O
161	GND
162	I/O
163	I/O
164	I/O
165	I/O
166	VCCI
167	I/O
168	I/O
169	I/O
170	I/O
171	DCLK