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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | - |
| Number of I/O | 57 |
| Number of Gates | 3000 |
| Voltage - Supply | 3V ~ 3.6V, 4.5V ~ 5.5V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Package / Case | 100-BQFP |
| Supplier Device Package | 100-PQFP (20x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/a40mx02-1pqg100i |

## 2.3 Ordering Information

The following figure shows ordering information.All the following tables show plastic and ceramic device resources, temperature and speed grade offerings.

***Figure 1 •*** **Ordering Information**

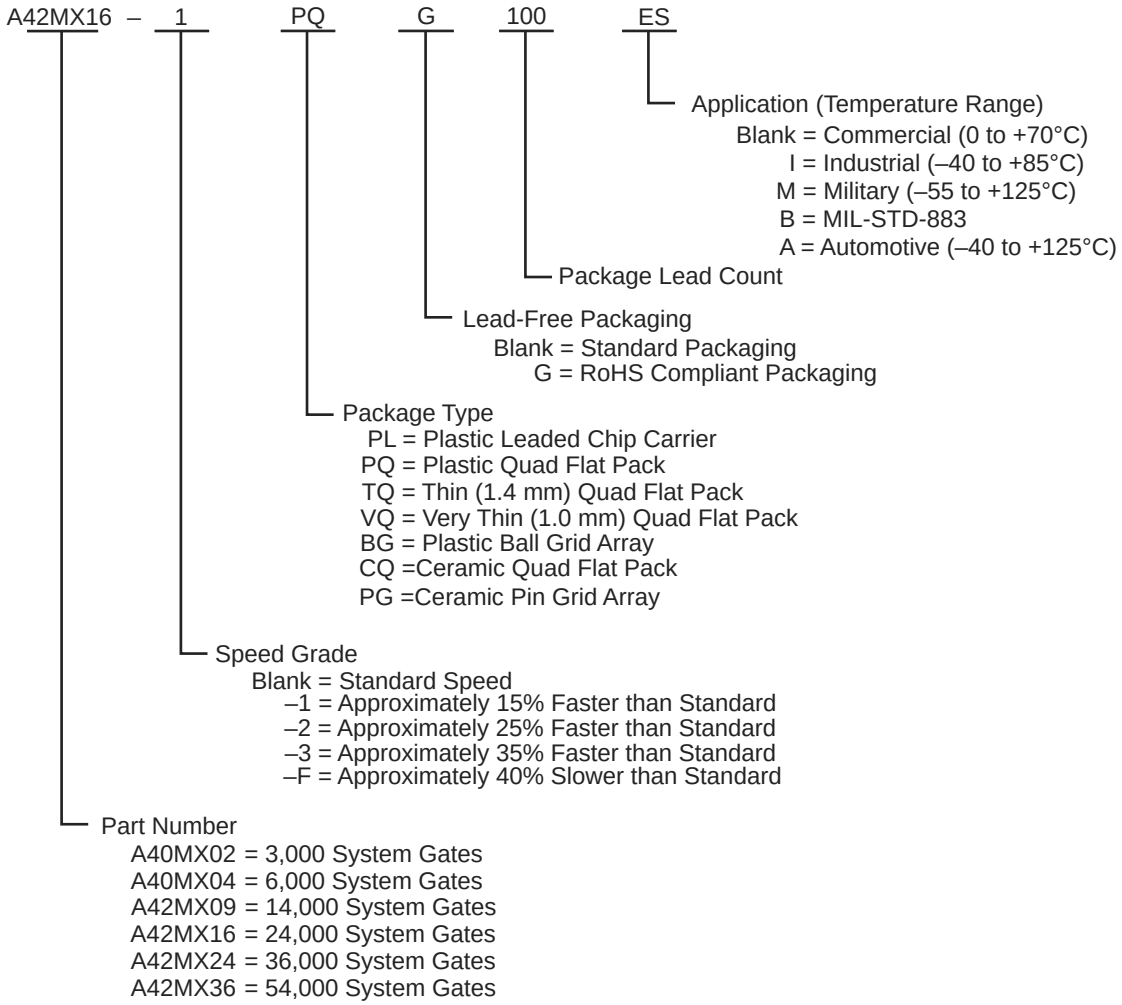
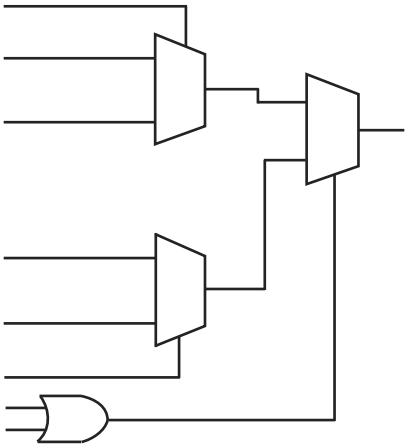


***Figure 2 •*** **42MX C-Module Implementation**



The 42MX devices contain three types of logic modules: combinatorial (C-modules), sequential (S-modules) and decode (D-modules). The following figure illustrates the combinatorial logic module. The S-module, shown in Figure 4, page 8, implements the same combinatorial logic function as the C-module while adding a sequential element. The sequential element can be configured as either a D-flip-flop or a transparent latch. The S-module register can be bypassed so that it implements purely combinatorial logic.

***Figure 3 •*** **42MX C-Module Implementation**

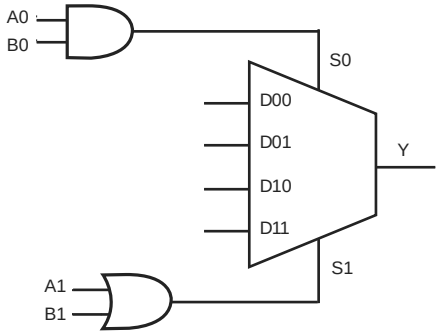
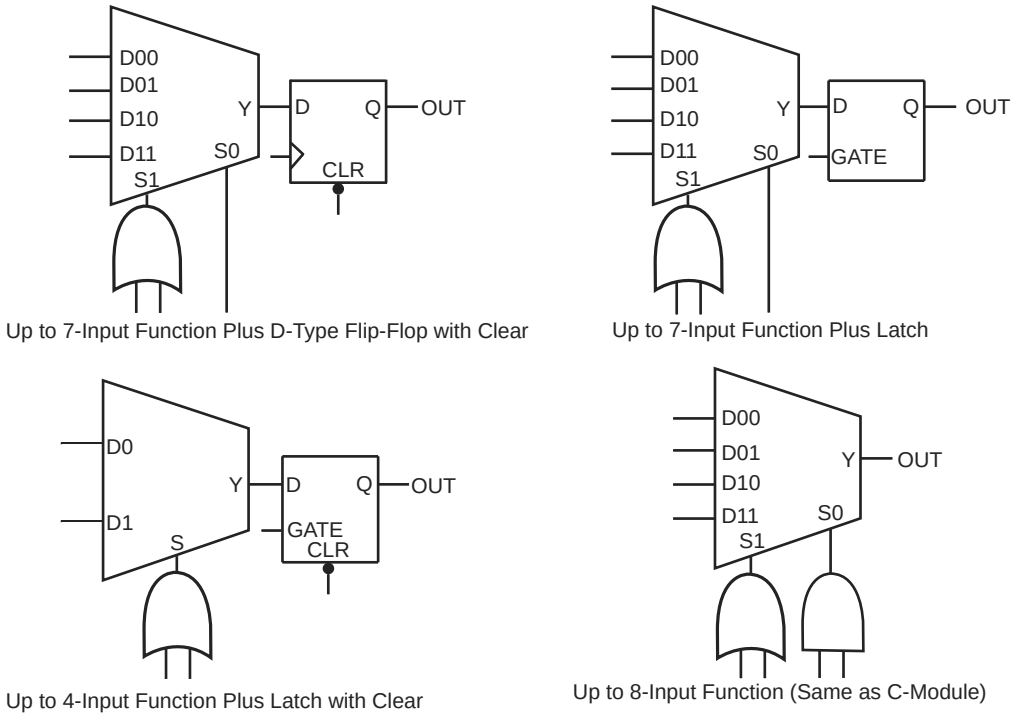


***Figure 4 •*** **42MX S-Module Implementation**




A42MX24 and A42MX36 devices contain D-modules, which are arranged around the periphery of the device. D-modules contain wide-decode circuitry, providing a fast, wide-input AND function similar to that found in CPLD architectures (Figure 5, page 9). The D-module allows A42MX24 and A42MX36 devices to perform wide-decode functions at speeds comparable to CPLDs and PALs. The output of the D-module has a programmable inverter for active HIGH or LOW assertion. The D-module output is hardwired to an output pin, and can also be fed back into the array to be incorporated into other logic.

## 3.2.2 Dual-Port SRAM Modules

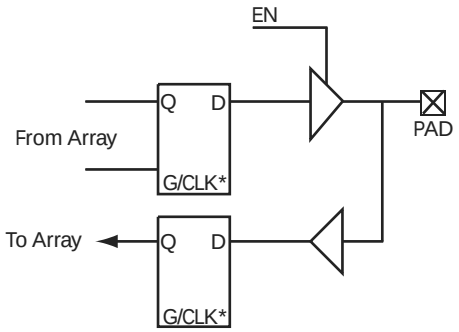
The A42MX36 device contains dual-port SRAM modules that have been optimized for synchronous or asynchronous applications. The SRAM modules are arranged in 256-bit blocks that can be configured as 32x8 or 64x4. SRAM modules can be cascaded together to form memory spaces of user-definable width and depth. A block diagram of the A42MX36 dual-port SRAM block is shown in Figure 6, page 9.

The A42MX36 SRAM modules are true dual-port structures containing independent read and write ports. Each SRAM module contains six bits of read and write addressing (RDAD[5:0] and WRAD[5:0], respectively) for 64x4-bit blocks. When configured in byte mode, the highest order address bits (RDAD5 and WRAD5) are not used. The read and write ports of the SRAM block contain independent clocks (RCLK and WCLK) with programmable polarities offering active HIGH or LOW implementation. The SRAM block contains eight data inputs (WD[7:0]), and eight outputs (RD[7:0]), which are connected to segmented vertical routing tracks.

The A42MX36 dual-port SRAM blocks provide an optimal solution for high-speed buffered applications requiring FIFO and LIFO queues. The ACTgen Macro Builder within Microsemi's designer software provides capability to quickly design memory functions with the SRAM blocks. Unused SRAM blocks can be used to implement registers for other user logic within the design.

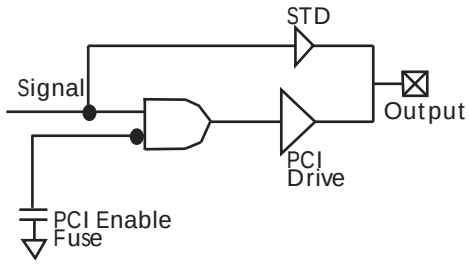
Designer software development tools provide a design library of I/O macro functions that can implement all I/O configurations supported by the MX FPGAs.

***Figure 10 •*** **42MX I/O Module**




***Note:*** **Can be configured as a Latch or D Flip-Flop (Using C-Module)*

***Figure 11 •*** **PCI Output Structure of A42MX24 and A42MX36 Devices**




# 3.3 Other Architectural Features

The following sections cover other architectural features of 40MX and 42MX FPGAs.

## 3.3.1 Performance

MX devices can operate with internal clock frequencies of 250 MHz, enabling fast execution of complex logic functions. MX devices are live on power-up and do not require auxiliary configuration devices and thus are an optimal platform to integrate the functionality contained in multiple programmable logic devices. In addition, designs that previously would have required a gate array to meet performance can be integrated into an MX device with improvements in cost and time-to-market. Using timing-driven place-and-route (TDPR) tools, designers can achieve highly deterministic device performance.

## 3.3.2 User Security

Microsemi FuseLock provides robust security against design theft. Special security fuses are hidden in the fabric of the device and protect against unauthorized users attempting to access the programming and/or probe interfaces. It is virtually impossible to identify or bypass these fuses without damaging the device, making Microsemi antifuse FPGAs protected with the highest level of security available from both invasive and noninvasive attacks.

Special security fuses in 40MX devices include the Probe Fuse and Program Fuse. The former disables the probing circuitry while the latter prohibits further programming of all fuses, including the Probe Fuse. In 42MX devices, there is the Security Fuse which, when programmed, both disables the probing circuitry and prohibits further programming of the device.

## 3.3.3 Programming

Device programming is supported through the Silicon Sculptor series of programmers. Silicon Sculptor is a compact, robust, single-site and multi-site device programmer for the PC. With standalone software, Silicon Sculptor is designed to allow concurrent programming of multiple units from the same PC.

### 3.4.9 JTAG Mode Activation

The JTAG test logic circuit is activated in the Designer software by selecting **Tools > Device Selection**. This brings up the Device Selection dialog box as shown in the following figure. The JTAG test logic circuit can be enabled by clicking the “Reserve JTAG Pins” check box. The following table explains the pins' behavior in either mode.

***Figure 15 •*** **Device Selection Wizard**

***Table 11 •*** **Boundary Scan Pin Configuration and Functionality**

| Reserve JTAG | Checked | Unchecked |
|---|---|---|
| TCK | BST input; must be terminated to logical HIGH or LOW to avoid floating | User I/O |
| TDI, TMS | BST input; may float or be tied to HIGH | User I/O |
| TDO | BST output; may float or be connected to TDI of another device | User I/O |

### 3.4.10 TRST Pin and TAP Controller Reset

An active reset (TRST) pin is not supported; however, MX devices contain power-on circuitry that resets the boundary scan circuitry upon power-up. Also, the TMS pin is equipped with an internal pull-up resistor. This allows the TAP controller to remain in or return to the Test-Logic-Reset state when there is no input or when a logical 1 is on the TMS pin. To reset the controller, TMS must be HIGH for at least five TCK cycles.

### 3.4.11 Boundary Scan Description Language (BSDL) File

Conforming to the IEEE Standard 1149.1 requires that the operation of the various JTAG components be documented. The BSDL file provides the standard format to describe the JTAG components that can be used by automatic test equipment software. The file includes the instructions that are supported, instruction bit pattern, and the boundary-scan chain order. For an in-depth discussion on BSDL files, see the *BSDL Files Format Description* application note.

BSDL files are grouped into two categories - generic and device-specific. The generic files assign all user I/Os as inouts. Device-specific files assign user I/Os as inputs, outputs or inouts.

Generic files for MX devices are available on the Microsemi SoC Product Group's website:

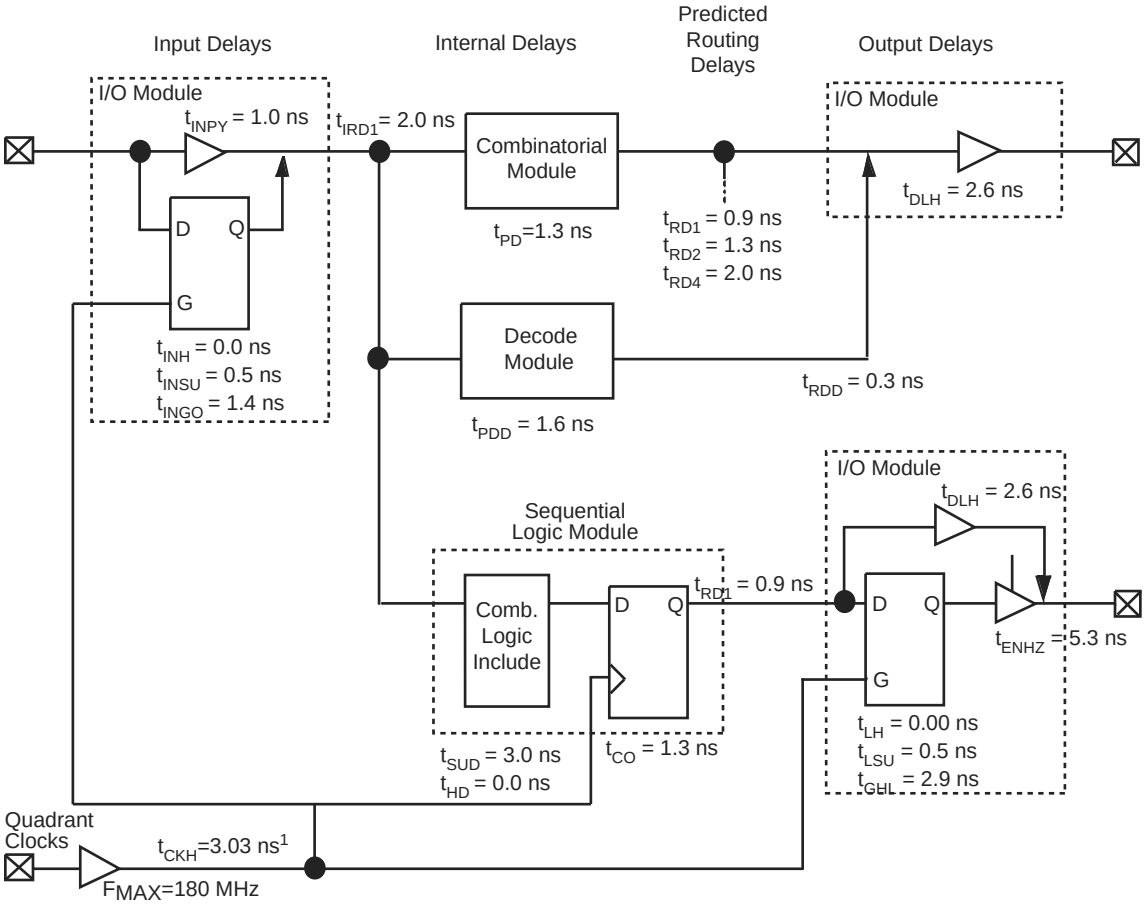
http://www.microsemi.com/soc/techdocs/models/bsdl.html.

## 3.5 Development Tool Support

The MX family of FPGAs is fully supported by Libero® Integrated Design Environment (IDE). Libero IDE is a design management environment, seamlessly integrating design tools while guiding the user through the design flow, managing all design and log files, and passing necessary design data among tools. Libero IDE allows users to integrate both schematic and HDL synthesis into a single flow and verify the entire design in a single environment. Libero IDE includes SynplifyPro from Synopsys, ModelSim® HDL Simulator from Mentor Graphics® and Viewdraw.

Libero IDE includes place-and-route and provides a comprehensive suite of backend support tools for FPGA development, including timing-driven place-and-route, and a world-class integrated static timing analyzer and constraints editor.

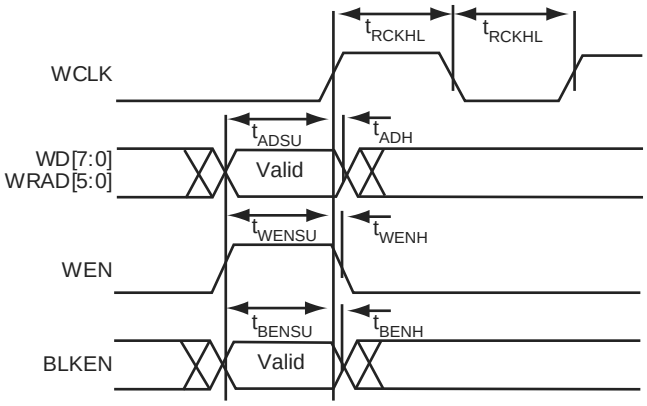
***Figure 19 •*** **42MX Timing Model (Logic Functions Using Quadrant Clocks)**




**Note:** 1. Load-dependent

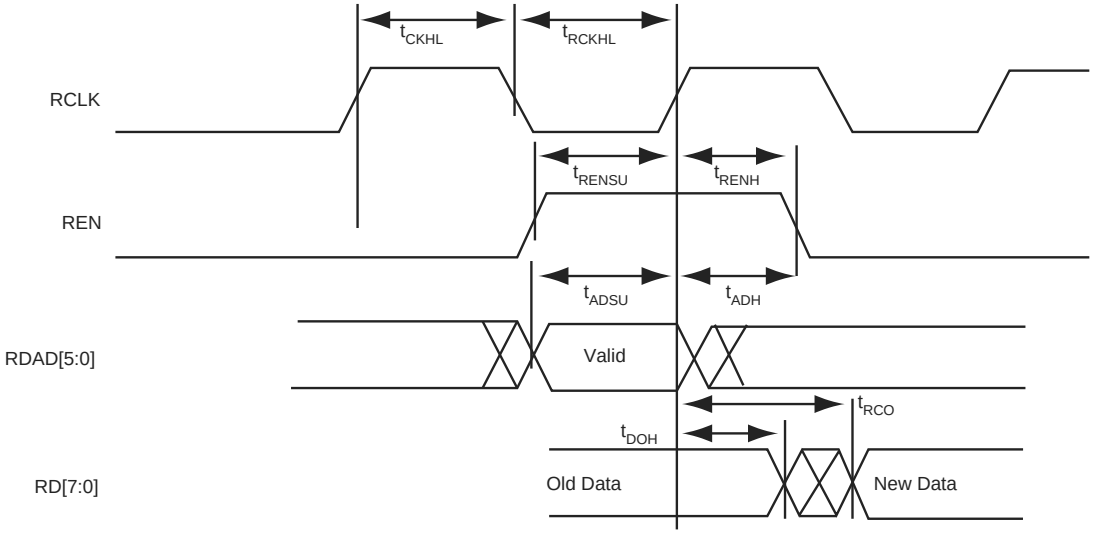
**Note:** 2. Values are shown for A42MX36 –3 at 5.0 V worst-case commercial conditions

***Figure 30 •*** **42MX SRAM Write Operation**




**Note:** Identical timing for falling edge clock

***Figure 31 •*** **42MX SRAM Synchronous Read Operation**




**Note:** Identical timing for falling edge clock

***Figure 32 •*** **42MX SRAM Asynchronous Read Operation—Type 1 (Read Address Controlled)**

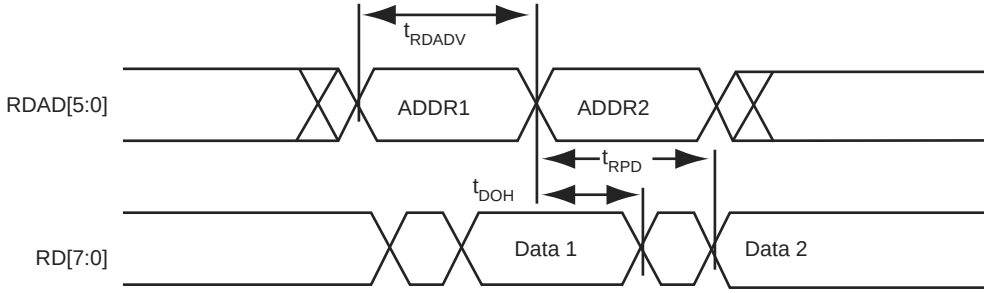
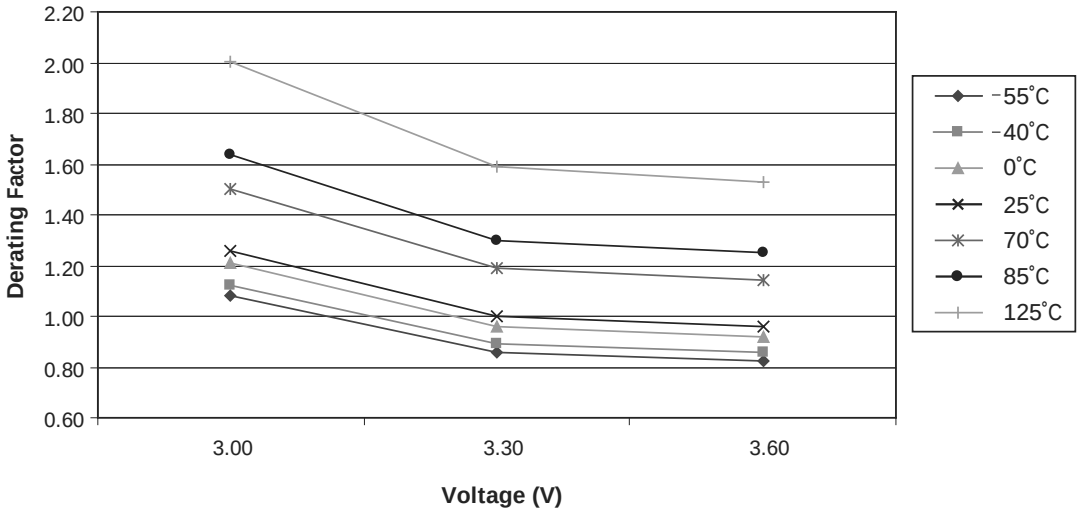


***Table 31 •*** **40MX Temperature and Voltage Derating Factors (Normalized to TJ = 25°C, VCC = 3.3 V)**

| | Temperature | | | | | | |
|---|---|---|---|---|---|---|---|
| **40MX Voltage** | **–55°C** | **–40°C** | **0°C** | **25°C** | **70°C** | **85°C** | **125°C** |
| 3.60 | 0.83 | 0.85 | 0.92 | 0.96 | 1.14 | 1.25 | 1.53 |

***Figure 37 •*** **40MX Junction Temperature and Voltage Derating Curves (Normalized to TJ = 25°C, VCC = 3.3 V)**




**Note:** This derating factor applies to all routing and propagation delays

## 3.11.5 PCI System Timing Specification

The following tables list the critical PCI timing parameters and the corresponding timing parameters for the MX PCI-compliant devices.

## 3.11.6 PCI Models

Microsemi provides synthesizable VHDL and Verilog-HDL models for a PCI Target interface, a PCI Target and Target+DMA Master interface. Contact the Microsemi sales representative for more details.

***Table 32 •*** **Clock Specification for 33 MHz PCI**

| | | PCI | | A42MX24 | | A42MX36 | | |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| $t_{CYC}$ | CLK Cycle Time | 30 | – | 4.0 | – | 4.0 | – | ns |
| $t_{HIGH}$ | CLK High Time | 11 | – | 1.9 | – | 1.9 | – | ns |
| $t_{LOW}$ | CLK Low Time | 11 | – | 1.9 | – | 1.9 | – | ns |

***Table 33 •*** **Timing Parameters for 33 MHz PCI**

| | | PCI | | A42MX24 | | A42MX36 | | |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| $t_{VAL}$ | CLK to Signal Valid—Bused Signals | 2 | 11 | 2.0 | 9.0 | 2.0 | 9.0 | ns |
| $t_{VAL(PTP)}$ | CLK to Signal Valid—Point-to-Point | 2 [2] | 12 | 2.0 | 9.0 | 2.0 | 9.0 | ns |
| $t_{ON}$ | Float to Active | 2 | – | 2.0 | 4.0 | 2.0 | 4.0 | ns |
| $t_{OFF}$ | Active to Float | – | 28 | – | 8.3[1] | – | 8.3[1] | ns |
| $t_{SU}$ | Input Set-Up Time to CLK—Bused Signals | 7 | – | 1.5 | – | 1.5 | – | ns |

***Table 36 •*** **A40MX04 Timing Characteristics (Nominal 5.0 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCC = 4.75 V, $T_J$ = 70°C)**

| Parameter / Description | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **CMOS Output Module Timing[1]** | | | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad HIGH | | 3.9 | | 4.5 | | 5.1 | | 6.05 | | 8.5 | ns |
| $t_{DHL}$ | Data-to-Pad LOW | | 3.4 | | 3.9 | | 4.4 | | 5.2 | | 7.3 | ns |
| $t_{ENZH}$ | Enable Pad Z to HIGH | | 3.4 | | 3.9 | | 4.4 | | 5.2 | | 7.3 | ns |
| $t_{ENZL}$ | Enable Pad Z to LOW | | 4.9 | | 5.6 | | 6.4 | | 7.5 | | 10.5 | ns |
| $t_{ENHZ}$ | Enable Pad HIGH to Z | | 7.9 | | 9.1 | | 10.4 | | 12.2 | | 17.0 | ns |
| $t_{ENLZ}$ | Enable Pad LOW to Z | | 5.9 | | 6.8 | | 7.7 | | 9.0 | | 12.6 | ns |
| $d_{TLH}$ | Delta LOW to HIGH | | 0.03 | | 0.04 | | 0.04 | | 0.05 | | 0.07 | ns/pF |
| $d_{THL}$ | Delta HIGH to LOW | | 0.02 | | 0.02 | | 0.03 | | 0.03 | | 0.04 | ns/pF |

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*
2. Set-up times assume fanout of 3. Further testing information can be obtained from the Timer utility
3. The hold time for the DFME1A macro may be greater than 0 ns. Use the Timer utility from the Designer software to check the hold time for this macro.
4. Delays based on 35 pF loading

***Table 37 •*** **A40MX04 Timing Characteristics (Nominal 3.3 V Operation) (Worst-Case Commercial Conditions, VCC = 3.0 V, $T_J$ = 70°C)**

| Parameter / Description | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Logic Module Propagation Delays** | | | | | | | | | | | | |
| $t_{PD1}$ | Single Module | | 1.7 | | 2.0 | | 2.3 | | 2.7 | | 3.7 | ns |
| $t_{PD2}$ | Dual-Module Macros | | 3.7 | | 4.3 | | 4.9 | | 5.7 | | 8.0 | ns |
| $t_{CO}$ | Sequential Clock-to-Q | | 1.7 | | 2.0 | | 2.3 | | 2.7 | | 3.7 | ns |
| $t_{GO}$ | Latch G-to-Q | | 1.7 | | 2.0 | | 2.3 | | 2.7 | | 3.7 | ns |
| $t_{RS}$ | Flip-Flop (Latch) Reset-to-Q | | 1.7 | | 2.0 | | 2.3 | | 2.7 | | 3.7 | ns |
| **Logic Module Predicted Routing Delays[1]** | | | | | | | | | | | | |
| $t_{RD1}$ | FO = 1 Routing Delay | | 1.9 | | 2.2 | | 2.5 | | 3.0 | | 4.2 | ns |
| $t_{RD2}$ | FO = 2 Routing Delay | | 2.7 | | 3.1 | | 3.5 | | 4.1 | | 5.7 | ns |
| $t_{RD3}$ | FO = 3 Routing Delay | | 3.4 | | 3.9 | | 4.4 | | 5.2 | | 7.3 | ns |
| $t_{RD4}$ | FO = 4 Routing Delay | | 4.1 | | 4.8 | | 5.4 | | 6.3 | | 8.9 | ns |
| $t_{RD8}$ | FO = 8 Routing Delay | | 7.1 | | 8.1 | | 9.2 | | 10.9 | | 15.2 | ns |
| **Logic Module Sequential Timing[2]** | | | | | | | | | | | | |
| $t_{SUD}$ | Flip-Flop (Latch) Data Input Set-Up | 4.3 | | 5.0 | | 5.6 | | 6.6 | | 9.2 | | ns |
| $t_{HD}$[3] | Flip-Flop (Latch) Data Input Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{SUENA}$ | Flip-Flop (Latch) Enable Set-Up | 4.3 | | 5.0 | | 5.6 | | 6.6 | | 9.2 | | ns |
| $t_{HENA}$ | Flip-Flop (Latch) Enable Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |

***Table 40 •*** **A42MX16 Timing Characteristics (Nominal 5.0 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 4.75 V, $T_J$ = 70°C)**

| Parameter / Description | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **TTL Output Module Timing[4]** | | | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad HIGH | | 2.5 | | 2.8 | | 3.2 | | 3.7 | | 5.2 | ns |
| $t_{DHL}$ | Data-to-Pad LOW | | 3.0 | | 3.3 | | 3.7 | | 4.4 | | 6.1 | ns |
| $t_{ENZH}$ | Enable Pad Z to HIGH | | 2.7 | | 3.0 | | 3.4 | | 4.0 | | 5.6 | ns |
| $t_{ENZL}$ | Enable Pad Z to LOW | | 3.0 | | 3.3 | | 3.8 | | 4.4 | | 6.2 | ns |
| $t_{ENHZ}$ | Enable Pad HIGH to Z | | 5.4 | | 6.0 | | 6.8 | | 8.0 | | 11.2 | ns |
| $t_{ENLZ}$ | Enable Pad LOW to Z | | 5.0 | | 5.6 | | 6.3 | | 7.4 | | 10.4 | ns |
| $t_{GLH}$ | G-to-Pad HIGH | | 2.9 | | 3.2 | | 3.6 | | 4.3 | | 6.0 | ns |
| $t_{GHL}$ | G-to-Pad LOW | | 2.9 | | 3.2 | | 3.6 | | 4.3 | | 6.0 | ns |
| $t_{LCO}$ | I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading | | 5.7 | | 6.3 | | 7.1 | | 8.4 | | 11.9 | ns |
| $t_{ACO}$ | Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading | | 8.0 | | 8.9 | | 10.1 | | 11.9 | | 16.7 | ns |
| $d_{TLH}$ | Capacitive Loading, LOW to HIGH | | 0.03 | | 0.03 | | 0.03 | | 0.04 | | 0.06 | ns/pF |
| $d_{THL}$ | Capacitive Loading, HIGH to LOW | | 0.04 | | 0.04 | | 0.04 | | 0.05 | | 0.07 | ns/pF |

***Table 43 •*** **A42MX24 Timing Characteristics (Nominal 3.3 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 3.0 V, $T_J$ = 70°C)**

| | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter / Description** | | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| **Logic Module Sequential Timing[3, 4]** | | | | | | | | | | | | |
| $t_{CO}$ | Flip-Flop Clock-to-Output | | 2.1 | | 2.0 | | 2.3 | | 2.7 | | 3.7 | ns |
| $t_{GO}$ | Latch Gate-to-Output | | 3.4 | | 1.9 | | 2.1 | | 2.5 | | 3.4 | ns |
| $t_{SUD}$ | Flip-Flop (Latch) Set-Up Time | 0.4 | | 0.5 | | 0.6 | | 0.7 | | 0.9 | | ns |
| $t_{HD}$ | Flip-Flop (Latch) Hold Time | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{RO}$ | Flip-Flop (Latch) Reset-to-Output | | 2.0 | | 2.2 | | 2.5 | | 2.9 | | 4.1 | ns |
| $t_{SUENA}$ | Flip-Flop (Latch) Enable Set-Up | 0.6 | | 0.6 | | 0.7 | | 0.8 | | 1.2 | | ns |
| $t_{HENA}$ | Flip-Flop (Latch) Enable Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{WCLKA}$ | Flip-Flop (Latch) Clock Active Pulse Width | 4.6 | | 5.2 | | 5.8 | | 6.9 | | 9.6 | | ns |
| $t_{WASYN}$ | Flip-Flop (Latch) Asynchronous Pulse Width | 6.1 | | 6.8 | | 7.7 | | 9.0 | | 12.6 | | ns |
| **Input Module Propagation Delays** | | | | | | | | | | | | |
| $t_{INPY}$ | Input Data Pad-to-Y | | 1.4 | | 1.6 | | 1.8 | | 2.2 | | 3.0 | ns |
| $t_{INGO}$ | Input Latch Gate-to-Output | | 1.8 | | 1.9 | | 2.2 | | 2.6 | | 3.6 | ns |
| $t_{INH}$ | Input Latch Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{INSU}$ | Input Latch Set-Up | 0.7 | | 0.7 | | 0.8 | | 1.0 | | 1.4 | | ns |
| $t_{ILA}$ | Latch Active Pulse Width | 6.5 | | 7.3 | | 8.2 | | 9.7 | | 13.5 | | ns |

Input, output, tristate or bidirectional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. Unused I/Os pins are configured by the Designer software as shown in Table 46, page 84.

***Table 46 •*** **Configuration of Unused I/Os**

| Device | Configuration |
|---|---|
| A40MX02, A40MX04 | Pulled LOW |
| A42MX09, A42MX16 | Pulled LOW |
| A42MX24, A42MX36 | Tristated |

In all cases, it is recommended to tie all unused MX I/O pins to LOW on the board. This applies to all dual-purpose pins when configured as I/Os as well.

**LP, Low Power Mode**

Controls the low power mode of all 42MX devices. The device is placed in the low power mode by connecting the LP pin to logic HIGH. In low power mode, all I/Os are tristated, all input buffers are turned OFF, and the core of the device is turned OFF. To exit the low power mode, the LP pin must be set LOW. The device enters the low power mode 800 ns after the LP pin is driven to a logic HIGH. It will resume normal operation in 200 µs after the LP pin is driven to a logic LOW.

**MODE, Mode**

Controls the use of multifunction pins (DCLK, PRA, PRB, SDI, TDO). The MODE pin is held HIGH to provide verification capability. The MODE pin should be terminated to GND through a 10kΩ resistor so that the MODE pin can be pulled HIGH when required.

**NC, No Connection**

This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

**PRA, I/O**

**PRB, I/OProbe A/B**

The Probe pin is used to output data from any user-defined design node within the device. Each diagnostic pin can be used in conjunction with the other probe pin to allow real-time diagnostic output of any signal path within the device. The Probe pin can be used as a user-defined I/O when verification has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. The Probe pin is accessible when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

**QCLKA/B/C/D, I/O Quadrant Clock**

Quadrant clock inputs for A42MX36 devices. When not used as a register control signal, these pins can function as user I/Os.

**SDI, I/OSerial Data Input**

Serial data input for diagnostic probe and device programming. SDI is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

**SDO, I/OSerial Data Output**

Serial data output for diagnostic probe and device programming. SDO is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW. SDO is available for 42MX devices only.

When Silicon Explorer II is being used, SDO will act as an output while the "checksum" command is run. It will return to user I/O when "checksum" is complete.

**TCK, I/O Test Clock**

***Table 48 •*** **PL68**

| **PL68** | | |
|---|---|---|
| **Pin Number** | **A40MX02 Function** | **A40MX04 Function** |
| 61 | I/O | I/O |
| 62 | I/O | I/O |
| 63 | I/O | I/O |
| 64 | I/O | I/O |
| 65 | I/O | I/O |
| 66 | GND | GND |
| 67 | I/O | I/O |
| 68 | I/O | I/O |

***Figure 40 •*** **PL84**

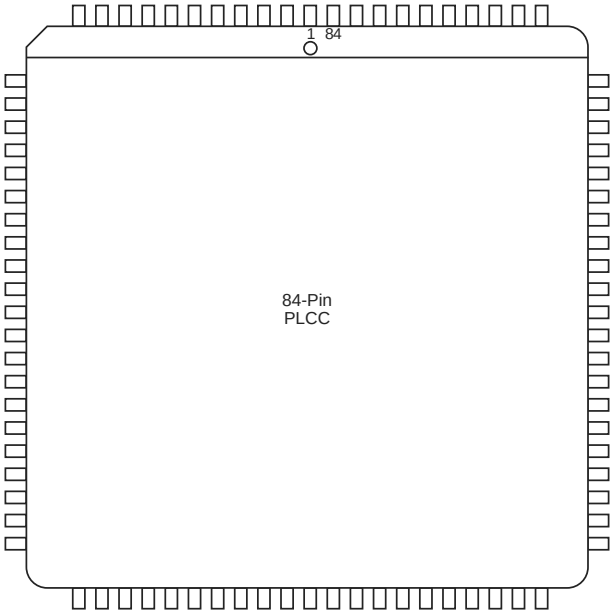



***Table 49 •*** **PL84**

| **PL84** | | | | |
|---|---|---|---|---|
| **Pin Number** | **A40MX04 Function** | **A42MX09 Function** | **A42MX16 Function** | **A42MX24 Function** |
| 1 | I/O | I/O | I/O | I/O |
| 2 | I/O | CLKB, I/O | CLKB, I/O | CLKB, I/O |
| 3 | I/O | I/O | I/O | I/O |
| 4 | VCC | PRB, I/O | PRB, I/O | PRB, I/O |
| 5 | I/O | I/O | I/O | WD, I/O |
| 6 | I/O | GND | GND | GND |
| 7 | I/O | I/O | I/O | I/O |
| 8 | I/O | I/O | I/O | WD, I/O |
| 9 | I/O | I/O | I/O | WD, I/O |

***Table 49 •*** **PL84**

| **PL84** | | | | |
|---|---|---|---|---|
| **Pin Number** | **A40MX04 Function** | **A42MX09 Function** | **A42MX16 Function** | **A42MX24 Function** |
| 47 | I/O | I/O | I/O | WD, I/O |
| 48 | I/O | I/O | I/O | I/O |
| 49 | I/O | GND | GND | GND |
| 50 | I/O | I/O | I/O | WD, I/O |
| 51 | I/O | I/O | I/O | WD, I/O |
| 52 | I/O | SDO, I/O | SDO, I/O | SDO, TDO, I/O |
| 53 | I/O | I/O | I/O | I/O |
| 54 | I/O | I/O | I/O | I/O |
| 55 | I/O | I/O | I/O | I/O |
| 56 | I/O | I/O | I/O | I/O |
| 57 | I/O | I/O | I/O | I/O |
| 58 | I/O | I/O | I/O | I/O |
| 59 | I/O | I/O | I/O | I/O |
| 60 | GND | I/O | I/O | I/O |
| 61 | GND | I/O | I/O | I/O |
| 62 | I/O | I/O | I/O | TCK, I/O |
| 63 | I/O | LP | LP | LP |
| 64 | CLK, I/O | VCCA | VCCA | VCCA |
| 65 | I/O | VCCI | VCCI | VCCI |
| 66 | MODE | I/O | I/O | I/O |
| 67 | VCC | I/O | I/O | I/O |
| 68 | VCC | I/O | I/O | I/O |
| 69 | I/O | I/O | I/O | I/O |
| 70 | I/O | GND | GND | GND |
| 71 | I/O | I/O | I/O | I/O |
| 72 | SDI, I/O | I/O | I/O | I/O |
| 73 | DCLK, I/O | I/O | I/O | I/O |
| 74 | PRA, I/O | I/O | I/O | I/O |
| 75 | PRB, I/O | I/O | I/O | I/O |
| 76 | I/O | SDI, I/O | SDI, I/O | SDI, I/O |
| 77 | I/O | I/O | I/O | I/O |
| 78 | I/O | I/O | I/O | WD, I/O |
| 79 | I/O | I/O | I/O | WD, I/O |
| 80 | I/O | I/O | I/O | WD, I/O |
| 81 | I/O | PRA, I/O | PRA, I/O | PRA, I/O |
| 82 | GND | I/O | I/O | I/O |
| 83 | I/O | CLKA, I/O | CLKA, I/O | CLKA, I/O |

***Figure 43 •*** **PQ160**

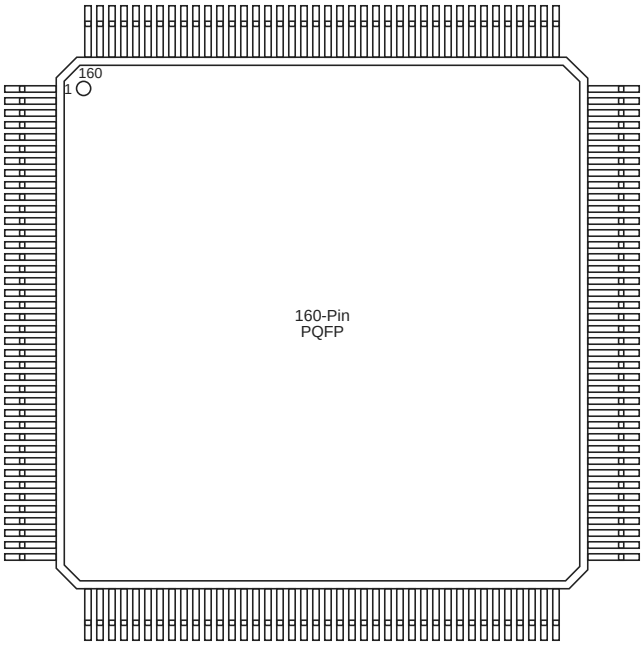



***Table 52 •*** **PQ160**

| **PQ160** | | | |
|---|---|---|---|
| **Pin Number** | **A42MX09 Function** | **A42MX16 Function** | **A42MX24 Function** |
| 1 | I/O | I/O | I/O |
| 2 | DCLK, I/O | DCLK, I/O | DCLK, I/O |
| 3 | NC | I/O | I/O |
| 4 | I/O | I/O | WD, I/O |
| 5 | I/O | I/O | WD, I/O |
| 6 | NC | VCCI | VCCI |
| 7 | I/O | I/O | I/O |
| 8 | I/O | I/O | I/O |
| 9 | I/O | I/O | I/O |
| 10 | NC | I/O | I/O |
| 11 | GND | GND | GND |
| 12 | NC | I/O | I/O |
| 13 | I/O | I/O | WD, I/O |
| 14 | I/O | I/O | WD, I/O |
| 15 | I/O | I/O | I/O |
| 16 | PRB, I/O | PRB, I/O | PRB, I/O |
| 17 | I/O | I/O | I/O |
| 18 | CLKB, I/O | CLKB, I/O | CLKB, I/O |
| 19 | I/O | I/O | I/O |
| 20 | VCCA | VCCA | VCCA |

***Table 52 •*** **PQ160**

| **PQ160** | | | |
|---|---|---|---|
| **Pin Number** | **A42MX09 Function** | **A42MX16 Function** | **A42MX24 Function** |
| 58 | VCCI | VCCI | VCCI |
| 59 | GND | GND | GND |
| 60 | VCCA | VCCA | VCCA |
| 61 | LP | LP | LP |
| 62 | I/O | I/O | TCK, I/O |
| 63 | I/O | I/O | I/O |
| 64 | GND | GND | GND |
| 65 | I/O | I/O | I/O |
| 66 | I/O | I/O | I/O |
| 67 | I/O | I/O | I/O |
| 68 | I/O | I/O | I/O |
| 69 | GND | GND | GND |
| 70 | NC | I/O | I/O |
| 71 | I/O | I/O | I/O |
| 72 | I/O | I/O | I/O |
| 73 | I/O | I/O | I/O |
| 74 | I/O | I/O | I/O |
| 75 | NC | I/O | I/O |
| 76 | I/O | I/O | I/O |
| 77 | NC | I/O | I/O |
| 78 | I/O | I/O | I/O |
| 79 | NC | I/O | I/O |
| 80 | GND | GND | GND |
| 81 | I/O | I/O | I/O |
| 82 | SDO, I/O | SDO, I/O | SDO, TDO, I/O |
| 83 | I/O | I/O | WD, I/O |
| 84 | I/O | I/O | WD, I/O |
| 85 | I/O | I/O | I/O |
| 86 | NC | VCCI | VCCI |
| 87 | I/O | I/O | I/O |
| 88 | I/O | I/O | WD, I/O |
| 89 | GND | GND | GND |
| 90 | NC | I/O | I/O |
| 91 | I/O | I/O | I/O |
| 92 | I/O | I/O | I/O |
| 93 | I/O | I/O | I/O |
| 94 | I/O | I/O | I/O |

***Table 55 •*** **VQ80**

| **VQ80** | | |
|---|---|---|
| **Pin Number** | **A40MX02 Function** | **A40MX04 Function** |
| 49 | I/O | I/O |
| 50 | CLK, I/O | CLK, I/O |
| 51 | I/O | I/O |
| 52 | MODE | MODE |
| 53 | VCC | VCC |
| 54 | NC | I/O |
| 55 | NC | I/O |
| 56 | NC | I/O |
| 57 | SDI, I/O | SDI, I/O |
| 58 | DCLK, I/O | DCLK, I/O |
| 59 | PRA, I/O | PRA, I/O |
| 60 | NC | NC |
| 61 | PRB, I/O | PRB, I/O |
| 62 | I/O | I/O |
| 63 | I/O | I/O |
| 64 | I/O | I/O |
| 65 | I/O | I/O |
| 66 | I/O | I/O |
| 67 | I/O | I/O |
| 68 | GND | GND |
| 69 | I/O | I/O |
| 70 | I/O | I/O |
| 71 | I/O | I/O |
| 72 | I/O | I/O |
| 73 | I/O | I/O |
| 74 | VCC | **VCC** |
| 75 | I/O | I/O |
| 76 | I/O | I/O |
| 77 | I/O | I/O |
| 78 | I/O | I/O |
| 79 | I/O | I/O |
| 80 | I/O | I/O |

***Table 59 •*** **CQ256**

| **CQ256** | |
|---|---|
| **Pin Number** | **A42MX36 Function** |
| 22 | I/O |
| 23 | I/O |
| 24 | I/O |
| 25 | I/O |
| 26 | VCCA |
| 27 | I/O |
| 28 | I/O |
| 29 | VCCA |
| 30 | VCCI |
| 31 | GND |
| 32 | VCCA |
| 33 | LP |
| 34 | TCK, I/O |
| 35 | I/O |
| 36 | GND |
| 37 | I/O |
| 38 | I/O |
| 39 | I/O |
| 40 | I/O |
| 41 | I/O |
| 42 | I/O |
| 43 | I/O |
| 44 | I/O |
| 45 | I/O |
| 46 | I/O |
| 47 | I/O |
| 48 | GND |
| 49 | I/O |
| 50 | I/O |
| 51 | I/O |
| 52 | I/O |
| 53 | I/O |
| 54 | I/O |
| 55 | I/O |
| 56 | I/O |
| 57 | I/O |
| 58 | I/O |

***Table 61 •*** **PG132**

| **PG132** | |
|---|---|
| **Pin Number** | **A42MX09 Function** |
| N10 | I/O |
| M10 | I/O |
| N11 | I/O |
| L10 | I/O |
| M11 | I/O |
| N12 | SDO |
| M12 | I/O |
| L11 | I/O |
| N13 | I/O |
| M13 | I/O |
| K11 | I/O |
| L12 | I/O |
| L13 | I/O |
| K13 | I/O |
| H10 | I/O |
| J12 | I/O |
| J13 | I/O |
| H11 | I/O |
| H12 | I/O |
| H13 | VKS |
| G13 | VPP |

***Table 61 •*** **PG132**

| **PG132** | |
|---|---|
| **Pin Number** | **A42MX09 Function** |
| B3 | I/O |
| A2 | I/O |
| C3 | DCLK |
| B5 | GNDA |
| E12 | GNDA |
| J2 | GNDA |
| M9 | GNDA |
| B9 | GNDI |
| C5 | GNDI |
| E11 | GNDI |
| F4 | GNDI |
| J3 | GNDI |
| J11 | GNDI |
| L5 | GNDI |
| L9 | GNDI |
| C9 | GNDQ |
| E3 | GNDQ |
| K12 | GNDQ |
| D7 | VCCA |
| G3 | VCCA |
| G10 | VCCA |
| L7 | VCCA |
| C7 | VCCI |
| G2 | VCCI |
| G11 | VCCI |
| K7 | VCCI |