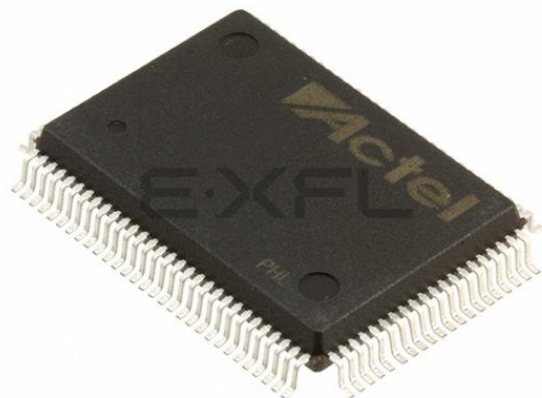




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

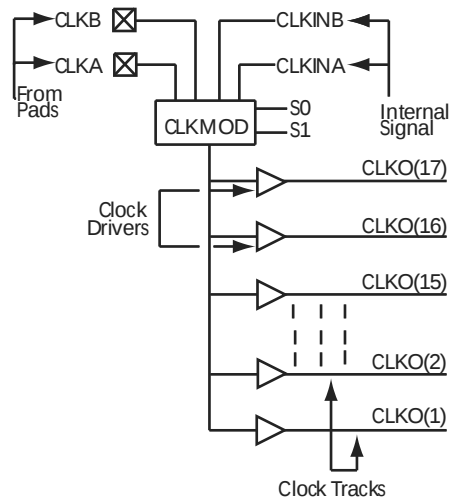
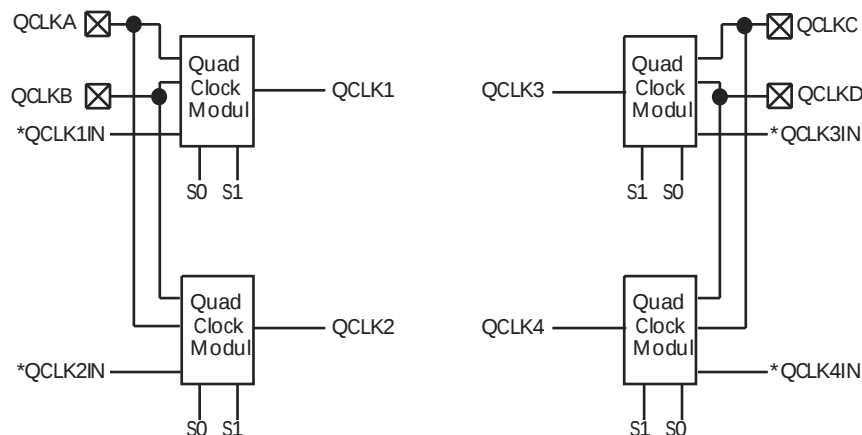
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	57
Number of Gates	3000
Voltage - Supply	3V ~ 3.6V, 4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TC)
Package / Case	100-BQFP
Supplier Device Package	100-PQFP (20x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a40mx02-1pqg100m

3.4.11	Boundary Scan Description Language (BSDL) File	19
3.5	Development Tool Support	19
3.6	Related Documents	20
3.6.1	Application Notes	20
3.6.2	User Guides and Manuals	20
3.6.3	Miscellaneous	20
3.7	5.0 V Operating Conditions	20
3.7.1	5 V TTL Electrical Specifications	21
3.8	3.3 V Operating Conditions	22
3.8.1	3.3 V LVTTTL Electrical Specifications	23
3.9	Mixed 5.0 V / 3.3 V Operating Conditions (for 42MX Devices Only)	23
3.9.1	Mixed 5.0V/3.3V Electrical Specifications	25
3.9.2	Output Drive Characteristics for 5.0 V PCI Signaling	25
3.9.3	Output Drive Characteristics for 3.3 V PCI Signaling	27
3.9.4	Junction Temperature (T_J)	28
3.9.5	Package Thermal Characteristics	28
3.10	Timing Models	30
3.10.1	Parameter Measurement	32
3.10.2	Sequential Module Timing Characteristics	34
3.10.3	Sequential Timing Characteristics	34
3.10.4	Decode Module Timing	35
3.10.5	SRAM Timing Characteristics	35
3.10.6	Dual-Port SRAM Timing Waveforms	35
3.10.7	Predictable Performance: Tight Delay Distributions	37
3.11	Timing Characteristics	37
3.11.1	Critical Nets and Typical Nets	37
3.11.2	Long Tracks	37
3.11.3	Timing Derating	38
3.11.4	Temperature and Voltage Derating Factors	38
3.11.5	PCI System Timing Specification	40
3.11.6	PCI Models	40
3.12	Pin Descriptions	83
4	Package Pin Assignments	86

Tables

Table 1	Product profile	1
Table 2	Plastic Device Resources	4
Table 3	Ceramic Device Resources	4
Table 4	Temperature Grade Offerings	5
Table 5	Speed Grade Offerings	5
Table 6	Voltage Support of MX Devices	13
Table 7	Fixed Capacitance Values for MX FPGAs (pF)	16
Table 8	Device Configuration Options for Probe Capability	17
Table 9	Test Access Port Descriptions	18
Table 10	Supported BST Public Instructions	18
Table 11	Boundary Scan Pin Configuration and Functionality	19
Table 12	Absolute Maximum Ratings for 40MX Devices*	20
Table 13	Absolute Maximum Ratings for 42MX Devices*	20
Table 14	Recommended Operating Conditions	21
Table 15	5V TTL Electrical Specifications	21
Table 16	Absolute Maximum Ratings for 40MX Devices*	22
Table 17	Absolute Maximum Ratings for 42MX Devices*	22
Table 18	Recommended Operating Conditions	22
Table 19	3.3V LVTTTL Electrical Specifications	23
Table 20	Absolute Maximum Ratings*	23
Table 21	Recommended Operating Conditions	24
Table 22	Mixed 5.0V/3.3V Electrical Specifications	25
Table 23	DC Specification (5.0 V PCI Signaling)	25
Table 24	AC Specifications (5.0V PCI Signaling)*	26
Table 25	DC Specification (3.3 V PCI Signaling)	27
Table 26	AC Specifications for (3.3 V PCI Signaling)*	27
Table 27	Package Thermal Characteristics	29
Table 28	42MX Temperature and Voltage Derating Factors (Normalized to $T_J = 25^{\circ}\text{C}$, $V_{CCA} = 5.0\text{ V}$)	38
Table 29	40MX Temperature and Voltage Derating Factors(Normalized to $T_J = 25^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V}$)	38
Table 30	42MX Temperature and Voltage Derating Factors(Normalized to $T_J = 25^{\circ}\text{C}$, $V_{CCA} = 3.3\text{ V}$)	39
Table 31	40MX Temperature and Voltage Derating Factors (Normalized to $T_J = 25^{\circ}\text{C}$, $V_{CC} = 3.3\text{ V}$)	39
Table 32	Clock Specification for 33 MHz PCI	40
Table 33	Timing Parameters for 33 MHz PCI	40
Table 34	A40MX02 Timing Characteristics (Nominal 5.0 V Operation)	41
Table 35	A40MX02 Timing Characteristics (Nominal 3.3 V Operation)	43
Table 36	A40MX04 Timing Characteristics (Nominal 5.0 V Operation) (Worst-Case Commercial Conditions, $V_{CC} = 4.75\text{ V}$, $T_J = 70^{\circ}\text{C}$)	46
Table 37	A40MX04 Timing Characteristics (Nominal 3.3 V Operation) (Worst-Case Commercial Conditions, $V_{CC} = 3.0\text{ V}$, $T_J = 70^{\circ}\text{C}$)	49
Table 38	A42MX09 Timing Characteristics (Nominal 5.0 V Operation) (Worst-Case Commercial Conditions, $V_{CCA} = 4.75\text{ V}$, $T_J = 70^{\circ}\text{C}$)	52
Table 39	A42MX09 Timing Characteristics (Nominal 3.3 V Operation) (Worst-Case Commercial Conditions, $V_{CCA} = 3.0\text{ V}$, $T_J = 70^{\circ}\text{C}$)	56
Table 40	A42MX16 Timing Characteristics (Nominal 5.0 V Operation) (Worst-Case Commercial Conditions, $V_{CCA} = 4.75\text{ V}$, $T_J = 70^{\circ}\text{C}$)	60
Table 41	A42MX16 Timing Characteristics (Nominal 3.3 V Operation) (Worst-Case Commercial Conditions, $V_{CCA} = 3.0\text{ V}$, $T_J = 70^{\circ}\text{C}$)	64
Table 42	A42MX24 Timing Characteristics (Nominal 5.0 V Operation) (Worst-Case Commercial Conditions, $V_{CCA} = 4.75\text{ V}$, $T_J = 70^{\circ}\text{C}$)	67
Table 43	A42MX24 Timing Characteristics (Nominal 3.3 V Operation) (Worst-Case Commercial Conditions, $V_{CCA} = 3.0\text{ V}$, $T_J = 70^{\circ}\text{C}$)	71
Table 44	A42MX36 Timing Characteristics (Nominal 5.0 V Operation)(Worst-Case Commercial Conditions, $V_{CCA} = 4.75\text{ V}$, $T_J = 70^{\circ}\text{C}$)	75
Table 45	A42MX36 Timing Characteristics (Nominal 3.3 V Operation) (Worst-Case Commercial Conditions,	

	VCCA = 3.0 V, T _J = 70°C)	79
Table 46	Configuration of Unused I/Os	84
Table 47	PL44	86
Table 48	PL68	88
Table 49	PL84	90
Table 50	PQ 100	93
Table 51	PQ144	97
Table 52	PQ160	102
Table 53	PQ208	107
Table 54	PQ240	113
Table 55	VQ80	120
Table 56	VQ100	123
Table 57	TQ176	126
Table 58	CQ208	132
Table 59	CQ256	138
Table 60	BG272	145
Table 61	PG132	153
Table 62	CQ172	158

Figure 8 • Clock Networks of 42MX Devices**Figure 9 • Quadrant Clock Network of A42MX36 Devices**

Note: *QCLK1IN, QCLK2IN, QCLK3IN, and QCLK4IN are internally-generated signals.

3.2.5 MultiPlex I/O Modules

42MX devices feature Multiplex I/Os and support 5.0 V, 3.3 V, and mixed 3.3 V/5.0 V operations.

The MultiPlex I/O modules provide the interface between the device pins and the logic array. Figure 10, page 12 is a block diagram of the 42MX I/O module. A variety of user functions, determined by a library macro selection, can be implemented in the module. (See the *Antifuse Macro Library Guide* for more information.) All 42MX I/O modules contain tristate buffers, with input and output latches that can be configured for input, output, or bidirectional operation.

All 42MX devices contain flexible I/O structures, where each output pin has a dedicated output-enable control (Figure 10, page 12). The I/O module can be used to latch input or output data, or both, providing fast set-up time. In addition, the Designer software tools can build a D-type flip-flop using a C-module combined with an I/O module to register input and output signals. See the *Antifuse Macro Library Guide* for more details.

A42MX24 and A42MX36 devices also offer selectable PCI output drives, enabling 100% compliance with version 2.1 of the PCI specification. For low-power systems, all inputs and outputs are turned off to reduce current consumption to below 500 μ A.

To achieve 5.0 V or 3.3 V PCI-compliant output drives on A42MX24 and A42MX36 devices, a chip-wide PCI fuse is programmed via the Device Selection Wizard in the Designer software (Figure 11, page 12). When the PCI fuse is not programmed, the output drive is standard.

Note: *Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the recommended operating conditions.

Table 14 • Recommended Operating Conditions

Parameter	Commercial	Industrial	Military	Units
Temperature Range*	0 to +70	–40 to +85	–55 to +125	°C
VCC (40MX)	4.75 to 5.25	4.5 to 5.5	4.5 to 5.5	V
VCCA (42MX)	4.75 to 5.25	4.5 to 5.5	4.5 to 5.5	V
VCCI (42MX)	4.75 to 5.25	4.5 to 5.5	4.5 to 5.5	V

Note: * Ambient temperature (T_A) is used for commercial and industrial grades; case temperature (T_C) is used for military grades.

3.7.1 5 V TTL Electrical Specifications

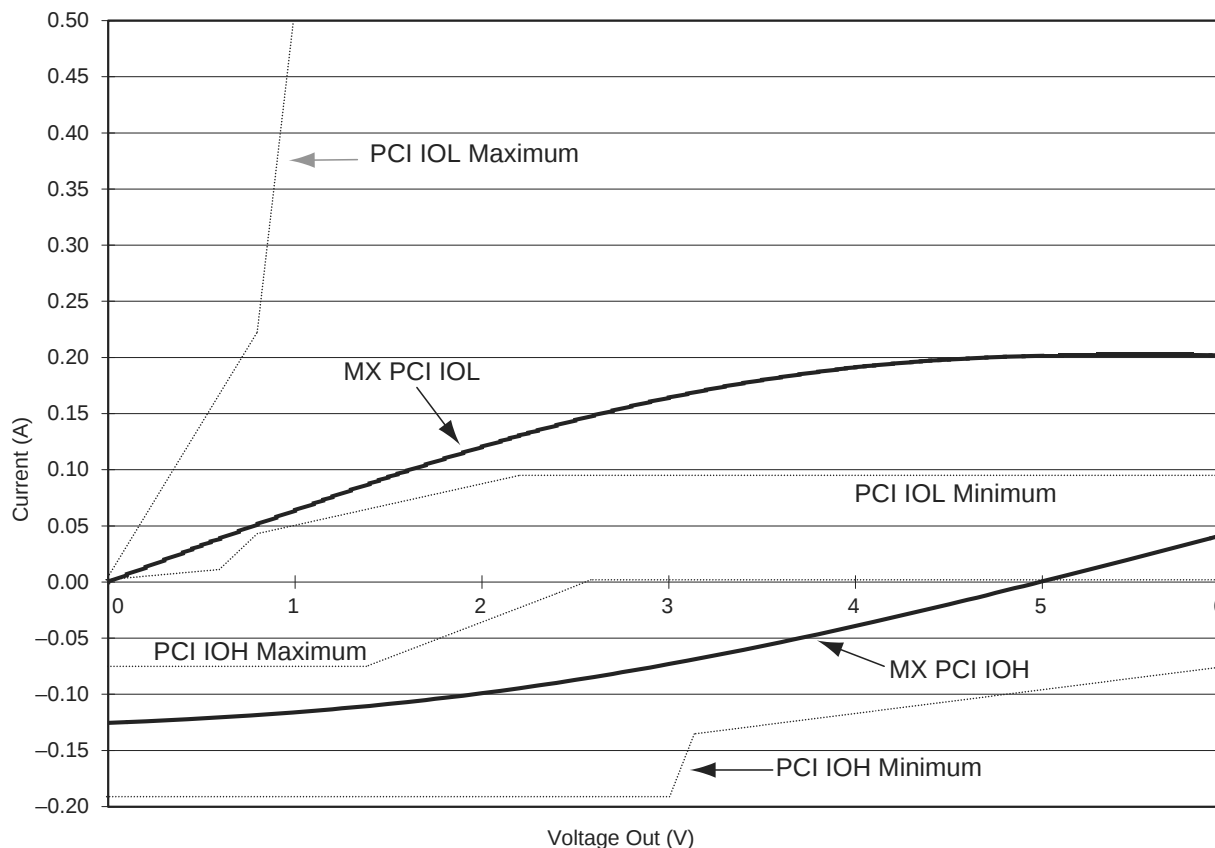
The following tables show 5 V TTL electrical specifications.

Table 15 • 5V TTL Electrical Specifications

Symbol	Parameter	Commercial		Commercial -F		Industrial		Military		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
VOH ¹	IOH = –10 mA	2.4		2.4						V
	IOH = –4 mA					3.7		3.7		V
VOL ¹	IOL = 10 mA		0.5		0.5					V
	IOL = 6 mA					0.4		0.4		V
VIL		–0.3	0.8	–0.3	0.8	–0.3	0.8	–0.3	0.8	V
VIH (40MX)		2.0	VCC + 0.3	2.0	VCC + 0.3	2.0	VCC + 0.3	2.0	VCC + 0.3	V
VIH (42MX) ²		2.0	VCCI + 0.3	2.0	VCCI + 0.3	2.0	VCCI + 0.3	2.0	VCCI + 0.3	V
IIL	VIN = 0.5 V		–10		–10		–10		–10	μA
IIH	VIN = 2.7 V		–10		–10		–10		–10	μA
Input Transition Time, T_R and T_F			500		500		500		500	ns
C _{IO} I/O Capacitance			10		10		10		10	pF
Standby Current, ICC ³	A40MX02, A40MX04		3		25		10		25	mA
	A42MX09		5		25		25		25	mA
	A42MX16		6		25		25		25	mA
	A42MX24, A42MX36		20		25		25		25	mA
Low power mode Standby Current	42MX devices only		0.5		ICC – 5.0		ICC – 5.0		ICC – 5.0	mA
IIO, I/O source sink current	Can be derived from the <i>IBIS model</i> (http://www.microsemi.com/soc/techdocs/models/ibis.html)									

1. Only one output tested at a time. VCC/VCCI = min

2. VIH(Min) is 2.4V for A42MX36 family. This applies only to VCCI of 5V and is not applicable to VCCI of 3.3V

Figure 16 • Typical Output Drive Characteristics (Based Upon Measured Data)

3.9.4 Junction Temperature (T_J)

The temperature variable in the Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because the heat generated from dynamic power consumption is usually hotter than the ambient temperature. The following equation can be used to calculate junction temperature.

$$\text{Junction Temperature} = \Delta T + T_a(1)$$

EQ 4

where:

- T_a = Ambient Temperature
- ΔT = Temperature gradient between junction (silicon) and ambient
- $\Delta T = \theta_{ja} * P$ (2)
- P = Power
- θ_{ja} = Junction to ambient of package. θ_{ja} numbers are located in Table 27, page 29.

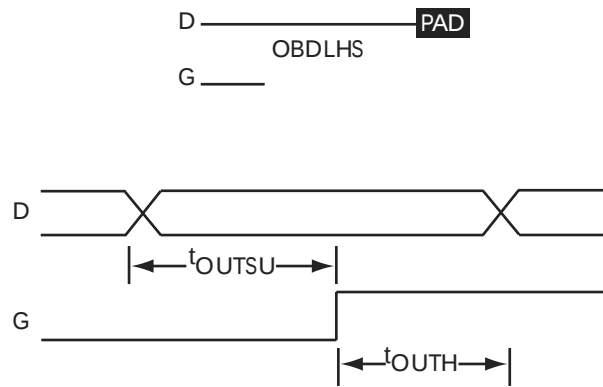
3.9.5 Package Thermal Characteristics

The device junction-to-case thermal characteristic is θ_{jc} , and the junction-to-ambient air characteristic is θ_{ja} . The thermal characteristics for θ_{ja} are shown with two different air flow rates.

The maximum junction temperature is 150°C.

Maximum power dissipation for commercial- and industrial-grade devices is a function of θ_{ja} .

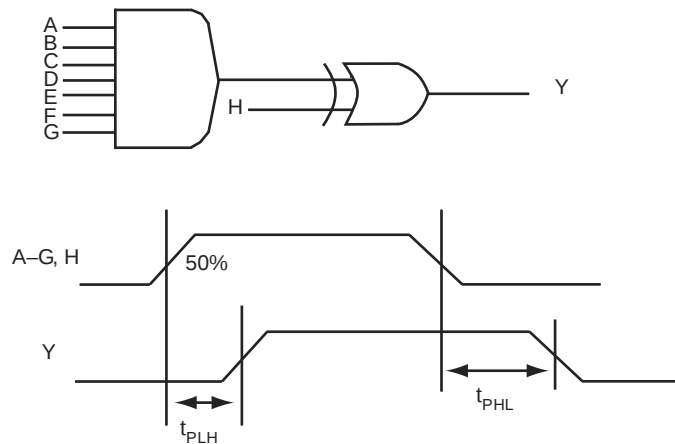
Figure 27 • Output Buffer Latches



3.10.4 Decode Module Timing

The following figure shows decode module timing.

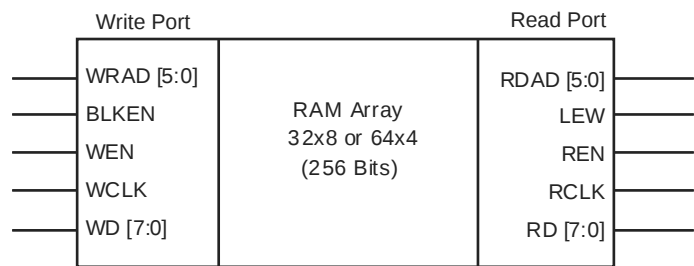
Figure 28 • Decode Module Timing



3.10.5 SRAM Timing Characteristics

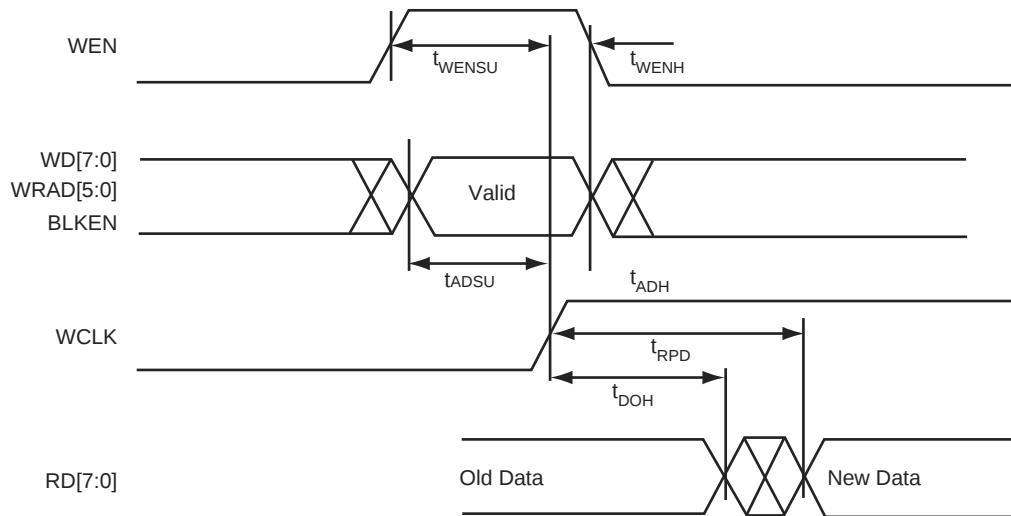
The following figure shows SRAM timing characteristics.

Figure 29 • SRAM Timing Characteristics



3.10.6 Dual-Port SRAM Timing Waveforms

The following figures show dual-port SRAM timing waveforms.

Figure 33 • 42MX SRAM Asynchronous Read Operation—Type 2 (Write Address Controlled)

3.10.7 Predictable Performance: Tight Delay Distributions

Propagation delay between logic modules depends on the resistive and capacitive loading of the routing tracks, the interconnect elements, and the module inputs being driven. Propagation delay increases as the length of routing tracks, the number of interconnect elements, or the number of inputs increases.

From a design perspective, the propagation delay can be statistically correlated or modeled by the fanout (number of loads) driven by a module. Higher fanout usually requires some paths to have longer routing tracks.

The MX FPGAs deliver a tight fanout delay distribution, which is achieved in two ways: by decreasing the delay of the interconnect elements and by decreasing the number of interconnect elements per path.

Microsemi's patented antifuse offers a very low resistive/capacitive interconnect. The antifuses, fabricated in 0.45 μm lithography, offer nominal levels of 100 Ω resistance and 7.0 fF capacitance per antifuse.

MX fanout distribution is also tight due to the low number of antifuses required for each interconnect path. The proprietary architecture limits the number of antifuses per path to a maximum of four, with 90 percent of interconnects using only two antifuses.

3.11 Timing Characteristics

Device timing characteristics fall into three categories: family-dependent, device-dependent, and design-dependent. The input and output buffer characteristics are common to all MX devices. Internal routing delays are device-dependent; actual delays are not determined until after place-and-route of the user's design is complete. Delay values may then be determined by using the Designer software utility or by performing simulation with post-layout delays.

3.11.1 Critical Nets and Typical Nets

Propagation delays are expressed only for typical nets, which are used for initial design performance evaluation. Critical net delays can then be applied to the most timing critical paths. Critical nets are determined by net property assignment in Microsemi's Designer software prior to placement and routing. Up to 6% of the nets in a design may be designated as critical.

3.11.2 Long Tracks

Some nets in the design use long tracks, which are special routing resources that span multiple rows, columns, or modules. Long tracks employ three and sometimes four antifuse connections, which increase capacitance and resistance, resulting in longer net delays for macros connected to long tracks. Typically, up to 6 percent of nets in a fully utilized device require long tracks. Long tracks add

Table 39 • A42MX09 Timing Characteristics (Nominal 3.3 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
TTL Output Module Timing ⁵												
t _{DLH}	Data-to-Pad HIGH	3.4		3.8		4.3		5.1		7.1		ns
t _{DHL}	Data-to-Pad LOW	4.0		4.5		5.1		6.1		8.3		ns
t _{ENZH}	Enable Pad Z to HIGH	3.7		4.1		4.6		5.5		7.6		ns
t _{ENZL}	Enable Pad Z to LOW	4.1		4.5		5.1		6.1		8.5		ns
t _{ENHZ}	Enable Pad HIGH to Z	6.9		7.6		8.6		10.2		14.2		ns
t _{ENLZ}	Enable Pad LOW to Z	7.5		8.3		9.4		11.1		15.5		ns
t _{GLH}	G-to-Pad HIGH	5.8		6.5		7.3		8.6		12.0		ns
t _{GHL}	G-to-Pad LOW	5.8		6.5		7.3		8.6		12.0		ns
t _{LSU}	I/O Latch Set-Up	0.7		0.8		0.9		1.0		1.4		ns
t _{LH}	I/O Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading	8.7		9.7		10.9		12.9		18.0		ns
t _{ACO}	Array Clock-to-Out (Pad-to-Pad),64 Clock Loading	12.2		13.5		15.4		18.1		25.3		ns
d _{TLH}	Capacity Loading, LOW to HIGH	0.00		0.00		0.00		0.10		0.01		ns/pF
d _{THL}	Capacity Loading, HIGH to LOW	0.09		0.10		0.10		0.10		0.10		ns/pF

Table 40 • A42MX16 Timing Characteristics (Nominal 5.0 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description			–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{PWL}	Minimum Pulse Width LOW	FO = 32	3.2		3.5		4.0		4.7		6.6		ns
		FO = 384	3.7		4.1		4.6		5.4		7.6		ns
t _{CKSW}	Maximum Skew	FO = 32		0.3		0.4		0.4		0.5		0.7	ns
		FO = 384		0.3		0.4		0.4		0.5		0.7	ns
t _{SUEXT}	Input Latch External Set-Up	FO = 32	0.0		0.0		0.0		0.0		0.0		ns
		FO = 384	0.0		0.0		0.0		0.0		0.0		ns
t _{HEXT}	Input Latch External Hold	FO = 32	2.8		3.1		5.5		4.1		5.7		ns
		FO = 384	3.2		3.5		4.0		4.7		6.6		ns
t _P	Minimum Period	FO = 32	4.2		4.67		5.1		5.8		9.7		ns
		FO = 384	4.6		5.1		5.6		6.4		10.7		ns
f _{MAX}	Maximum Frequency	FO = 32		237		215		198		172		103	MHz
		FO = 384		215		195		179		156		94	MHz

Table 43 • A42MX24 Timing Characteristics (Nominal 3.3 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)

Parameter / Description			–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
TTL Output Module Timing ⁵ (continued)													
t _{LH}	I/O Latch Output Hold		0.0		0.0		0.0		0.0		0.0		ns
t _{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O			7.7		8.5		9.6		11.3		15.9	ns
t _{ACO}	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O			14.8		16.5		18.7		22.0		30.8	ns
d _{TLH}	Capacitive Loading, LOW to HIGH			0.05		0.05		0.06		0.07		0.10	ns/pF
d _{THL}	Capacitive Loading, HIGH to LOW			0.04		0.04		0.05		0.06		0.08	ns/pF
CMOS Output Module Timing ⁵													
t _{DLH}	Data-to-Pad HIGH			4.8		5.3		5.5		6.4		9.0	ns
t _{DHL}	Data-to-Pad LOW			3.5		3.9		4.1		4.9		6.8	ns
t _{ENZH}	Enable Pad Z to HIGH			3.6		4.0		4.5		5.3		7.4	ns
t _{ENZL}	Enable Pad Z to LOW			3.4		4.0		5.0		5.8		8.2	ns
t _{ENHZ}	Enable Pad HIGH to Z			7.2		8.0		9.0		10.7		14.9	ns
t _{ENLZ}	Enable Pad LOW to Z			6.7		7.5		8.5		9.9		13.9	ns
t _{GLH}	G-to-Pad HIGH			6.8		7.6		8.6		10.1		14.2	ns
t _{GHL}	G-to-Pad LOW			6.8		7.6		8.6		10.1		14.2	ns
t _{LSU}	I/O Latch Set-Up		0.7		0.7		0.8		1.0		1.4		ns
t _{LH}	I/O Latch Hold		0.0		0.0		0.0		0.0		0.0		ns
t _{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O			7.7		8.5		9.6		11.3		15.9	ns
t _{ACO}	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O			14.8		16.5		18.7		22.0		30.8	ns
d _{TLH}	Capacitive Loading, LOW to HIGH			0.05		0.05		0.06		0.07		0.10	ns/pF
d _{THL}	Capacitive Loading, HIGH to LOW			0.04		0.04		0.05		0.06		0.08	ns/pF
t _{HEXT}	Input Latch External Hold	FO = 32	3.9		4.3		4.9		5.7		8.1		ns
		FO = 486	4.6		5.2		5.8		6.9		9.6		ns
t _P	Minimum Period (1/f _{MAX})	FO = 32	7.8		8.7		9.5		10.8		18.2		ns
		FO = 486	8.6		9.5		10.4		11.9		19.9		ns

1. For dual-module macros, use t_{PD1} + t_{RD1} + t_{PDn}, t_{CO} + t_{RD1} + t_{PDn}, or t_{PD1} + t_{RD1} + t_{SUD}, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
4. Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.
5. Delays based on 35 pF loading.

Table 48 • PL68

PL68		
Pin Number	A40MX02 Function	A40MX04 Function
24	I/O	I/O
25	VCC	VCC
26	I/O	I/O
27	I/O	I/O
28	I/O	I/O
29	I/O	I/O
30	I/O	I/O
31	I/O	I/O
32	GND	GND
33	I/O	I/O
34	I/O	I/O
35	I/O	I/O
36	I/O	I/O
37	I/O	I/O
38	VCC	VCC
39	I/O	I/O
40	I/O	I/O
41	I/O	I/O
42	I/O	I/O
43	I/O	I/O
44	I/O	I/O
45	I/O	I/O
46	I/O	I/O
47	I/O	I/O
48	I/O	I/O
49	GND	GND
50	I/O	I/O
51	I/O	I/O
52	CLK, I/O	CLK, I/O
53	I/O	I/O
54	MODE	MODE
55	VCC	VCC
56	SDI, I/O	SDI, I/O
57	DCLK, I/O	DCLK, I/O
58	PRA, I/O	PRA, I/O
59	PRB, I/O	PRB, I/O
60	I/O	I/O

Table 50 • PQ 100

PQ100				
Pin Number	A40MX02 Function	A40MX04 Function	A42MX09 Function	A42MX16 Function
19	VCC	V _{CC}	I/O	I/O
20	I/O	I/O	I/O	I/O
21	I/O	I/O	I/O	I/O
22	I/O	I/O	GND	GND
23	I/O	I/O	I/O	I/O
24	I/O	I/O	I/O	I/O
25	I/O	I/O	I/O	I/O
26	I/O	I/O	I/O	I/O
27	NC	NC	I/O	I/O
28	NC	NC	I/O	I/O
29	NC	NC	I/O	I/O
30	NC	NC	I/O	I/O
31	NC	I/O	I/O	I/O
32	NC	I/O	I/O	I/O
33	NC	I/O	I/O	I/O
34	I/O	I/O	GND	GND
35	I/O	I/O	I/O	I/O
36	GND	GND	I/O	I/O
37	GND	GND	I/O	I/O
38	I/O	I/O	I/O	I/O
39	I/O	I/O	I/O	I/O
40	I/O	I/O	VCCA	VCCA
41	I/O	I/O	I/O	I/O
42	I/O	I/O	I/O	I/O
43	VCC	VCC	I/O	I/O
44	VCC	VCC	I/O	I/O
45	I/O	I/O	I/O	I/O
46	I/O	I/O	GND	GND
47	I/O	I/O	I/O	I/O
48	NC	I/O	I/O	I/O
49	NC	I/O	I/O	I/O
50	NC	I/O	I/O	I/O
51	NC	NC	I/O	I/O
52	NC	NC	SDO, I/O	SDO, I/O
53	NC	NC	I/O	I/O
54	NC	NC	I/O	I/O
55	NC	NC	I/O	I/O

Figure 42 • PQ144

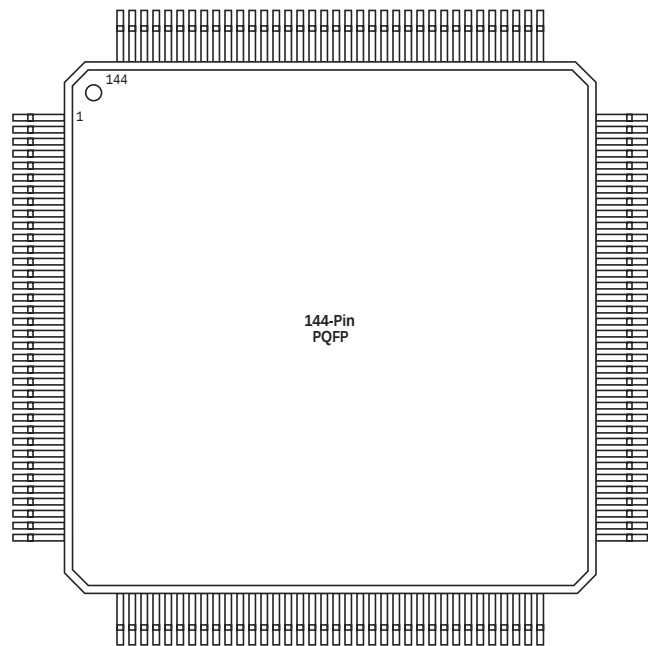


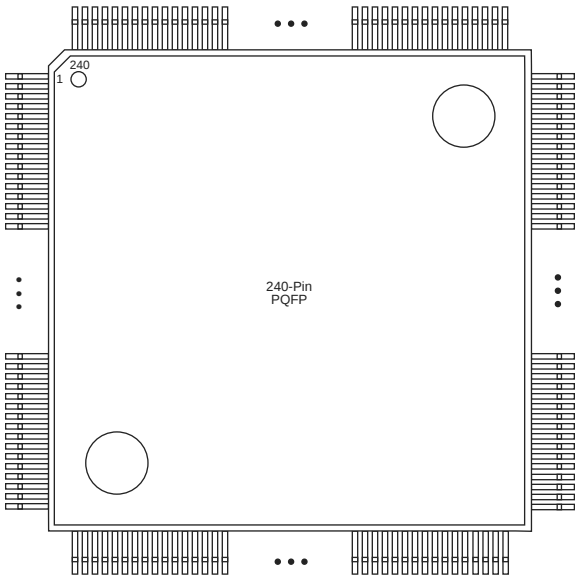
Table 51 • PQ144

PQ144	
Pin Number	A42MX09 Function
1	I/O
2	MODE
3	I/O
4	I/O
5	I/O

Table 53 • PQ208

PQ208			
Pin Number	A42MX16 Function	A42MX24 Function	A42MX36 Function
206	I/O	I/O	I/O
207	DCLK, I/O	DCLK, I/O	DCLK, I/O
208	I/O	I/O	I/O

Figure 45 • PQ240



Note: This figure shows the 240-Pin PQFP Package top view.

Table 54 • PQ240

PQ240	
Pin Number	A42MX36 Function
1	I/O
2	DCLK, I/O
3	I/O
4	I/O
5	I/O
6	WD, I/O
7	WD, I/O
8	VCCI
9	I/O
10	I/O
11	I/O
12	I/O
13	I/O
14	I/O

Table 54 • PQ240

PQ240	
Pin Number	A42MX36 Function
52	VCCI
53	I/O
54	WD, I/O
55	WD, I/O
56	I/O
57	SDI, I/O
58	I/O
59	VCCA
60	GND
61	GND
62	I/O
63	I/O
64	I/O
65	I/O
66	I/O
67	I/O
68	I/O
69	I/O
70	I/O
71	VCCI
72	I/O
73	I/O
74	I/O
75	I/O
76	I/O
77	I/O
78	I/O
79	I/O
80	I/O
81	I/O
82	I/O
83	I/O
84	I/O
85	VCCA
86	I/O
87	I/O
88	VCCA

Figure 47 • VQ100

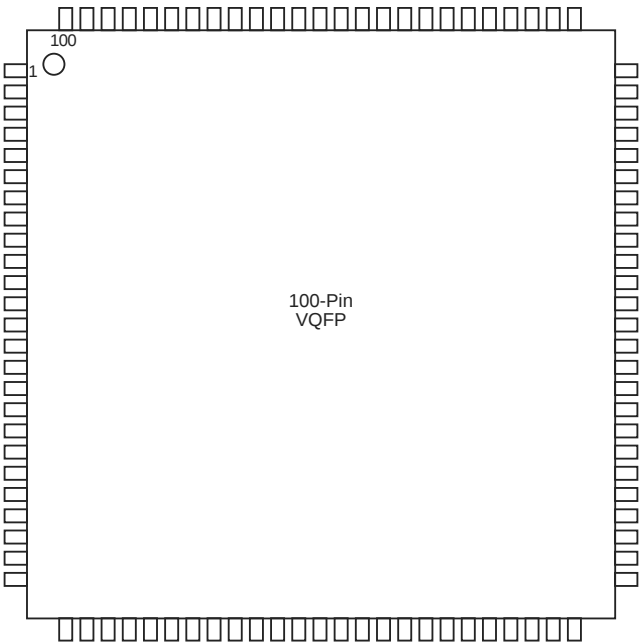


Table 56 • VQ100

VQ100		
Pin Number	A42MX09 Function	A42MX16 Function
1	I/O	I/O
2	MODE	MODE
3	I/O	I/O
4	I/O	I/O
5	I/O	I/O
6	I/O	I/O
7	GND	GND
8	I/O	I/O
9	I/O	I/O
10	I/O	I/O
11	I/O	I/O
12	I/O	I/O
13	I/O	I/O
14	VCCA	NC
15	VCCI	VCCI
16	I/O	I/O
17	I/O	I/O
18	I/O	I/O
19	I/O	I/O
20	GND	GND

Table 58 • CQ208

CQ208	
Pin Number	A42MX36 Function
1	GND
2	VCCA
3	MODE
4	I/O
5	I/O
6	I/O
7	I/O
8	I/O
9	I/O
10	I/O
11	I/O
12	I/O
13	I/O
14	I/O
15	I/O
16	I/O
17	VCCA
18	I/O
19	I/O
20	I/O
21	I/O
22	GND
23	I/O
24	I/O
25	I/O
26	I/O
27	GND
28	VCCI
29	VCCA
30	I/O
31	I/O
32	VCCA
33	I/O
34	I/O
35	I/O
36	I/O

Table 58 • CQ208

CQ208	
Pin Number	A42MX36 Function
185	I/O
186	CLKB, I/O
187	I/O
188	PRB, I/O
189	I/O
190	WD, I/O
191	WD, I/O
192	I/O
193	I/O
194	WD, I/O
195	WD, I/O
196	QCLKC, I/O
197	I/O
198	I/O
199	I/O
200	I/O
201	I/O
202	VCCI
203	WD, I/O
204	WD, I/O
205	I/O
206	I/O
207	DCLK, I/O
208	I/O

Table 61 • PG132

PG132	
Pin Number	A42MX09 Function
F2	I/O
F1	I/O
G1	I/O
G4	VSV
H1	I/O
H2	I/O
H3	I/O
H4	I/O
J1	I/O
K1	I/O
L1	I/O
K2	I/O
M1	I/O
K3	I/O
L2	I/O
N1	I/O
L3	BININ
M2	BINOUT
N2	I/O
M3	I/O
L4	I/O
N3	I/O
M4	I/O
N4	I/O
M5	I/O
K6	I/O
N5	I/O
N6	I/O
L6	I/O
M6	I/O
M7	I/O
N7	I/O
N8	I/O
M8	I/O
L8	I/O
K8	I/O
N9	I/O