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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	57
Number of Gates	3000
Voltage - Supply	3V ~ 3.6V, 4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	80-TQFP
Supplier Device Package	80-VQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a40mx02-2vq80i

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3.3.7 Low Power Mode

42MX devices have been designed with a Low Power Mode. This feature, activated with setting the special LP pin to HIGH for a period longer than 800 ns, is particularly useful for battery-operated systems where battery life is a primary concern. In this mode, the core of the device is turned off and the device consumes minimal power with low standby current. In addition, all input buffers are turned off, and all outputs and bidirectional buffers are tristated. Since the core of the device is turned off, the states of the registers are lost. The device must be re-initialized when exiting Low Power Mode. I/Os can be driven during LP mode, and clock pins should be driven HIGH or LOW and should not float to avoid drawing current. To exit LP mode, the LP pin must be pulled LOW for over 200 μ s to allow for charge pumps to power up, and device initialization will begin.

3.4 Power Dissipation

The general power consumption of MX devices is made up of static and dynamic power and can be expressed with the following equation.

3.4.1 General Power Equation

$$P = [ICC_{standby} + ICC_{active}] * V_{CCI} + IOL * VOL * N + IOH * (V_{CCI} - VOH) * M$$

EQ 1

where:

- $ICC_{standby}$ is the current flowing when no inputs or outputs are changing.
- ICC_{active} is the current flowing due to CMOS switching.
- IOL , IOH are TTL sink/source currents.
- VOL , VOH are TTL level output voltages.
- N equals the number of outputs driving TTL loads to VOL .
- M equals the number of outputs driving TTL loads to VOH .

Accurate values for N and M are difficult to determine because they depend on the family type, on design details, and on the system I/O. The power can be divided into two components: static and active.

3.4.2 Static Power Component

The static power due to standby current is typically a small component of the overall power consumption. Standby power is calculated for commercial, worst-case conditions. The static power dissipation by TTL loads depends on the number of outputs driving, and on the DC load current. For instance, a 32-bit bus sinking 4mA at 0.33V will generate 42mW with all outputs driving LOW, and 140mW with all outputs driving HIGH. The actual dissipation will average somewhere in between, as I/Os switch states with time.

3.4.3 Active Power Component

Power dissipation in CMOS devices is usually dominated by the dynamic power dissipation. Dynamic power consumption is frequency-dependent and is a function of the logic and the external I/O. Active power dissipation results from charging internal chip capacitances of the interconnect, unprogrammed antifuses, module inputs, and module outputs, plus external capacitances due to PC board traces and load device inputs. An additional component of the active power dissipation is the totem pole current in the CMOS transistor pairs. The net effect can be associated with an equivalent capacitance that can be combined with frequency and voltage to represent active power dissipation.

The power dissipated by a CMOS circuit can be expressed by the equation:

$$\text{Power}(\mu\text{W}) = C_{EQ} * V_{CCA}^2 * F(1)$$

EQ 2

where:

- C_{EQ} = Equivalent capacitance expressed in picofarads (pF)

3.8.1 3.3 V LVTTTL Electrical Specifications

Table 19 • 3.3V LVTTTL Electrical Specifications

Symbol	Parameter	Commercial		Commercial -F		Industrial		Military		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
VOH ¹	IOH = -4 mA	2.15		2.15		2.4		2.4		V
VOL ¹	IOL = 6 mA		0.4		0.4		0.48		0.48	V
VIL		-0.3	0.8	-0.3	0.8	-0.3	0.8	-0.3	0.8	V
VIH (40MX)		2.0	VCC + 0.3	2.0	VCC + 0.3	2.0	VCC + 0.3	2.0	VCC + 0.3	V
VIH (42MX)		2.0	VCCI + 0.3	2.0	VCCI + 0.3	2.0	VCCI + 0.3	2.0	VCCI + 0.3	V
IIL			-10		-10		-10		-10	μA
IIH			-10		-10		-10		-10	μA
Input Transition Time, T _R and T _F			500		500		500		500	ns
C _{IO} I/O Capacitance			10		10		10		10	pF
Standby Current, ICC ²	A40MX02, A40MX04		3		25		10		25	mA
	A42MX09		5		25		25		25	mA
	A42MX16		6		25		25		25	mA
	A42MX24, A42MX36		15		25		25		25	mA
Low-Power Mode Standby Current	42MX devices only		0.5		ICC - 5.0		ICC - 5.0		ICC - 5.0	mA
IIO, I/O source sink current	Can be derived from the <i>IBIS model</i> (http://www.microsemi.com/soc/techdocs/models/ibis.html)									

1. Only one output tested at a time. VCC/VCCI = min.
2. All outputs unloaded. All inputs = VCC/VCCI or GND.

3.9 Mixed 5.0 V / 3.3 V Operating Conditions (for 42MX Devices Only)

Table 20 • Absolute Maximum Ratings*

Symbol	Parameter	Limits	Units
VCCI	DC Supply Voltage for I/Os	-0.5 to +7.0	V
VCCA	DC Supply Voltage for Array	-0.5 to +7.0	V
VI	Input Voltage	-0.5 to VCCA + 0.5	V
VO	Output Voltage	-0.5 to VCCI + 0.5	V
t _{STG}	Storage Temperature	-65 to +150	°C

Note: *Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device

Table 23 • DC Specification (5.0 V PCI Signaling)¹

Symbol	Parameter	Condition	PCI		MX		Units
			Min.	Max.	Min.	Max.	
C _{IN}	Input Pin Capacitance			10	—	10	pF
C _{CLK}	CLK Pin Capacitance		5	12	—	10	pF
L _{PIN}	Pin Inductance			20	—	< 8 nH ⁴	nH

1. PCI Local Bus Specification, Version 2.1, Section 4.2.1.1.

2. Maximum rating for VCCI –0.5 V to 7.0 V

3. VIH(Min) is 2.4V for A42MX36 family. This applies only to VCCI of 5V and is not applicable to VCCI of 3.3V.

4. Dependent upon the chosen package. PCI recommends QFP and BGA packaging to reduce pin inductance and capacitance.

Table 24 • AC Specifications (5.0V PCI Signaling)*

Symbol	Parameter	Condition	PCI		MX		Units
			Min.	Max.	Min.	Max.	
ICL	Low Clamp Current	$-5 < V_{IN} \leq -1$	$-25 + (V_{IN} + 1) / 0.015$		–60	–10	mA
Slew (r)	Output Rise Slew Rate	0.4 V to 2.4 V load	1	5	1.8	2.8	V/ns
Slew (f)	Output Fall Slew Rate	2.4 V to 0.4 V load	1	5	2.8	4.3	V/ns

Note: *PCI Local Bus Specification, Version 2.1, Section 4.2.1.2.

A sample calculation of the absolute maximum power dissipation allowed for a TQ176 package at commercial temperature and still air is given in the following equation

$$\text{MaximumPowerAllowed} = \frac{\text{Max} \cdot \text{junction temp} \cdot (^\circ\text{C}) - \text{Max} \cdot \text{ambient temp} \cdot (^\circ\text{C})}{\theta_{ja}(^\circ\text{C/W})} = \frac{150^\circ\text{C} - 70^\circ\text{C}}{(28^\circ\text{C})/\text{W}} = 2.86\text{W}$$

EQ 5

The maximum power dissipation for military-grade devices is a function of θ_{jc} . A sample calculation of the absolute maximum power dissipation allowed for CQFP 208-pin package at military temperature and still air is given in the following equation

$$\text{MaximumPowerAllowed} = \frac{\text{Max} \cdot \text{junction temp} \cdot (^\circ\text{C}) - \text{Max} \cdot \text{ambient temp} \cdot (^\circ\text{C})}{\theta_{jc}(^\circ\text{C/W})} = \frac{150^\circ\text{C} - 125^\circ\text{C}}{(6.3^\circ\text{C})/\text{W}} = 3.97\text{W}$$

EQ 6

Table 27 • Package Thermal Characteristics

Plastic Packages	Pin Count	θ_{jc}	θ_{ja}			Units
			Still Air	1.0 m/s 200 ft/min.	2.5 m/s 500 ft/min.	
Plastic Quad Flat Pack	100	12.0	27.8	23.4	21.2	$^\circ\text{C/W}$
Plastic Quad Flat Pack	144	10.0	26.2	22.8	21.1	$^\circ\text{C/W}$
Plastic Quad Flat Pack	160	10.0	26.2	22.8	21.1	$^\circ\text{C/W}$
Plastic Quad Flat Pack	208	8.0	26.1	22.5	20.8	$^\circ\text{C/W}$
Plastic Quad Flat Pack	240	8.5	25.6	22.3	20.8	$^\circ\text{C/W}$
Plastic Leaded Chip Carrier	44	16.0	20.0	24.5	22.0	$^\circ\text{C/W}$
Plastic Leaded Chip Carrier	68	13.0	25.0	21.0	19.4	$^\circ\text{C/W}$
Plastic Leaded Chip Carrier	84	12.0	22.5	18.9	17.6	$^\circ\text{C/W}$
Thin Plastic Quad Flat Pack	176	11.0	24.7	19.9	18.0	$^\circ\text{C/W}$
Very Thin Plastic Quad Flat Pack	80	12.0	38.2	31.9	29.4	$^\circ\text{C/W}$
Very Thin Plastic Quad Flat Pack	100	10.0	35.3	29.4	27.1	$^\circ\text{C/W}$
Plastic Ball Grid Array	272	3.0	18.3	14.9	13.9	$^\circ\text{C/W}$
Ceramic Packages						
Ceramic Pin Grid Array	132	4.8	25.0	20.6	18.7	$^\circ\text{C/W}$
Ceramic Quad Flat Pack	208	2.0	22.0	19.8	18.0	$^\circ\text{C/W}$
Ceramic Quad Flat Pack	256	2.0	20.0	16.5	15.0	$^\circ\text{C/W}$

Table 37 • A40MX04 Timing Characteristics (Nominal 3.3 V Operation) (continued)(Worst-Case Commercial Conditions, VCC = 3.0 V, T_J = 70°C)

Parameter / Description			–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Input Module Predicted Routing Delays ¹													
t _{IRD1}	FO = 1 Routing Delay		2.9		3.3		3.8		4.5		6.3		ns
t _{IRD2}	FO = 2 Routing Delay		3.6		4.2		4.8		5.6		7.8		ns
t _{IRD3}	FO = 3 Routing Delay		4.4		5.0		5.7		6.7		9.4		ns
t _{IRD4}	FO = 4 Routing Delay		5.1		5.9		6.7		7.8		11.0		ns
t _{IRD8}	FO = 8 Routing Delay		8.0		9.3		10.5		12.4		17.2		ns
Global Clock Network													
t _{CKH}	Input LOW to HIGH	FO = 16 FO = 128	6.4 6.4		7.4 7.4		8.4 8.4		9.9 9.9		13.8 13.8		ns
t _{CKL}	Input HIGH to LOW	FO = 16 FO = 128	6.8 6.8		7.8 7.8		8.9 8.9		10.4 10.4		14.6 14.6		ns
t _{PWH}	Minimum Pulse Width HIGH	FO = 16 FO = 128	3.1 3.3		3.6 3.8		4.1 4.3		4.8 5.1		6.7 7.1		ns
t _{PWL}	Minimum Pulse Width LOW	FO = 16 FO = 128	3.1 3.3		3.6 3.8		4.1 4.3		4.8 5.1		6.7 7.1		ns
t _{CKSW}	Maximum Skew	FO = 16 FO = 128	0.6 0.8		0.6 0.9		0.7 1.0		0.8 1.2		1.2 1.6		ns
t _P	Minimum Period	FO = 16 FO = 128	6.5 6.8		7.5 7.8		8.5 8.9		10.1 10.4		14.1 14.6		ns
f _{MAX}	Maximum Frequency	FO = 16 FO = 128	113 109		105 101		96 92		83 80		50 48		MHz
TTL Output Module Timing ⁴													
t _{DLH}	Data-to-Pad HIGH		4.7		5.4		6.1		7.2		10.0		ns
t _{DHL}	Data-to-Pad LOW		5.6		6.4		7.3		8.6		12.0		ns
t _{ENZH}	Enable Pad Z to HIGH		5.2		6.0		6.9		8.1		11.3		ns
t _{ENZL}	Enable Pad Z to LOW		6.6		7.6		8.6		10.1		14.1		ns
t _{ENHZ}	Enable Pad HIGH to Z		11.1		12.8		14.5		17.1		23.9		ns
t _{ENLZ}	Enable Pad LOW to Z		8.2		9.5		10.7		12.6		17.7		ns
d _{TLH}	Delta LOW to HIGH		0.03		0.03		0.04		0.04		0.06		ns/pF
d _{THL}	Delta HIGH to LOW		0.04		0.04		0.05		0.06		0.08		ns/pF

Table 39 • A42MX09 Timing Characteristics (Nominal 3.3 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{RD4}	FO = 4 Routing Delay	1.9		2.1		2.4		2.9		4.0		ns
t _{RD8}	FO = 8 Routing Delay	3.2		3.6		4.1		4.8		6.7		ns
Logic Module Sequential Timing ^{3, 4}												
t _{SUD}	Flip-Flop (Latch) Data Input Set-Up	0.5		0.5		0.6		0.7		0.9		ns
t _{HD}	Flip-Flop (Latch) Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{SUENA}	Flip-Flop (Latch) Enable Set-Up	0.6		0.6		0.7		0.8		1.2		ns
t _{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	4.7		5.3		6.0		7.0		9.8		ns
t _{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	6.2		6.9		7.8		9.2		12.9		ns
t _A	Flip-Flop Clock Input Period	5.0		5.6		6.2		7.1		9.9		ns
t _{INH}	Input Buffer Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{INSU}	Input Buffer Latch Set-Up	0.3		0.3		0.3		0.4		0.6		ns
t _{OUTH}	Output Buffer Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{OUTSU}	Output Buffer Latch Set-Up	0.3		0.3		0.3		0.4		0.6		ns
f _{MAX}	Flip-Flop (Latch) Clock Frequency	161		146		135		117		70		MHz

Table 39 • A42MX09 Timing Characteristics (Nominal 3.3 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
CMOS Output Module Timing ⁵												
t _{DLH}	Data-to-Pad HIGH		3.4		3.8		5.5		6.4		9.0	ns
t _{DHL}	Data-to-Pad LOW		4.1		4.5		4.2		5.0		7.0	ns
t _{ENZH}	Enable Pad Z to HIGH		3.7		4.1		4.6		5.5		7.6	ns
t _{ENZL}	Enable Pad Z to LOW		4.1		4.5		5.1		6.1		8.5	ns
t _{ENHZ}	Enable Pad HIGH to Z		6.9		7.6		8.6		10.2		14.2	ns
t _{ENLZ}	Enable Pad LOW to Z		7.5		8.3		9.4		11.1		15.5	ns
t _{GLH}	G-to-Pad HIGH		5.8		6.5		7.3		8.6		12.0	ns
t _{GHL}	G-to-Pad LOW		5.8		6.5		7.3		8.6		12.0	ns
t _{LSU}	I/O Latch Set-Up		0.7		0.8		0.9		1.0		1.4	ns
t _{LH}	I/O Latch Hold		0.0		0.0		0.0		0.0		0.0	ns
t _{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading		8.7		9.7		10.9		12.9		18.0	ns
t _{ACO}	Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading		12.2		13.5		15.4		18.1		25.3	ns
d _{TLH}	Capacity Loading, LOW to HIGH		0.04		0.04		0.05		0.06		0.08	ns/pF
d _{THL}	Capacity Loading, HIGH to LOW		0.05		0.05		0.06		0.07		0.10	ns/pF

1. For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
4. Set-up and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.
5. Delays based on 35 pF loading.

Table 40 • A42MX16 Timing Characteristics (Nominal 5.0 V Operation) (Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units	
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Logic Module Propagation Delays ¹													
t _{PD1}	Single Module		1.4		1.5		1.7		2.0		2.8		ns
t _{CO}	Sequential Clock-to-Q		1.4		1.6		1.8		2.1		3.0		ns
t _{GO}	Latch G-to-Q		1.4		1.5		1.7		2.0		2.8		ns
t _{RS}	Flip-Flop (Latch) Reset-to-Q		1.6		1.7		2.0		2.3		3.3		ns
Logic Module Predicted Routing Delays ²													
t _{RD1}	FO = 1 Routing Delay		0.8		0.9		1.0		1.2		1.6		ns
t _{RD2}	FO = 2 Routing Delay		1.0		1.2		1.3		1.5		2.1		ns

Table 44 • A42MX36 Timing Characteristics (Nominal 5.0 V Operation)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
TTL Output Module Timing ⁵ (Continued)												
t _{ENLZ}	Enable Pad LOW to Z		4.9		5.5		6.2		7.3		10.2	ns
t _{GLH}	G-to-Pad HIGH		2.9		3.3		3.7		4.4		6.1	ns
t _{GHL}	G-to-Pad LOW		2.9		3.3		3.7		4.4		6.1	ns
t _{LSU}	I/O Latch Output Set-Up	0.5		0.5		0.6		0.7		1.0		ns
t _{LH}	I/O Latch Output Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		5.7		6.3		7.1		8.4		11.8	ns
t _{ACO}	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O		7.8		8.6		9.8		11.5		16.1	ns
d _{TLH}	Capacitive Loading, LOW to HIGH		0.07		0.08		0.09		0.10		0.14	ns/pF
d _{THL}	Capacitive Loading, HIGH to LOW		0.07		0.08		0.09		0.10		0.14	ns/pF

Figure 39 • PL68

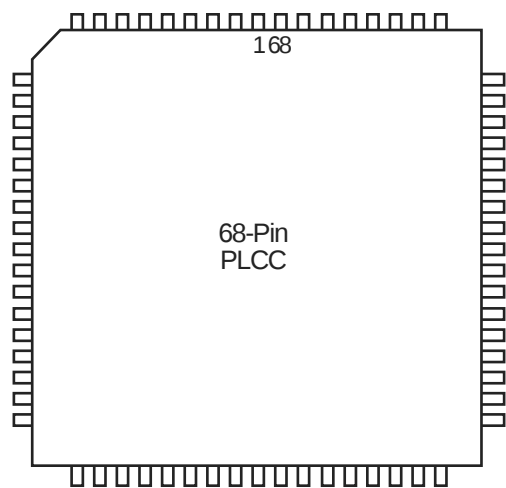


Table 48 • PL68

PL68		
Pin Number	A40MX02 Function	A40MX04 Function
1	I/O	I/O
2	I/O	I/O
3	I/O	I/O
4	VCC	VCC
5	I/O	I/O
6	I/O	I/O
7	I/O	I/O
8	I/O	I/O
9	I/O	I/O
10	I/O	I/O
11	I/O	I/O
12	I/O	I/O
13	I/O	I/O
14	GND	GND
15	GND	GND
16	I/O	I/O
17	I/O	I/O
18	I/O	I/O
19	I/O	I/O
20	I/O	I/O
21	VCC	VCC
22	I/O	I/O
23	I/O	I/O

Table 51 • PQ144

PQ144	
Pin Number	A42MX09 Function
43	I/O
44	GNDQ
45	GNDI
46	NC
47	I/O
48	I/O
49	I/O
50	I/O
51	I/O
52	I/O
53	I/O
54	VCC
55	VCCI
56	NC
57	I/O
58	I/O
59	I/O
60	I/O
61	I/O
62	I/O
63	I/O
64	GND
65	GNDI
66	I/O
67	I/O
68	I/O
69	I/O
70	I/O
71	SDO
72	I/O
73	I/O
74	I/O
75	I/O
76	I/O
77	I/O
78	I/O
79	GNDQ

Table 52 • PQ160

PQ160			
Pin Number	A42MX09 Function	A42MX16 Function	A42MX24 Function
95	I/O	I/O	I/O
96	I/O	I/O	WD, I/O
97	I/O	I/O	I/O
98	VCCA	VCCA	VCCA
99	GND	GND	GND
100	NC	I/O	I/O
101	I/O	I/O	I/O
102	I/O	I/O	I/O
103	NC	I/O	I/O
104	I/O	I/O	I/O
105	I/O	I/O	I/O
106	I/O	I/O	WD, I/O
107	I/O	I/O	WD, I/O
108	I/O	I/O	I/O
109	GND	GND	GND
110	NC	I/O	I/O
111	I/O	I/O	WD, I/O
112	I/O	I/O	WD, I/O
113	I/O	I/O	I/O
114	NC	VCCI	VCCI
115	I/O	I/O	WD, I/O
116	NC	I/O	WD, I/O
117	I/O	I/O	I/O
118	I/O	I/O	TDI, I/O
119	I/O	I/O	TMS, I/O
120	GND	GND	GND
121	I/O	I/O	I/O
122	I/O	I/O	I/O
123	I/O	I/O	I/O
124	NC	I/O	I/O
125	GND	GND	GND
126	I/O	I/O	I/O
127	I/O	I/O	I/O
128	I/O	I/O	I/O
129	NC	I/O	I/O
130	GND	GND	GND
131	I/O	I/O	I/O

Table 53 • PQ208

PQ208			
Pin Number	A42MX16 Function	A42MX24 Function	A42MX36 Function
21	I/O	I/O	I/O
22	GND	GND	GND
23	I/O	I/O	I/O
24	I/O	I/O	I/O
25	I/O	I/O	I/O
26	I/O	I/O	I/O
27	GND	GND	GND
28	VCCI	VCCI	VCCI
29	VCCA	VCCA	VCCA
30	I/O	I/O	I/O
31	I/O	I/O	I/O
32	VCCA	VCCA	VCCA
33	I/O	I/O	I/O
34	I/O	I/O	I/O
35	I/O	I/O	I/O
36	I/O	I/O	I/O
37	I/O	I/O	I/O
38	I/O	I/O	I/O
39	I/O	I/O	I/O
40	I/O	I/O	I/O
41	NC	I/O	I/O
42	NC	I/O	I/O
43	NC	I/O	I/O
44	I/O	I/O	I/O
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	I/O	I/O	I/O
48	I/O	I/O	I/O
49	I/O	I/O	I/O
50	NC	I/O	I/O
51	NC	I/O	I/O
52	GND	GND	GND
53	GND	GND	GND
54	I/O	TMS, I/O	TMS, I/O
55	I/O	TDI, I/O	TDI, I/O
56	I/O	I/O	I/O
57	I/O	WD, I/O	WD, I/O

Table 53 • PQ208

PQ208			
Pin Number	A42MX16 Function	A42MX24 Function	A42MX36 Function
132	VCCI	VCCI	VCCI
133	VCCA	VCCA	VCCA
134	I/O	I/O	I/O
135	I/O	I/O	I/O
136	VCCA	VCCA	VCCA
137	I/O	I/O	I/O
138	I/O	I/O	I/O
139	I/O	I/O	I/O
140	I/O	I/O	I/O
141	NC	I/O	I/O
142	I/O	I/O	I/O
143	I/O	I/O	I/O
144	I/O	I/O	I/O
145	I/O	I/O	I/O
146	NC	I/O	I/O
147	NC	I/O	I/O
148	NC	I/O	I/O
149	NC	I/O	I/O
150	GND	GND	GND
151	I/O	I/O	I/O
152	I/O	I/O	I/O
153	I/O	I/O	I/O
154	I/O	I/O	I/O
155	I/O	I/O	I/O
156	I/O	I/O	I/O
157	GND	GND	GND
158	I/O	I/O	I/O
159	SDI, I/O	SDI, I/O	SDI, I/O
160	I/O	I/O	I/O
161	I/O	WD, I/O	WD, I/O
162	I/O	WD, I/O	WD, I/O
163	I/O	I/O	I/O
164	VCCI	VCCI	VCCI
165	NC	I/O	I/O
166	NC	I/O	I/O
167	I/O	I/O	I/O
168	I/O	WD, I/O	WD, I/O

Table 54 • PQ240

PQ240	
Pin Number	A42MX36 Function
89	VCCI
90	VCCA
91	LP
92	TCK, I/O
93	I/O
94	GND
95	I/O
96	I/O
97	I/O
98	I/O
99	I/O
100	I/O
101	I/O
102	I/O
103	I/O
104	I/O
105	I/O
106	I/O
107	I/O
108	VCCI
109	I/O
110	I/O
111	I/O
112	I/O
113	I/O
114	I/O
115	I/O
116	I/O
117	I/O
118	VCCA
119	GND
120	GND
121	GND
122	I/O
123	SDO, TDO, I/O
124	I/O
125	WD, I/O

Table 55 • VQ80

VQ80		
Pin Number	A40MX02 Function	A40MX04 Function
49	I/O	I/O
50	CLK, I/O	CLK, I/O
51	I/O	I/O
52	MODE	MODE
53	VCC	VCC
54	NC	I/O
55	NC	I/O
56	NC	I/O
57	SDI, I/O	SDI, I/O
58	DCLK, I/O	DCLK, I/O
59	PRA, I/O	PRA, I/O
60	NC	NC
61	PRB, I/O	PRB, I/O
62	I/O	I/O
63	I/O	I/O
64	I/O	I/O
65	I/O	I/O
66	I/O	I/O
67	I/O	I/O
68	GND	GND
69	I/O	I/O
70	I/O	I/O
71	I/O	I/O
72	I/O	I/O
73	I/O	I/O
74	VCC	VCC
75	I/O	I/O
76	I/O	I/O
77	I/O	I/O
78	I/O	I/O
79	I/O	I/O
80	I/O	I/O

Table 56 • VQ100

VQ100		
Pin Number	A42MX09 Function	A42MX16 Function
21	I/O	I/O
22	I/O	I/O
23	I/O	I/O
24	I/O	I/O
25	I/O	I/O
26	I/O	I/O
27	I/O	I/O
28	I/O	I/O
29	I/O	I/O
30	I/O	I/O
31	I/O	I/O
32	GND	GND
33	I/O	I/O
34	I/O	I/O
35	I/O	I/O
36	I/O	I/O
37	I/O	I/O
38	VCCA	VCCA
39	I/O	I/O
40	I/O	I/O
41	I/O	I/O
42	I/O	I/O
43	I/O	I/O
44	GND	GND
45	I/O	I/O
46	I/O	I/O
47	I/O	I/O
48	I/O	I/O
49	I/O	I/O
50	SDO, I/O	SDO, I/O
51	I/O	I/O
52	I/O	I/O
53	I/O	I/O
54	I/O	I/O
55	GND	GND
56	I/O	I/O

Table 57 • TQ176

TQ176			
Pin Number	A42MX09 Function	A42MX16 Function	A42MX24 Function
47	I/O	I/O	TDI, I/O
48	I/O	I/O	I/O
49	I/O	I/O	WD, I/O
50	I/O	I/O	WD, I/O
51	I/O	I/O	I/O
52	NC	VCCI	VCCI
53	I/O	I/O	I/O
54	NC	I/O	I/O
55	NC	I/O	WD, I/O
56	I/O	I/O	WD, I/O
57	NC	NC	I/O
58	I/O	I/O	I/O
59	I/O	I/O	WD, I/O
60	I/O	I/O	WD, I/O
61	NC	I/O	I/O
62	I/O	I/O	I/O
63	I/O	I/O	I/O
64	NC	I/O	I/O
65	I/O	I/O	I/O
66	NC	I/O	I/O
67	GND	GND	GND
68	VCCA	VCCA	VCCA
69	I/O	I/O	WD, I/O
70	I/O	I/O	WD, I/O
71	I/O	I/O	I/O
72	I/O	I/O	I/O
73	I/O	I/O	I/O
74	NC	I/O	I/O
75	I/O	I/O	I/O
76	I/O	I/O	I/O
77	NC	NC	WD, I/O
78	NC	I/O	WD, I/O
79	I/O	I/O	I/O
80	NC	I/O	I/O
81	I/O	I/O	I/O
82	NC	VCCI	VCCI
83	I/O	I/O	I/O

Table 57 • TQ176

TQ176			
Pin Number	A42MX09 Function	A42MX16 Function	A42MX24 Function
121	NC	NC	I/O
122	I/O	I/O	I/O
123	I/O	I/O	I/O
124	NC	I/O	I/O
125	NC	I/O	I/O
126	NC	NC	I/O
127	I/O	I/O	I/O
128	I/O	I/O	I/O
129	I/O	I/O	I/O
130	I/O	I/O	I/O
131	I/O	I/O	I/O
132	I/O	I/O	I/O
133	GND	GND	GND
134	I/O	I/O	I/O
135	SDI, I/O	SDI, I/O	SDI, I/O
136	NC	I/O	I/O
137	I/O	I/O	WD, I/O
138	I/O	I/O	WD, I/O
139	I/O	I/O	I/O
140	NC	VCCI	VCCI
141	I/O	I/O	I/O
142	I/O	I/O	I/O
143	NC	I/O	I/O
144	NC	I/O	WD, I/O
145	NC	NC	WD, I/O
146	I/O	I/O	I/O
147	NC	I/O	I/O
148	I/O	I/O	I/O
149	I/O	I/O	I/O
150	I/O	I/O	WD, I/O
151	NC	I/O	WD, I/O
152	PRA, I/O	PRA, I/O	PRA, I/O
153	I/O	I/O	I/O
154	CLKA, I/O	CLKA, I/O	CLKA, I/O
155	VCCA	VCCA	VCCA
156	GND	GND	GND
157	I/O	I/O	I/O

Table 57 • TQ176

TQ176			
Pin Number	A42MX09 Function	A42MX16 Function	A42MX24 Function
158	CLKB, I/O	CLKB, I/O	CLKB, I/O
159	I/O	I/O	I/O
160	PRB, I/O	PRB, I/O	PRB, I/O
161	NC	I/O	WD, I/O
162	I/O	I/O	WD, I/O
163	I/O	I/O	I/O
164	I/O	I/O	I/O
165	NC	NC	WD, I/O
166	NC	I/O	WD, I/O
167	I/O	I/O	I/O
168	NC	I/O	I/O
169	I/O	I/O	I/O
170	NC	VCCI	VCCI
171	I/O	I/O	WD, I/O
172	I/O	I/O	WD, I/O
173	NC	I/O	I/O
174	I/O	I/O	I/O
175	DCLK, I/O	DCLK, I/O	DCLK, I/O
176	I/O	I/O	I/O

Figure 49 • CQ208