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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | - |
| Number of I/O | 57 |
| Number of Gates | 3000 |
| Voltage - Supply | 3V ~ 3.6V, 4.75V ~ 5.25V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Package / Case | 80-TQFP |
| Supplier Device Package | 80-VQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/a40mx02-2vqg80 |

- The Transient Current, page 13 is new (SAR 36930).
- Package names were revised according to standards established in *Package Mechanical Drawings* (SAR 34774)

## 1.7 Revision 9.0

The following is a summary of the changes in revision 9.0 of this document

- In Table 20, page 23, the limits in VI were changed from -0.5 to VCCI + 0.5 to -0.5 to VCCA + 0.5

In Table 22, page 25, $V_{OH}$ was changed from 3.7 to 2.4 for the min in industrial and military. $V_{IH}$ had $V_{CCI}$ and that was changed to VCCA

## 1.8 Revision 6.0

The following is a summary of the changes in revision 6.0 of this document.

- The Ease of Integration, page 1 was updated
- The Temperature Grade Offerings, page 5 is new
- The Speed Grade Offerings, page 5 is new
- The General Description, page 6 was updated
- The MultiPlex I/O Modules, page 11 was updated
- The User Security, page 12 was updated
- Table 6, page 13 was updated
- The Power Dissipation, page 14 was updated.
- The Static Power Component, page 14 was updated
- The Equivalent Capacitance, page 15 was updated
- Figure 13, page 17 was updated
- Table 10, page 18 was updated.
- Figure 14, page 18 was updated.
- Table 11, page 19 was updated.

A sample calculation of the absolute maximum power dissipation allowed for a TQ176 package at commercial temperature and still air is given in the following equation

$$\text{MaximumPowerAllowed} = \frac{\text{Max} \cdot \text{junction temp} \cdot (°\text{C}) - \text{Max} \cdot \text{ambient temp} \cdot (°\text{C})}{\theta_{ja}(°(\text{C}/\text{W}))} = \frac{150°\text{C} - 70°\text{C}}{(28°\text{C})/\text{W}} = 2.86\text{W}$$

**EQ 5**

The maximum power dissipation for military-grade devices is a function of $\theta_{jc}$. A sample calculation of the absolute maximum power dissipation allowed for CQFP 208-pin package at military temperature and still air is given in the following equation

$$\text{MaximumPowerAllowed} = \frac{\text{Max} \cdot \text{junction temp} \cdot (°\text{C}) - \text{Max} \cdot \text{ambient temp} \cdot (°\text{C})}{\theta_{jc}(°(\text{C}/\text{W}))} = \frac{150°\text{C} - 125°\text{C}}{(6.3°\text{C})/\text{W}} = 3.97\text{W}$$

**EQ 6**

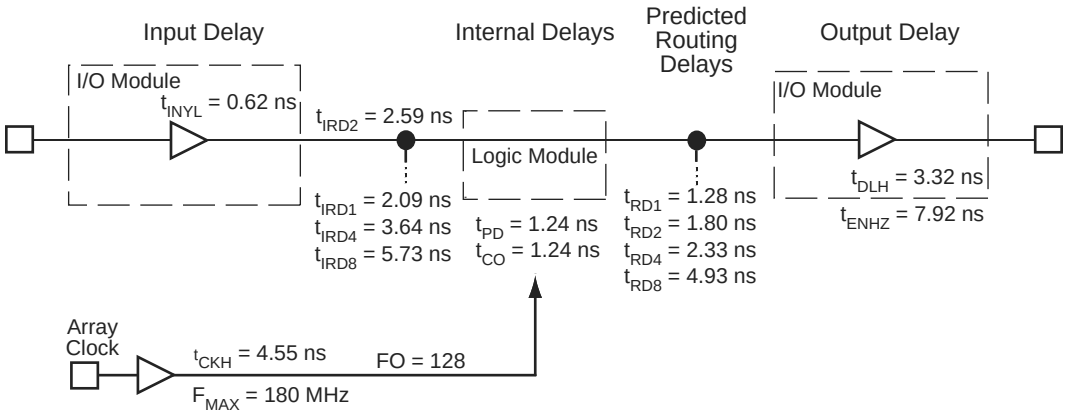
***Table 27 •*** **Package Thermal Characteristics**

| | | | $\theta_{ja}$ | | | |
|---|---|---|---|---|---|---|
| **Plastic Packages** | **Pin Count** | $\theta_{jc}$ | **Still Air** | **1.0 m/s 200 ft/min.** | **2.5 m/s 500 ft/min.** | **Units** |
| Plastic Quad Flat Pack | 100 | 12.0 | 27.8 | 23.4 | 21.2 | °C/W |
| Plastic Quad Flat Pack | 144 | 10.0 | 26.2 | 22.8 | 21.1 | °C/W |
| Plastic Quad Flat Pack | 160 | 10.0 | 26.2 | 22.8 | 21.1 | °C/W |
| Plastic Quad Flat Pack | 208 | 8.0 | 26.1 | 22.5 | 20.8 | °C/W |
| Plastic Quad Flat Pack | 240 | 8.5 | 25.6 | 22.3 | 20.8 | °C/W |
| Plastic Leaded Chip Carrier | 44 | 16.0 | 20.0 | 24.5 | 22.0 | °C/W |
| Plastic Leaded Chip Carrier | 68 | 13.0 | 25.0 | 21.0 | 19.4 | °C/W |
| Plastic Leaded Chip Carrier | 84 | 12.0 | 22.5 | 18.9 | 17.6 | °C/W |
| Thin Plastic Quad Flat Pack | 176 | 11.0 | 24.7 | 19.9 | 18.0 | °C/W |
| Very Thin Plastic Quad Flat Pack | 80 | 12.0 | 38.2 | 31.9 | 29.4 | °C/W |
| Very Thin Plastic Quad Flat Pack | 100 | 10.0 | 35.3 | 29.4 | 27.1 | °C/W |
| Plastic Ball Grid Array | 272 | 3.0 | 18.3 | 14.9 | 13.9 | °C/W |
| **Ceramic Packages** | | | | | | |
| Ceramic Pin Grid Array | 132 | 4.8 | 25.0 | 20.6 | 18.7 | °C/W |
| Ceramic Quad Flat Pack | 208 | 2.0 | 22.0 | 19.8 | 18.0 | °C/W |
| Ceramic Quad Flat Pack | 256 | 2.0 | 20.0 | 16.5 | 15.0 | °C/W |

# 3.10 Timing Models

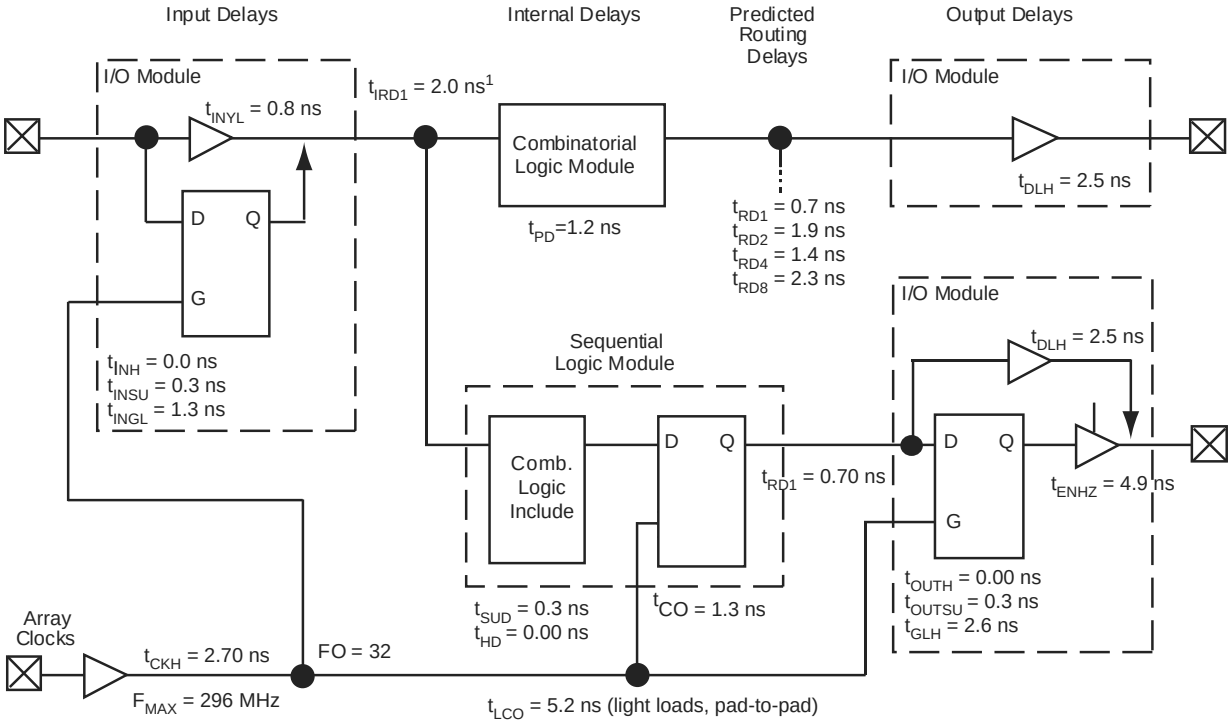
The following figures show various timing models.

***Figure 17 •*** **40MX Timing Model***




**Note:** Values are shown for 40MX –3 speed devices at 5.0 V worst-case commercial conditions.

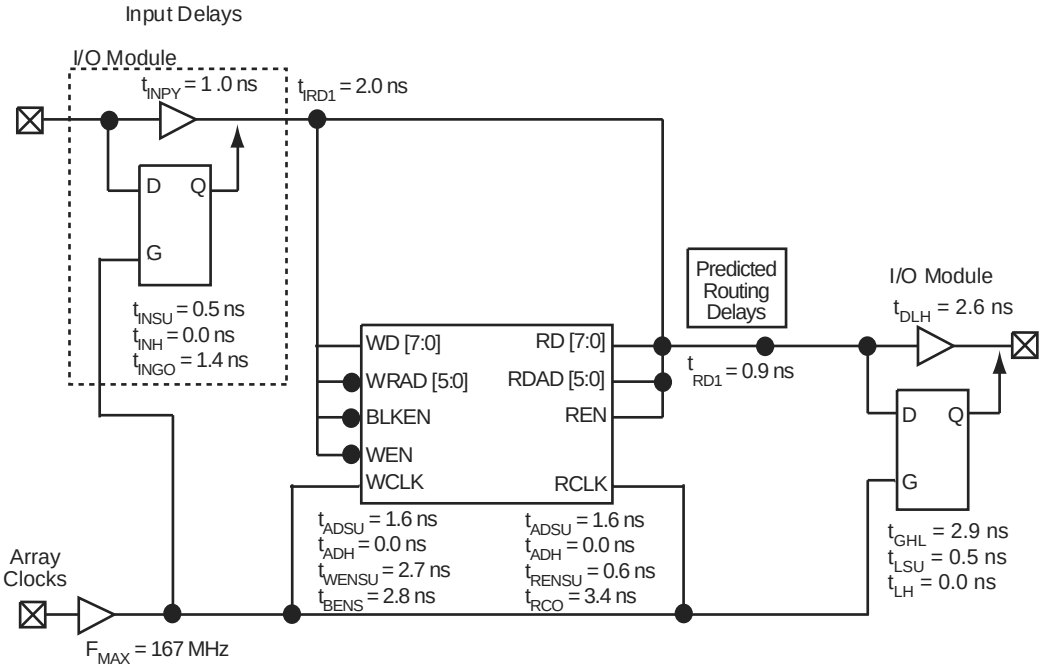
***Figure 18 •*** **42MX Timing Model**




**Note:** 1. Input module predicted routing delay

**Note:** 2. Values are shown for A42MX09 –3 at 5.0 V worst-case commercial conditions.

***Figure 20 •*** **42MX Timing Model (SRAM Functions)**

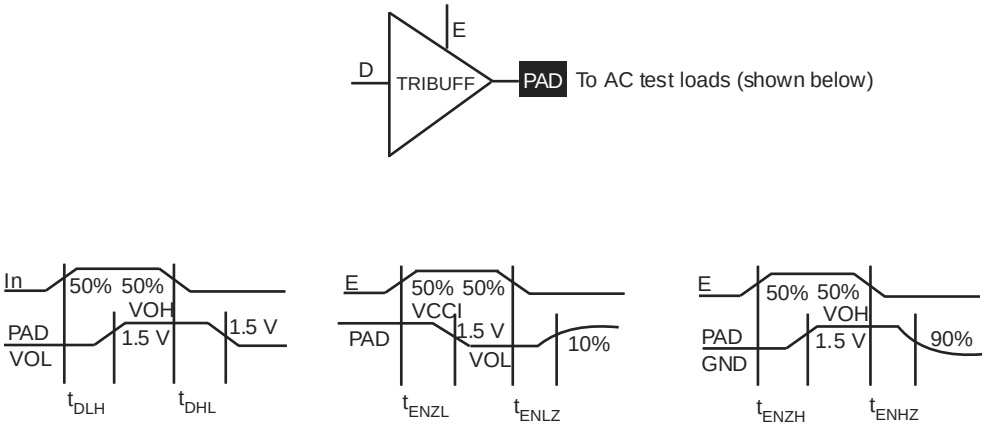



**Note:** Values are shown for A42MX36 –3 at 5.0 V worst-case commercial conditions.

## 3.10.1 Parameter Measurement

The following figures show parameter measurement details.

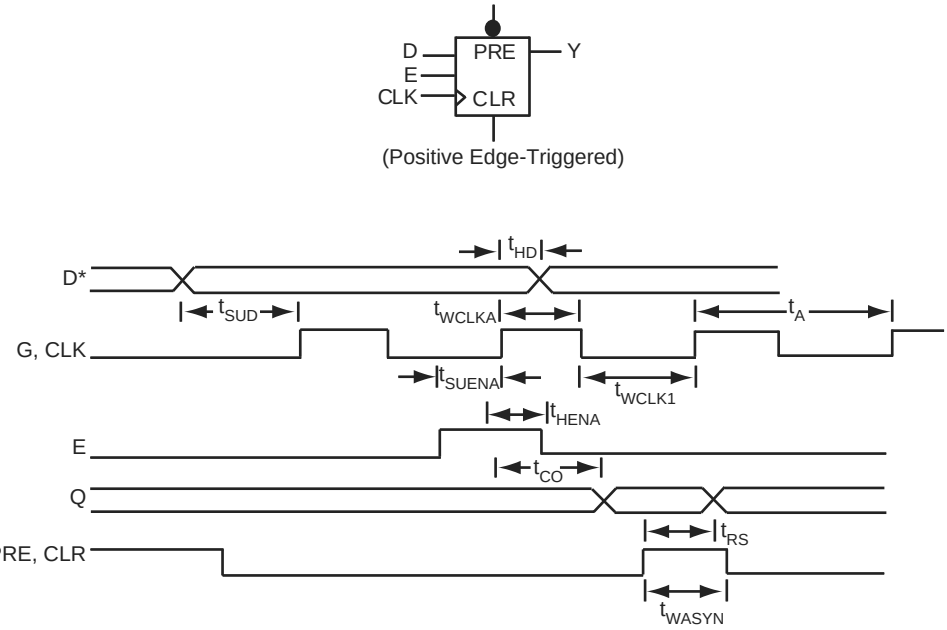
***Figure 21 •*** **Output Buffer Delays**



## 3.10.2 Sequential Module Timing Characteristics

The following figure shows sequential module timing characteristics.

***Figure 25 •*** **Flip-Flops and Latches**




**Note:** *D represents all data functions involving A, B, and S for multiplexed flip-flops.

## 3.10.3 Sequential Timing Characteristics

The following figures show sequential timing characteristics.

***Figure 26 •*** **Input Buffer Latches**

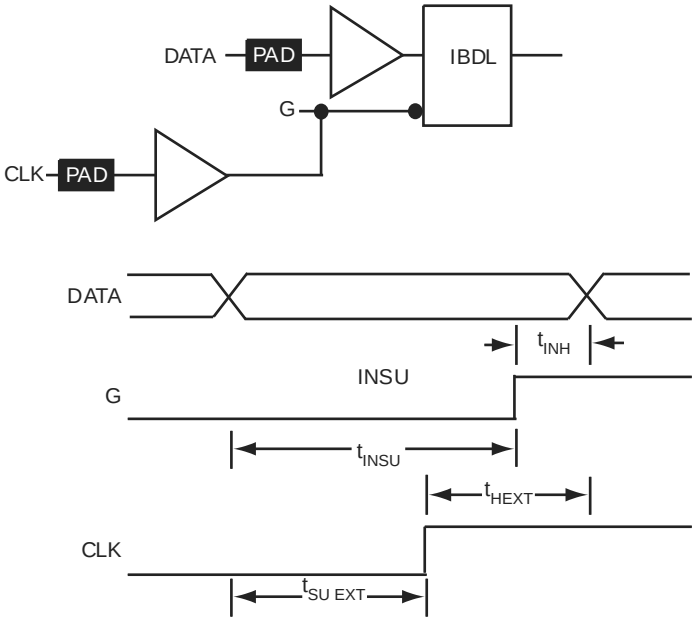
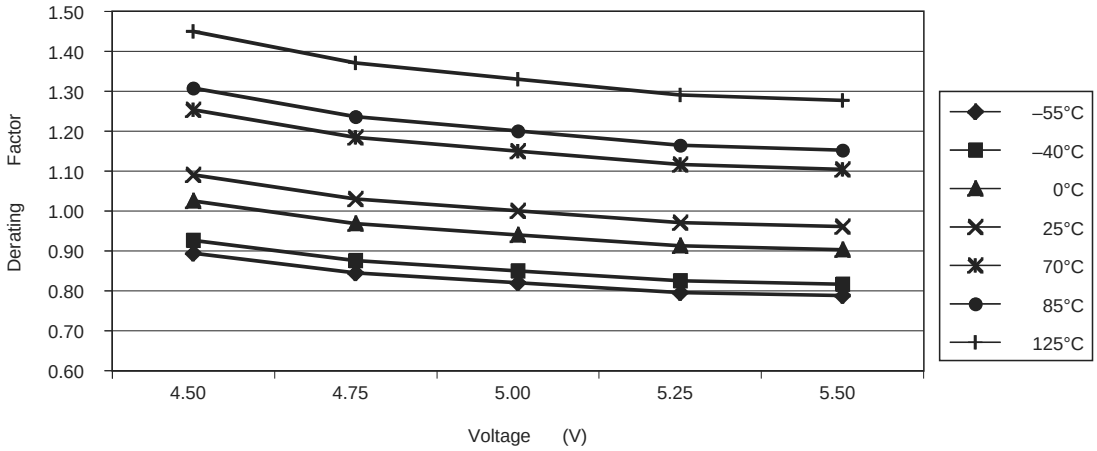


***Figure 35 •*** **40MX Junction Temperature and Voltage Derating Curves (Normalized to TJ = 25°C, VCC = 5.0 V)**

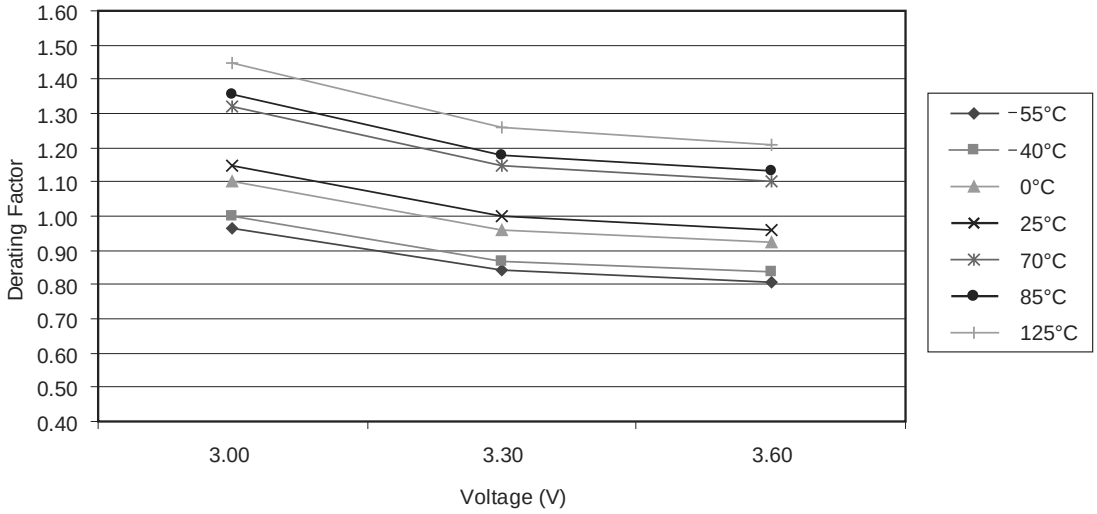



**Note:** This derating factor applies to all routing and propagation delays

***Table 30 •*** **42MX Temperature and Voltage Derating Factors(Normalized to TJ = 25°C, VCCA = 3.3 V)**

| | Temperature | | | | | | |
|---|---|---|---|---|---|---|---|
| **42MX Voltage** | **–55°C** | **–40°C** | **0°C** | **25°C** | **70°C** | **85°C** | **125°C** |
| 3.00 | 0.97 | 1.00 | 1.10 | 1.15 | 1.32 | 1.36 | 1.45 |
| 3.30 | 0.84 | 0.87 | 0.96 | 1.00 | 1.15 | 1.18 | 1.26 |
| 3.60 | 0.81 | 0.84 | 0.92 | 0.96 | 1.10 | 1.13 | 1.21 |

***Figure 36 •*** **42MX Junction Temperature and Voltage Derating Curves (Normalized to TJ = 25°C, VCCA = 3.3 V)**




**Note:** This derating factor applies to all routing and propagation delays

***Table 31 •*** **40MX Temperature and Voltage Derating Factors (Normalized to TJ = 25°C, VCC = 3.3 V)**

| | Temperature | | | | | | |
|---|---|---|---|---|---|---|---|
| **40MX Voltage** | **–55°C** | **–40°C** | **0°C** | **25°C** | **70°C** | **85°C** | **125°C** |
| 3.00 | 1.08 | 1.12 | 1.21 | 1.26 | 1.50 | 1.64 | 2.00 |
| 3.30 | 0.86 | 0.89 | 0.96 | 1.00 | 1.19 | 1.30 | 1.59 |

***Table 35 •*** **A40MX02 Timing Characteristics (Nominal 3.3 V Operation) *(continued)***
**(Worst-Case Commercial Conditions, VCC = 3.0 V, $T_J$ = 70°C)**

| Parameter / Description | | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{RD1}$ | FO = 1 Routing Delay | | | 2.0 | | 2.2 | | 2.5 | | 3.0 | | 4.2 | ns |
| $t_{RD2}$ | FO = 2 Routing Delay | | | 2.7 | | 3.1 | | 3.5 | | 4.1 | | 5.7 | ns |
| $t_{RD3}$ | FO = 3 Routing Delay | | | 3.4 | | 3.9 | | 4.4 | | 5.2 | | 7.3 | ns |
| $t_{RD4}$ | FO = 4 Routing Delay | | | 4.2 | | 4.8 | | 5.4 | | 6.3 | | 8.9 | ns |
| $t_{RD8}$ | FO = 8 Routing Delay | | | 7.1 | | 8.2 | | 9.2 | | 10.9 | | 15.2 | ns |
| **Logic Module Sequential Timing[2]** | | | | | | | | | | | | | |
| $t_{SUD}$ | Flip-Flop (Latch) Data Input Set-Up | | 4.3 | | 4.9 | | 5.6 | | 6.6 | | 9.2 | | ns |
| $t_{HD}$[3] | Flip-Flop (Latch) Data Input Hold | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{SUENA}$ | Flip-Flop (Latch) Enable Set-Up | | 4.3 | | 4.9 | | 5.6 | | 6.6 | | 9.2 | | ns |
| $t_{HENA}$ | Flip-Flop (Latch) Enable Hold | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{WCLKA}$ | Flip-Flop (Latch) Clock Active Pulse Width | | 4.6 | | 5.3 | | 6.0 | | 7.0 | | 9.8 | | ns |
| $t_{WASYN}$ | Flip-Flop (Latch) Asynchronous Pulse Width | | 4.6 | | 5.3 | | 6.0 | | 7.0 | | 9.8 | | ns |
| $t_A$ | Flip-Flop Clock Input Period | | 6.8 | | 7.8 | | 8.9 | | 10.4 | | 14.6 | | ns |
| $f_{MAX}$ | Flip-Flop (Latch) Clock Frequency (FO = 128) | | | 109 | | 101 | | 92 | | 80 | | 48 | MHz |
| **Input Module Propagation Delays** | | | | | | | | | | | | | |
| $t_{INYH}$ | Pad-to-Y HIGH | | | 1.0 | | 1.1 | | 1.3 | | 1.5 | | 2.1 | ns |
| $t_{INYL}$ | Pad-to-Y LOW | | | 0.9 | | 1.0 | | 1.1 | | 1.3 | | 1.9 | ns |
| **Input Module Predicted Routing Delays[1]** | | | | | | | | | | | | | |
| $t_{IRD1}$ | FO = 1 Routing Delay | | | 2.9 | | 3.4 | | 3.8 | | 4.5 | | 6.3 | ns |
| $t_{IRD2}$ | FO = 2 Routing Delay | | | 3.6 | | 4.2 | | 4.8 | | 5.6 | | 7.8 | ns |
| $t_{IRD3}$ | FO = 3 Routing Delay | | | 4.4 | | 5.0 | | 5.7 | | 6.7 | | 9.4 | ns |
| $t_{IRD4}$ | FO = 4 Routing Delay | | | 5.1 | | 5.9 | | 6.7 | | 7.8 | | 11.0 | ns |
| $t_{IRD8}$ | FO = 8 Routing Delay | | | 8.0 | | 9.26 | | 10.5 | | 12.6 | | 17.3 | ns |
| **Global Clock Network** | | | | | | | | | | | | | |
| $t_{CKH}$ | Input LOW to HIGH | FO = 16<br>FO = 128 | | 6.4<br>6.4 | | 7.4<br>7.4 | | 8.3<br>8.3 | | 9.8<br>9.8 | | 13.7<br>13.7 | ns |
| $t_{CKL}$ | Input HIGH to LOW | FO = 16<br>FO = 128 | | 6.7<br>6.7 | | 7.8<br>7.8 | | 8.8<br>8.8 | | 10.4<br>10.4 | | 14.5<br>14.5 | ns |
| $t_{PWH}$ | Minimum Pulse Width HIGH | FO = 16<br>FO = 128 | 3.1<br>3.3 | | 3.6<br>3.8 | | 4.1<br>4.3 | | 4.8<br>5.1 | | 6.7<br>7.1 | | ns |
| $t_{PWL}$ | Minimum Pulse Width LOW | FO = 16<br>FO = 128 | 3.1<br>3.3 | | 3.6<br>3.8 | | 4.1<br>4.3 | | 4.8<br>5.1 | | 6.7<br>7.1 | | ns |
| $t_{CKSW}$ | Maximum Skew | FO = 16<br>FO = 128 | | 0.6<br>0.8 | | 0.6<br>0.9 | | 0.7<br>1.0 | | 0.8<br>1.2 | | 1.2<br>1.6 | ns |

***Table 42 •*** **A42MX24 Timing Characteristics (Nominal 5.0 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 4.75 V, $T_J$ = 70°C)**

| | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter / Description** | | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| **Input Module Propagation Delays** | | | | | | | | | | | | |
| $t_{INPY}$ | Input Data Pad-to-Y | | 1.0 | | 1.1 | | 1.3 | | 1.5 | | 2.1 | ns |
| $t_{INGO}$ | Input Latch Gate-to-Output | | 1.3 | | 1.4 | | 1.6 | | 1.9 | | 2.6 | ns |
| $t_{INH}$ | Input Latch Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{INSU}$ | Input Latch Set-Up | 0.5 | | 0.5 | | 0.6 | | 0.7 | | 1.0 | | ns |
| $t_{ILA}$ | Latch Active Pulse Width | 4.7 | | 5.2 | | 5.9 | | 6.9 | | 9.7 | | ns |

***Table 44 •*** **A42MX36 Timing Characteristics (Nominal 5.0 V Operation)(Worst-Case Commercial Conditions, VCCA = 4.75 V, $T_J$ = 70°C)**

| Parameter / Description | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Logic Module Combinatorial Functions[1]** | | | | | | | | | | | | |
| $t_{PD}$ | Internal Array Module Delay | | 1.3 | | 1.5 | | 1.7 | | 2.0 | | 2.7 | ns |
| $t_{PDD}$ | Internal Decode Module Delay | | 1.6 | | 1.8 | | 2.0 | | 2.4 | | 3.3 | ns |
| **Logic Module Predicted Routing Delays[2]** | | | | | | | | | | | | |
| $t_{RD1}$ | FO = 1 Routing Delay | | 0.9 | | 1.0 | | 1.2 | | 1.4 | | 2.0 | ns |
| $t_{RD2}$ | FO = 2 Routing Delay | | 1.3 | | 1.4 | | 1.6 | | 1.9 | | 2.7 | ns |
| $t_{RD3}$ | FO =3 Routing Delay | | 1.6 | | 1.8 | | 2.0 | | 2.4 | | 3.4 | ns |
| $t_{RD4}$ | FO = 4 Routing Delay | | 2.0 | | 2.2 | | 2.5 | | 2.9 | | 4.1 | ns |
| $t_{RD5}$ | FO = 8 Routing Delay | | 3.3 | | 3.7 | | 4.2 | | 4.9 | | 6.9 | ns |
| $t_{RDD}$ | Decode-to-Output Routing Delay | | 0.3 | | 0.4 | | 0.4 | | 0.5 | | 0.7 | ns |
| **Logic Module Sequential Timing[3, 4]** | | | | | | | | | | | | |
| $t_{CO}$ | Flip-Flop Clock-to-Output | | 1.3 | | 1.4 | | 1.6 | | 1.9 | | 2.7 | ns |
| $t_{GO}$ | Latch Gate-to-Output | | 1.3 | | 1.4 | | 1.6 | | 1.9 | | 2.7 | ns |
| $t_{SUD}$ | Flip-Flop (Latch) Set-Up Time | 0.3 | | 0.3 | | 0.4 | | 0.5 | | 0.7 | | ns |
| $t_{HD}$ | Flip-Flop (Latch) Hold Time | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{RO}$ | Flip-Flop (Latch) Reset-to-Output | | 1.6 | | 1.7 | | 2.0 | | 2.3 | | 3.2 | ns |
| $t_{SUENA}$ | Flip-Flop (Latch) Enable Set-Up | 0.7 | | 0.8 | | 0.9 | | 1.0 | | 1.4 | | ns |
| $t_{HENA}$ | Flip-Flop (Latch) Enable Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{WCLKA}$ | Flip-Flop (Latch) Clock Active Pulse Width | 3.3 | | 3.7 | | 4.2 | | 4.9 | | 6.9 | | ns |
| $t_{WASYN}$ | Flip-Flop (Latch) Asynchronous Pulse Width | 4.4 | | 4.8 | | 5.5 | | 6.4 | | 9.0 | | ns |
| **Synchronous SRAM Operations** | | | | | | | | | | | | |
| $t_{RC}$ | Read Cycle Time | 6.8 | | 7.5 | | 8.5 | | 10.0 | | 14.0 | | ns |
| $t_{WC}$ | Write Cycle Time | 6.8 | | 7.5 | | 8.5 | | 10.0 | | 14.0 | | ns |
| $t_{RCKHL}$ | Clock HIGH/LOW Time | 3.4 | | 3.8 | | 4.3 | | 5.0 | | 7.0 | | ns |
| $t_{RCO}$ | Data Valid After Clock HIGH/LOW | | 3.4 | | 3.8 | | 4.3 | | 5.0 | | 7.0 | ns |
| $t_{ADSU}$ | Address/Data Set-Up Time | 1.6 | | 1.8 | | 2.0 | | 2.4 | | 3.4 | | ns |
| **Synchronous SRAM Operations (continued)** | | | | | | | | | | | | |
| $t_{ADH}$ | Address/Data Hold Time | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{RENSU}$ | Read Enable Set-Up | 0.6 | | 0.7 | | 0.8 | | 0.9 | | 1.3 | | ns |
| $t_{RENH}$ | Read Enable Hold | 3.4 | | 3.8 | | 4.3 | | 5.0 | | 7.0 | | ns |
| $t_{WENSU}$ | Write Enable Set-Up | 2.7 | | 3.0 | | 3.4 | | 4.0 | | 5.6 | | ns |
| $t_{WENH}$ | Write Enable Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{BENS}$ | Block Enable Set-Up | 2.8 | | 3.1 | | 3.5 | | 4.1 | | 5.7 | | ns |
| $t_{BENH}$ | Block Enable Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |

***Table 45 •*** **A42MX36 Timing Characteristics (Nominal 3.3 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 3.0 V, $T_J$ = 70°C)**

| Parameter / Description | | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Input Module Predicted Routing Delays[2]** | | | | | | | | | | | | | |
| $t_{IRD1}$ | FO = 1 Routing Delay | | | 2.8 | | 3.1 | | 3.5 | | 4.1 | | 5.7 | ns |
| $t_{IRD2}$ | FO = 2 Routing Delay | | | 3.2 | | 3.5 | | 4.1 | | 4.8 | | 6.7 | ns |
| $t_{IRD3}$ | FO = 3 Routing Delay | | | 3.7 | | 4.1 | | 4.7 | | 5.5 | | 7.7 | ns |
| $t_{IRD4}$ | FO = 4 Routing Delay | | | 4.2 | | 4.6 | | 5.3 | | 6.2 | | 8.7 | ns |
| $t_{IRD8}$ | FO = 8 Routing Delay | | | 6.1 | | 6.8 | | 7.7 | | 9.0 | | 12.6 | ns |
| **Global Clock Network** | | | | | | | | | | | | | |
| $t_{CKH}$ | Input LOW to HIGH | FO = 32 | | 4.6 | | 5.1 | | 5.7 | | 6.7 | | 9.3 | ns |
| | | FO = 635 | | 5.0 | | 5.6 | | 6.3 | | 7.4 | | 10.3 | ns |
| $t_{CKL}$ | Input HIGH to LOW | FO = 32 | | 5.3 | | 5.9 | | 6.7 | | 7.8 | | 11.0 | ns |
| | | FO = 635 | | 6.8 | | 7.6 | | 8.6 | | 10.1 | | 14.1 | ns |
| $t_{PWH}$ | Minimum Pulse Width HIGH | FO = 32 | 2.5 | | 2.7 | | 3.1 | | 3.6 | | 5.1 | | ns |
| | | FO = 635 | 2.8 | | 3.1 | | 3.5 | | 4.1 | | 5.7 | | ns |
| $t_{PWL}$ | Minimum Pulse Width LOW | FO = 32 | 2.5 | | 2.7 | | 3.1 | | 3.6 | | 5.1 | | ns |
| | | FO = 635 | 2.8 | | 3.1 | | 3.5 | | 4.1 | | 5.7 | | ns |
| $t_{CKSW}$ | Maximum Skew | FO = 32 | | 1.0 | | 1.2 | | 1.3 | | 1.5 | | 2.2 | ns |
| | | FO = 635 | | 1.0 | | 1.2 | | 1.3 | | 1.5 | | 2.2 | ns |
| $t_{SUEXT}$ | Input Latch External Set-Up | FO = 32 | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| | | FO = 635 | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{HEXT}$ | Input Latch External Hold | FO = 32 | 4.0 | | 4.4 | | 5.0 | | 5.9 | | 8.2 | | ns |
| | | FO = 635 | 4.6 | | 5.2 | | 5.9 | | 6.9 | | 9.6 | | ns |
| $t_P$ | Minimum Period ($1/f_{MAX}$) | FO = 32 | 9.2 | | 10.2 | | 11.1 | | 12.7 | | 21.2 | | ns |
| | | FO = 635 | 9.9 | | 11.0 | | 12.0 | | 13.8 | | 23.0 | | ns |
| $f_{MAX}$ | Maximum Datapath Frequency | FO = 32 | | 108 | | 98 | | 90 | | 79 | | 47 | MHz |
| | | FO = 635 | | 100 | | 91 | | 83 | | 73 | | 44 | MHz |
| **TTL Output Module Timing[5]** | | | | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad HIGH | | | 3.6 | | 4.0 | | 4.5 | | 5.3 | | 7.4 | ns |
| $t_{DHL}$ | Data-to-Pad LOW | | | 4.2 | | 4.6 | | 5.2 | | 6.2 | | 8.6 | ns |
| $t_{ENZH}$ | Enable Pad Z to HIGH | | | 3.7 | | 4.2 | | 4.7 | | 5.5 | | 7.7 | ns |
| $t_{ENZL}$ | Enable Pad Z to LOW | | | 4.1 | | 4.6 | | 5.2 | | 6.1 | | 8.5 | ns |
| $t_{ENHZ}$ | Enable Pad HIGH to Z | | | 7.34 | | 8.2 | | 9.3 | | 10.9 | | 15.3 | ns |
| **TTL Output Module Timing[5]** | | | | | | | | | | | | | |
| $t_{ENLZ}$ | Enable Pad LOW to Z | | | 6.9 | | 7.6 | | 8.7 | | 10.2 | | 14.3 | ns |
| $t_{GLH}$ | G-to-Pad HIGH | | | 4.9 | | 5.5 | | 6.2 | | 7.3 | | 10.2 | ns |
| $t_{GHL}$ | G-to-Pad LOW | | | 4.9 | | 5.5 | | 6.2 | | 7.3 | | 10.2 | ns |
| $t_{LSU}$ | I/O Latch Output Set-Up | | 0.7 | | 0.7 | | 0.8 | | 1.0 | | 1.4 | | ns |
| $t_{LH}$ | I/O Latch Output Hold | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{LCO}$ | I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O | | | 7.9 | | 8.8 | | 10.0 | | 11.8 | | 16.5 | ns |

***Table 54 •*** **PQ240**

| **PQ240** | |
|---|---|
| **Pin Number** | **A42MX36 Function** |
| 15 | QCLKC, I/O |
| 16 | I/O |
| 17 | WD, I/O |
| 18 | WD, I/O |
| 19 | I/O |
| 20 | I/O |
| 21 | WD, I/O |
| 22 | WD, I/O |
| 23 | I/O |
| 24 | PRB, I/O |
| 25 | I/O |
| 26 | CLKB, I/O |
| 27 | I/O |
| 28 | GND |
| 29 | VCCA |
| 30 | VCCI |
| 31 | I/O |
| 32 | CLKA, I/O |
| 33 | I/O |
| 34 | PRA, I/O |
| 35 | I/O |
| 36 | I/O |
| 37 | WD, I/O |
| 38 | WD, I/O |
| 39 | I/O |
| 40 | I/O |
| 41 | I/O |
| 42 | I/O |
| 43 | I/O |
| 44 | I/O |
| 45 | QCLKD, I/O |
| 46 | I/O |
| 47 | WD, I/O |
| 48 | WD, I/O |
| 49 | I/O |
| 50 | I/O |
| 51 | I/O |

***Table 54 •*** **PQ240**

| **PQ240** | |
|---|---|
| **Pin Number** | **A42MX36 Function** |
| 52 | VCCI |
| 53 | I/O |
| 54 | WD, I/O |
| 55 | WD, I/O |
| 56 | I/O |
| 57 | SDI, I/O |
| 58 | I/O |
| 59 | VCCA |
| 60 | GND |
| 61 | GND |
| 62 | I/O |
| 63 | I/O |
| 64 | I/O |
| 65 | I/O |
| 66 | I/O |
| 67 | I/O |
| 68 | I/O |
| 69 | I/O |
| 70 | I/O |
| 71 | VCCI |
| 72 | I/O |
| 73 | I/O |
| 74 | I/O |
| 75 | I/O |
| 76 | I/O |
| 77 | I/O |
| 78 | I/O |
| 79 | I/O |
| 80 | I/O |
| 81 | I/O |
| 82 | I/O |
| 83 | I/O |
| 84 | I/O |
| 85 | VCCA |
| 86 | I/O |
| 87 | I/O |
| 88 | VCCA |

***Table 55 •*** **VQ80**

| **VQ80** | | |
|---|---|---|
| **Pin Number** | **A40MX02 Function** | **A40MX04 Function** |
| 49 | I/O | I/O |
| 50 | CLK, I/O | CLK, I/O |
| 51 | I/O | I/O |
| 52 | MODE | MODE |
| 53 | VCC | VCC |
| 54 | NC | I/O |
| 55 | NC | I/O |
| 56 | NC | I/O |
| 57 | SDI, I/O | SDI, I/O |
| 58 | DCLK, I/O | DCLK, I/O |
| 59 | PRA, I/O | PRA, I/O |
| 60 | NC | NC |
| 61 | PRB, I/O | PRB, I/O |
| 62 | I/O | I/O |
| 63 | I/O | I/O |
| 64 | I/O | I/O |
| 65 | I/O | I/O |
| 66 | I/O | I/O |
| 67 | I/O | I/O |
| 68 | GND | GND |
| 69 | I/O | I/O |
| 70 | I/O | I/O |
| 71 | I/O | I/O |
| 72 | I/O | I/O |
| 73 | I/O | I/O |
| 74 | VCC | **VCC** |
| 75 | I/O | I/O |
| 76 | I/O | I/O |
| 77 | I/O | I/O |
| 78 | I/O | I/O |
| 79 | I/O | I/O |
| 80 | I/O | I/O |

***Figure 47 •*** **VQ100**

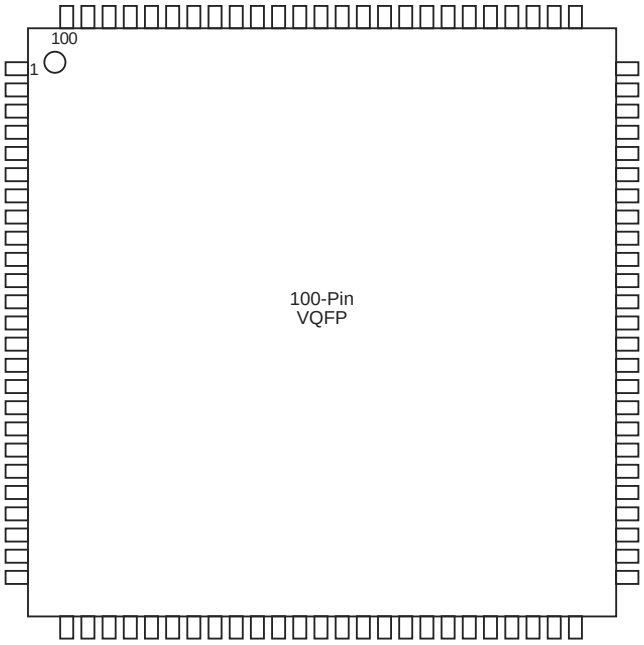



***Table 56 •*** **VQ100**

| **VQ100** | | |
|---|---|---|
| **Pin Number** | **A42MX09 Function** | **A42MX16 Function** |
| 1 | I/O | I/O |
| 2 | MODE | MODE |
| 3 | I/O | I/O |
| 4 | I/O | I/O |
| 5 | I/O | I/O |
| 6 | I/O | I/O |
| 7 | GND | GND |
| 8 | I/O | I/O |
| 9 | I/O | I/O |
| 10 | I/O | I/O |
| 11 | I/O | I/O |
| 12 | I/O | I/O |
| 13 | I/O | I/O |
| 14 | VCCA | NC |
| 15 | VCCI | VCCI |
| 16 | I/O | I/O |
| 17 | I/O | I/O |
| 18 | I/O | I/O |
| 19 | I/O | I/O |
| 20 | GND | GND |

***Table 57 •*** **TQ176**

| **TQ176** | | | |
|---|---|---|---|
| **Pin Number** | **A42MX09 Function** | **A42MX16 Function** | **A42MX24 Function** |
| 121 | NC | NC | I/O |
| 122 | I/O | I/O | I/O |
| 123 | I/O | I/O | I/O |
| 124 | NC | I/O | I/O |
| 125 | NC | I/O | I/O |
| 126 | NC | NC | I/O |
| 127 | I/O | I/O | I/O |
| 128 | I/O | I/O | I/O |
| 129 | I/O | I/O | I/O |
| 130 | I/O | I/O | I/O |
| 131 | I/O | I/O | I/O |
| 132 | I/O | I/O | I/O |
| 133 | GND | GND | GND |
| 134 | I/O | I/O | I/O |
| 135 | SDI, I/O | SDI, I/O | SDI, I/O |
| 136 | NC | I/O | I/O |
| 137 | I/O | I/O | WD, I/O |
| 138 | I/O | I/O | WD, I/O |
| 139 | I/O | I/O | I/O |
| 140 | NC | VCCI | VCCI |
| 141 | I/O | I/O | I/O |
| 142 | I/O | I/O | I/O |
| 143 | NC | I/O | I/O |
| 144 | NC | I/O | WD, I/O |
| 145 | NC | NC | WD, I/O |
| 146 | I/O | I/O | I/O |
| 147 | NC | I/O | I/O |
| 148 | I/O | I/O | I/O |
| 149 | I/O | I/O | I/O |
| 150 | I/O | I/O | WD, I/O |
| 151 | NC | I/O | WD, I/O |
| 152 | PRA, I/O | PRA, I/O | PRA, I/O |
| 153 | I/O | I/O | I/O |
| 154 | CLKA, I/O | CLKA, I/O | CLKA, I/O |
| 155 | VCCA | VCCA | VCCA |
| 156 | GND | GND | GND |
| 157 | I/O | I/O | I/O |

***Table 58 •*** **CQ208**

| **CQ208** | |
|---|---|
| **Pin Number** | **A42MX36 Function** |
| 74 | I/O |
| 75 | I/O |
| 76 | I/O |
| 77 | I/O |
| 78 | GND |
| 79 | VCCA |
| 80 | VCCI |
| 81 | I/O |
| 82 | I/O |
| 83 | I/O |
| 84 | I/O |
| 85 | WD, I/O |
| 86 | WD, I/O |
| 87 | I/O |
| 88 | I/O |
| 89 | I/O |
| 90 | I/O |
| 91 | QCLKB, I/O |
| 92 | I/O |
| 93 | WD, I/O |
| 94 | WD, I/O |
| 95 | I/O |
| 96 | I/O |
| 97 | I/O |
| 98 | VCCI |
| 99 | I/O |
| 100 | WD, I/O |
| 101 | WD, I/O |
| 102 | I/O |
| 103 | TDO, I/O |
| 104 | I/O |
| 105 | GND |
| 106 | VCCA |
| 107 | I/O |
| 108 | I/O |
| 109 | I/O |
| 110 | I/O |

***Figure 50 •*** **CQ256**

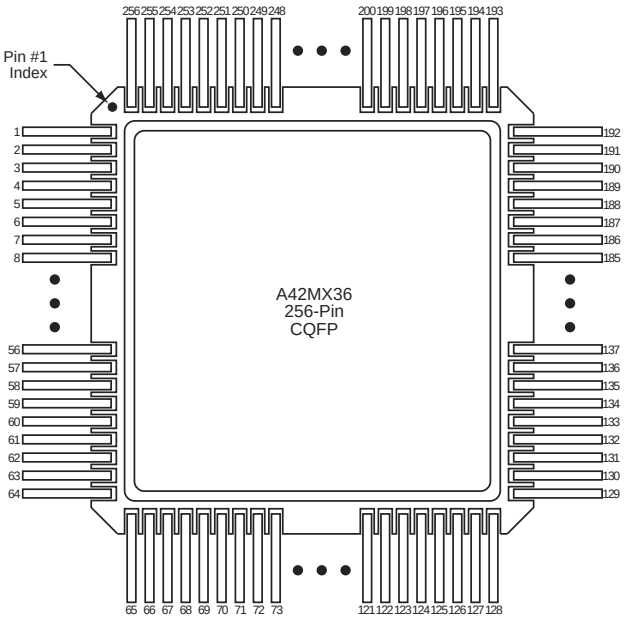



***Table 59 •*** **CQ256**

| **CQ256** | |
|---|---|
| **Pin Number** | **A42MX36 Function** |
| 1 | NC |
| 2 | GND |
| 3 | I/O |
| 4 | I/O |
| 5 | I/O |
| 6 | I/O |
| 7 | I/O |
| 8 | I/O |
| 9 | I/O |
| 10 | GND |
| 11 | I/O |
| 12 | I/O |
| 13 | I/O |
| 14 | I/O |
| 15 | I/O |
| 16 | I/O |
| 17 | I/O |
| 18 | I/O |
| 19 | I/O |
| 20 | I/O |
| 21 | I/O |

***Table 60 •*** **BG272**

| **BG272** | |
|---|---|
| **Pin Number** | **A42MX36 Function** |
| J9 | GND |
| J10 | GND |
| J11 | GND |
| J12 | GND |
| J17 | VCCA |
| J18 | I/O |
| J19 | I/O |
| J20 | I/O |
| K1 | I/O |
| K2 | I/O |
| K3 | I/O |
| K4 | VCCI |
| K9 | GND |
| K10 | GND |
| K11 | GND |
| K12 | GND |
| K17 | I/O |
| K18 | VCCA |
| K19 | VCCA |
| K20 | LP |
| L1 | I/O |
| L2 | I/O |
| L3 | VCCA |
| L4 | VCCA |
| L9 | GND |
| L10 | GND |
| L11 | GND |
| L12 | GND |
| L17 | VCCI |
| L18 | I/O |
| L19 | I/O |
| L20 | TCK, I/O |
| M1 | I/O |
| M2 | I/O |
| M3 | I/O |
| M4 | VCCI |
| M9 | GND |

***Table 61 •*** **PG132**

| **PG132** | |
|---|---|
| **Pin Number** | **A42MX09 Function** |
| F2 | I/O |
| F1 | I/O |
| G1 | I/O |
| G4 | VSV |
| H1 | I/O |
| H2 | I/O |
| H3 | I/O |
| H4 | I/O |
| J1 | I/O |
| K1 | I/O |
| L1 | I/O |
| K2 | I/O |
| M1 | I/O |
| K3 | I/O |
| L2 | I/O |
| N1 | I/O |
| L3 | BININ |
| M2 | BINOUT |
| N2 | I/O |
| M3 | I/O |
| L4 | I/O |
| N3 | I/O |
| M4 | I/O |
| N4 | I/O |
| M5 | I/O |
| K6 | I/O |
| N5 | I/O |
| N6 | I/O |
| L6 | I/O |
| M6 | I/O |
| M7 | I/O |
| N7 | I/O |
| N8 | I/O |
| M8 | I/O |
| L8 | I/O |
| K8 | I/O |
| N9 | I/O |

***Table 61 •*** **PG132**

| **PG132** | |
|---|---|
| **Pin Number** | **A42MX09 Function** |
| B3 | I/O |
| A2 | I/O |
| C3 | DCLK |
| B5 | GNDA |
| E12 | GNDA |
| J2 | GNDA |
| M9 | GNDA |
| B9 | GNDI |
| C5 | GNDI |
| E11 | GNDI |
| F4 | GNDI |
| J3 | GNDI |
| J11 | GNDI |
| L5 | GNDI |
| L9 | GNDI |
| C9 | GNDQ |
| E3 | GNDQ |
| K12 | GNDQ |
| D7 | VCCA |
| G3 | VCCA |
| G10 | VCCA |
| L7 | VCCA |
| C7 | VCCI |
| G2 | VCCI |
| G11 | VCCI |
| K7 | VCCI |