**Welcome to E-XFL.COM**

## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | - |
| Number of I/O | 57 |
| Number of Gates | 3000 |
| Voltage - Supply | 3V ~ 3.6V, 4.75V ~ 5.25V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Package / Case | 80-TQFP |
| Supplier Device Package | 80-VQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/a40mx02-3vqg80 |

**Microsemi Corporate Headquarters**
One Enterprise, Aliso Viejo,
CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Fax: +1 (949) 215-4996
Email: sales.support@microsemi.com
www.microsemi.com





## About Microsemi

Microsemi Corporation (Nasdaq: MSCC) offers a comprehensive portfolio of semiconductor and system solutions for aerospace & defense, communications, data center and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; enterprise storage and communication solutions, security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, California, and has approximately 4,800 employees globally. Learn more at www.microsemi.com.

5172136. 15.0 12/16

- The Transient Current, page 13 is new (SAR 36930).
- Package names were revised according to standards established in *Package Mechanical Drawings* (SAR 34774)

## 1.7 Revision 9.0

The following is a summary of the changes in revision 9.0 of this document

- In Table 20, page 23, the limits in VI were changed from -0.5 to VCCI + 0.5 to -0.5 to VCCA + 0.5

In Table 22, page 25, $V_{OH}$ was changed from 3.7 to 2.4 for the min in industrial and military. $V_{IH}$ had $V_{CCI}$ and that was changed to VCCA

## 1.8 Revision 6.0

The following is a summary of the changes in revision 6.0 of this document.

- The Ease of Integration, page 1 was updated
- The Temperature Grade Offerings, page 5 is new
- The Speed Grade Offerings, page 5 is new
- The General Description, page 6 was updated
- The MultiPlex I/O Modules, page 11 was updated
- The User Security, page 12 was updated
- Table 6, page 13 was updated
- The Power Dissipation, page 14 was updated.
- The Static Power Component, page 14 was updated
- The Equivalent Capacitance, page 15 was updated
- Figure 13, page 17 was updated
- Table 10, page 18 was updated.
- Figure 14, page 18 was updated.
- Table 11, page 19 was updated.

# 2 40MX and 42MX FPGA Families

## 2.1 Features

The following sections list out various features of the 40MX and 42MX FPGA family devices.

### 2.1.1 High Capacity

- Single-Chip ASIC Alternative
- 3,000 to 54,000 System Gates
- Up to 2.5 kbits Configurable Dual-Port SRAM
- Fast Wide-Decode Circuitry
- Up to 202 User-Programmable I/O Pins

### 2.1.2 High Performance

- 5.6 ns Clock-to-Out
- 250 MHz Performance
- 5 ns Dual-Port SRAM Access
- 100 MHz FIFOs
- 7.5 ns 35-Bit Address Decode

### 2.1.3 HiRel Features

- Commercial, Industrial, Automotive, and Military Temperature Plastic Packages
- Commercial, Military Temperature, and MIL-STD-883 Ceramic Packages
- QML Certification
- Ceramic Devices Available to DSCC SMD

### 2.1.4 Ease of Integration

- Mixed-Voltage Operation (5.0 V or 3.3 V for core and I/Os), with PCI-Compliant I/Os
- Up to 100% Resource Utilization and 100% Pin Locking
- Deterministic, User-Controllable Timing
- Unique In-System Diagnostic and Verification Capability with Silicon Explorer II
- Low Power Consumption
- IEEE Standard 1149.1 (JTAG) Boundary Scan Testing

## 2.2 Product Profile

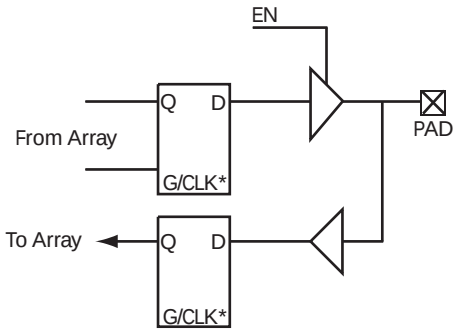
The following table gives the features of the products.

***Table 1 •*** **Product profile**

| Device | A40MX02 | A40MX04 | A42MX09 | A42MX16 | A42MX24 | A42MX36 |
|---|---|---|---|---|---|---|
| **Capacity** | | | | | | |
| System Gates | 3,000 | 6,000 | 14,000 | 24,000 | 36,000 | 54,000 |
| SRAM Bits | – | – | – | – | – | 2,560 |
| **Logic Modules** | | | | | | |
| Sequential | – | – | 348 | 624 | 954 | 1,230 |
| Combinatorial | 295 | 547 | 336 | 608 | 912 | 1,184 |
| Decode | – | – | – | – | 24 | 24 |
| **Clock-to-Out** | 9.5 ns | 9.5 ns | 5.6 ns | 6.1 ns | 6.1 ns | 6.3 ns |
| **SRAM Modules (64x4 or 32x8)** | – | – | – | – | – | 10 |
| **Dedicated Flip-Flops** | – | – | 348 | 624 | 954 | 1,230 |

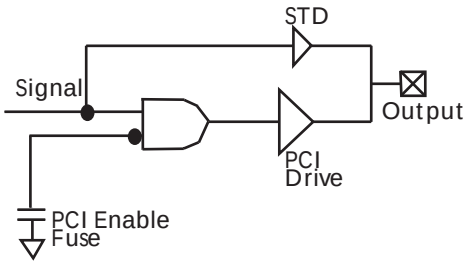
Designer software development tools provide a design library of I/O macro functions that can implement all I/O configurations supported by the MX FPGAs.

***Figure 10 •*** **42MX I/O Module**




***Note:*** **Can be configured as a Latch or D Flip-Flop (Using C-Module)*

***Figure 11 •*** **PCI Output Structure of A42MX24 and A42MX36 Devices**




# 3.3 Other Architectural Features

The following sections cover other architectural features of 40MX and 42MX FPGAs.

## 3.3.1 Performance

MX devices can operate with internal clock frequencies of 250 MHz, enabling fast execution of complex logic functions. MX devices are live on power-up and do not require auxiliary configuration devices and thus are an optimal platform to integrate the functionality contained in multiple programmable logic devices. In addition, designs that previously would have required a gate array to meet performance can be integrated into an MX device with improvements in cost and time-to-market. Using timing-driven place-and-route (TDPR) tools, designers can achieve highly deterministic device performance.

## 3.3.2 User Security

Microsemi FuseLock provides robust security against design theft. Special security fuses are hidden in the fabric of the device and protect against unauthorized users attempting to access the programming and/or probe interfaces. It is virtually impossible to identify or bypass these fuses without damaging the device, making Microsemi antifuse FPGAs protected with the highest level of security available from both invasive and noninvasive attacks.

Special security fuses in 40MX devices include the Probe Fuse and Program Fuse. The former disables the probing circuitry while the latter prohibits further programming of all fuses, including the Probe Fuse. In 42MX devices, there is the Security Fuse which, when programmed, both disables the probing circuitry and prohibits further programming of the device.

## 3.3.3 Programming

Device programming is supported through the Silicon Sculptor series of programmers. Silicon Sculptor is a compact, robust, single-site and multi-site device programmer for the PC. With standalone software, Silicon Sculptor is designed to allow concurrent programming of multiple units from the same PC.

Silicon Sculptor programs devices independently to achieve the fastest programming times possible. After being programmed, each fuse is verified to insure that it has been programmed correctly. Furthermore, at the end of programming, there are integrity tests that are run to ensure no extra fuses have been programmed. Not only does it test fuses (both programmed and non-programmed), Silicon Sculptor also allows self-test to verify its own hardware extensively.

The procedure for programming an MX device using Silicon Sculptor is as follows:

1. Load the *.AFM file
2. Select the device to be programmed
3. Begin programming

When the design is ready to go to production, Microsemi offers device volume-programming services either through distribution partners or via In-House Programming from the factory.

For more details on programming MX devices, see the *AC225: Programming Antifuse Devices* application note and the *Silicon Sculptor 3 Programmers User Guide*.

## 3.3.4 Power Supply

MX devices are designed to operate in both 5.0V and 3.3V environments. In particular, 42MX devices can operate in mixed 5.0 V/3.3 V systems. The following table describes the voltage support of MX devices.

***Table 6 •*** **Voltage Support of MX Devices**

| Device | VCC | VCCA | VCCI | Maximum Input Tolerance | Nominal Output Voltage |
|---|---|---|---|---|---|
| 40MX | 5.0 V | – | – | 5.5 V | 5.0 V |
| | 3.3 V | – | – | 3.6 V | 3.3 V |
| 42MX | – | 5.0 V | 5.0 V | 5.5 V | 5.0 V |
| | – | 3.3 V | 3.3 V | 3.6 V | 3.3 V |
| | – | 5.0 V | 3.3 V | 5.5 V | 3.3 V |

For A42MX24 and A42MX36 devices the VCCA supply has to be monotonic during power up in order for the POR to issue reset to the JTAG state machine correctly. For more information, see the *AC291: 42MX Family Devices Power-Up Behavior*.

## 3.3.5 Power-Up/Down in Mixed-Voltage Mode

When powering up 42MX in mixed voltage mode (VCCA = 5.0 V and VCCI = 3.3 V), VCCA must be greater than or equal to VCCI throughout the power-up sequence. If VCCI exceeds VCCA during power-up, one of two things will happen:

- The input protection diode on the I/Os will be forward biased
- The I/Os will be at logical High

In either case, ICC rises to high levels. For power-down, any sequence with VCCA and VCCI can be implemented.

## 3.3.6 Transient Current

Due to the simultaneous random logic switching activity during power-up, a transient current may appear on the core supply (VCC). Customers must use a regulator for the VCC supply that can source a minimum of 100 mA for transient current during power-up. Failure to provide enough power can prevent the system from powering up properly and result in functional failure. However, there are no reliability concerns, since transient current is distributed across the die instead of confined to a localized spot.

Since the transient current is not due to I/O switching, its value and duration are independent of the VCCI.

## 3.9.3 Output Drive Characteristics for 3.3 V PCI Signaling

***Table 25 •*** **DC Specification (3.3 V PCI Signaling)[1]**

| | | | PCI | | MX | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Condition** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| VCCI | Supply Voltage for I/Os | | 3.0 | 3.6 | 3.0 | 3.6[2] | V |
| VIH | Input High Voltage | | 0.5 | VCC + 0.5 | 0.5 | VCCI + 0.3 | V |
| VIL | Input Low Voltage | | –0.5 | 0.8 | –0.3 | 0.8 | V |
| IIH | Input High Leakage Current | VIN = 2.7 V | | 70 | | 10 | µA |
| IIL | Input Leakage Current | | | –70 | | –10 | µA |
| VOH | Output High Voltage | IOUT = –2 mA | 0.9 | | 3.3 | | V |
| VOL | Output Low Voltage | IOUT = 3 mA, 6 mA | | 0.1 | | 0.1 VCCI | V |
| $C_{IN}$ | Input Pin Capacitance | | | 10 | | 10 | pF |
| $C_{CLK}$ | CLK Pin Capacitance | | 5 | 12 | | 10 | pF |
| $L_{PIN}$ | Pin Inductance | | | 20 | | < 8 nH[3] | nH |

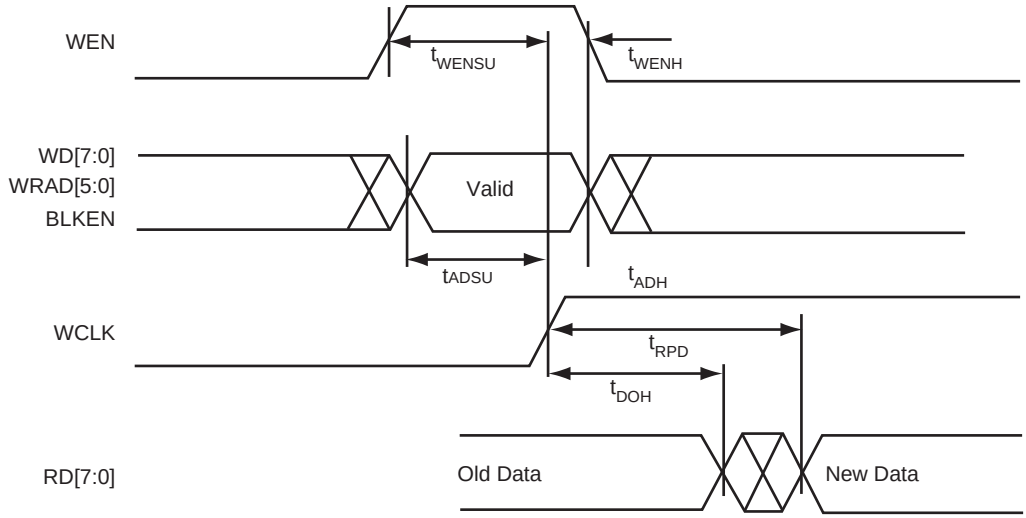
1. PCI Local Bus Specification, Version 2.1, Section 4.2.2.1.
2. Maximum rating for VCCI –0.5 V to 7.0V.
3. Dependent upon the chosen package. PCI recommends QFP and BGA packaging to reduce pin inductance and capacitance.

***Table 26 •*** **AC Specifications for (3.3 V PCI Signaling)***

| | | | PCI | | MX | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Condition** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| ICL | Low Clamp Current | –5 < VIN ≤ –1 | –25 + (VIN +1) /0.015 | | –60 | –10 | mA |
| Slew (r) | Output Rise Slew Rate | 0.2 V to 0.6 V load | 1 | 4 | 1.8 | 2.8 | V/ns |
| Slew (f) | Output Fall Slew Rate | 0.6 V to 0.2 V load | 1 | 4 | 2.8 | 4.0 | V/ns |

**Note:** *PCI Local Bus Specification, Version 2.1, Section 4.2.2.2.

***Figure 33 •*** **42MX SRAM Asynchronous Read Operation—Type 2 (Write Address Controlled)**




## 3.10.7 Predictable Performance: Tight Delay Distributions

Propagation delay between logic modules depends on the resistive and capacitive loading of the routing tracks, the interconnect elements, and the module inputs being driven. Propagation delay increases as the length of routing tracks, the number of interconnect elements, or the number of inputs increases.

From a design perspective, the propagation delay can be statistically correlated or modeled by the fanout (number of loads) driven by a module. Higher fanout usually requires some paths to have longer routing tracks.

The MX FPGAs deliver a tight fanout delay distribution, which is achieved in two ways: by decreasing the delay of the interconnect elements and by decreasing the number of interconnect elements per path.

Microsemi's patented antifuse offers a very low resistive/capacitive interconnect. The antifuses, fabricated in 0.45 µm lithography, offer nominal levels of 100 Ω resistance and 7.0 fF capacitance per antifuse.

MX fanout distribution is also tight due to the low number of antifuses required for each interconnect path. The proprietary architecture limits the number of antifuses per path to a maximum of four, with 90 percent of interconnects using only two antifuses.

# 3.11 Timing Characteristics

Device timing characteristics fall into three categories: family-dependent, device-dependent, and design-dependent. The input and output buffer characteristics are common to all MX devices. Internal routing delays are device-dependent; actual delays are not determined until after place-and-route of the user's design is complete. Delay values may then be determined by using the Designer software utility or by performing simulation with post-layout delays.

## 3.11.1 Critical Nets and Typical Nets

Propagation delays are expressed only for typical nets, which are used for initial design performance evaluation. Critical net delays can then be applied to the most timing critical paths. Critical nets are determined by net property assignment in Microsemi's Designer software prior to placement and routing. Up to 6% of the nets in a design may be designated as critical.

## 3.11.2 Long Tracks

Some nets in the design use long tracks, which are special routing resources that span multiple rows, columns, or modules. Long tracks employ three and sometimes four antifuse connections, which increase capacitance and resistance, resulting in longer net delays for macros connected to long tracks. Typically, up to 6 percent of nets in a fully utilized device require long tracks. Long tracks add

***Table 34 •*** **A40MX02 Timing Characteristics (Nominal 5.0 V Operation) *(continued)***
**(Worst-Case Commercial Conditions, VCC = 4.75 V, $T_J$ = 70°C)**

| Parameter / Description | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **TTL Output Module Timing[4]** | | | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad HIGH | | 3.3 | | 3.8 | | 4.3 | | 5.1 | | 7.2 | ns |
| $t_{DHL}$ | Data-to-Pad LOW | | 4.0 | | 4.6 | | 5.2 | | 6.1 | | 8.6 | ns |
| $t_{ENZH}$ | Enable Pad Z to HIGH | | 3.7 | | 4.3 | | 4.9 | | 5.8 | | 8.0 | ns |
| $t_{ENZL}$ | Enable Pad Z to LOW | | 4.7 | | 5.4 | | 6.1 | | 7.2 | | 10.1 | ns |
| $t_{ENHZ}$ | Enable Pad HIGH to Z | | 7.9 | | 9.1 | | 10.4 | | 12.2 | | 17.1 | ns |
| $t_{ENLZ}$ | Enable Pad LOW to Z | | 5.9 | | 6.8 | | 7.7 | | 9.0 | | 12.6 | ns |
| $d_{TLH}$ | Delta LOW to HIGH | | 0.02 | | 0.02 | | 0.03 | | 0.03 | | 0.04 | ns/pF |
| $d_{THL}$ | Delta HIGH to LOW | | 0.03 | | 0.03 | | 0.03 | | 0.04 | | 0.06 | ns/pF |
| **CMOS Output Module Timing[4]** | | | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad HIGH | | 3.9 | | 4.5 | | 5.1 | | 6.05 | | 8.5 | ns |
| $t_{DHL}$ | Data-to-Pad LOW | | 3.4 | | 3.9 | | 4.4 | | 5.2 | | 7.3 | ns |
| $t_{ENZH}$ | Enable Pad Z to HIGH | | 3.4 | | 3.9 | | 4.4 | | 5.2 | | 7.3 | ns |
| $t_{ENZL}$ | Enable Pad Z to LOW | | 4.9 | | 5.6 | | 6.4 | | 7.5 | | 10.5 | ns |
| $t_{ENHZ}$ | Enable Pad HIGH to Z | | 7.9 | | 9.1 | | 10.4 | | 12.2 | | 17.0 | ns |
| $t_{ENLZ}$ | Enable Pad LOW to Z | | 5.9 | | 6.8 | | 7.7 | | 9.0 | | 12.6 | ns |
| $d_{TLH}$ | Delta LOW to HIGH | | 0.03 | | 0.04 | | 0.04 | | 0.05 | | 0.07 | ns/pF |
| $d_{THL}$ | Delta HIGH to LOW | | 0.02 | | 0.02 | | 0.03 | | 0.03 | | 0.04 | ns/pF |

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance
2. Set-up times assume fanout of 3. Further testing information can be obtained from the Timer utility
3. The hold time for the DFME1A macro may be greater than 0 ns. Use the Timer tool from the Designer software to check the hold time for this macro.
4. Delays based on 35pF loading

***Table 35 •*** **A40MX02 Timing Characteristics (Nominal 3.3 V Operation)**
**(Worst-Case Commercial Conditions, VCC = 3.0 V, $T_J$ = 70°C)**

| Parameter / Description | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Logic Module Propagation Delays** | | | | | | | | | | | | |
| $t_{PD1}$ | Single Module | | 1.7 | | 2.0 | | 2.3 | | 2.7 | | 3.7 | ns |
| $t_{PD2}$ | Dual-Module Macros | | 3.7 | | 4.3 | | 4.9 | | 5.7 | | 8.0 | ns |
| $t_{CO}$ | Sequential Clock-to-Q | | 1.7 | | 2.0 | | 2.3 | | 2.7 | | 3.7 | ns |
| $t_{GO}$ | Latch G-to-Q | | 1.7 | | 2.0 | | 2.3 | | 2.7 | | 3.7 | ns |
| $t_{RS}$ | Flip-Flop (Latch) Reset-to-Q | | 1.7 | | 2.0 | | 2.3 | | 2.7 | | 3.7 | ns |
| **Logic Module Predicted Routing Delays[1]** | | | | | | | | | | | | |

***Table 35 •*** **A40MX02 Timing Characteristics (Nominal 3.3 V Operation) *(continued)***
**(Worst-Case Commercial Conditions, VCC = 3.0 V, $T_J$ = 70°C)**

| Parameter / Description | | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{RD1}$ | FO = 1 Routing Delay | | | 2.0 | | 2.2 | | 2.5 | | 3.0 | | 4.2 | ns |
| $t_{RD2}$ | FO = 2 Routing Delay | | | 2.7 | | 3.1 | | 3.5 | | 4.1 | | 5.7 | ns |
| $t_{RD3}$ | FO = 3 Routing Delay | | | 3.4 | | 3.9 | | 4.4 | | 5.2 | | 7.3 | ns |
| $t_{RD4}$ | FO = 4 Routing Delay | | | 4.2 | | 4.8 | | 5.4 | | 6.3 | | 8.9 | ns |
| $t_{RD8}$ | FO = 8 Routing Delay | | | 7.1 | | 8.2 | | 9.2 | | 10.9 | | 15.2 | ns |
| **Logic Module Sequential Timing[2]** | | | | | | | | | | | | | |
| $t_{SUD}$ | Flip-Flop (Latch) Data Input Set-Up | | 4.3 | | 4.9 | | 5.6 | | 6.6 | | 9.2 | | ns |
| $t_{HD}$[3] | Flip-Flop (Latch) Data Input Hold | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{SUENA}$ | Flip-Flop (Latch) Enable Set-Up | | 4.3 | | 4.9 | | 5.6 | | 6.6 | | 9.2 | | ns |
| $t_{HENA}$ | Flip-Flop (Latch) Enable Hold | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{WCLKA}$ | Flip-Flop (Latch) Clock Active Pulse Width | | 4.6 | | 5.3 | | 6.0 | | 7.0 | | 9.8 | | ns |
| $t_{WASYN}$ | Flip-Flop (Latch) Asynchronous Pulse Width | | 4.6 | | 5.3 | | 6.0 | | 7.0 | | 9.8 | | ns |
| $t_A$ | Flip-Flop Clock Input Period | | 6.8 | | 7.8 | | 8.9 | | 10.4 | | 14.6 | | ns |
| $f_{MAX}$ | Flip-Flop (Latch) Clock Frequency (FO = 128) | | | 109 | | 101 | | 92 | | 80 | | 48 | MHz |
| **Input Module Propagation Delays** | | | | | | | | | | | | | |
| $t_{INYH}$ | Pad-to-Y HIGH | | | 1.0 | | 1.1 | | 1.3 | | 1.5 | | 2.1 | ns |
| $t_{INYL}$ | Pad-to-Y LOW | | | 0.9 | | 1.0 | | 1.1 | | 1.3 | | 1.9 | ns |
| **Input Module Predicted Routing Delays[1]** | | | | | | | | | | | | | |
| $t_{IRD1}$ | FO = 1 Routing Delay | | | 2.9 | | 3.4 | | 3.8 | | 4.5 | | 6.3 | ns |
| $t_{IRD2}$ | FO = 2 Routing Delay | | | 3.6 | | 4.2 | | 4.8 | | 5.6 | | 7.8 | ns |
| $t_{IRD3}$ | FO = 3 Routing Delay | | | 4.4 | | 5.0 | | 5.7 | | 6.7 | | 9.4 | ns |
| $t_{IRD4}$ | FO = 4 Routing Delay | | | 5.1 | | 5.9 | | 6.7 | | 7.8 | | 11.0 | ns |
| $t_{IRD8}$ | FO = 8 Routing Delay | | | 8.0 | | 9.26 | | 10.5 | | 12.6 | | 17.3 | ns |
| **Global Clock Network** | | | | | | | | | | | | | |
| $t_{CKH}$ | Input LOW to HIGH | FO = 16<br>FO = 128 | | 6.4<br>6.4 | | 7.4<br>7.4 | | 8.3<br>8.3 | | 9.8<br>9.8 | | 13.7<br>13.7 | ns |
| $t_{CKL}$ | Input HIGH to LOW | FO = 16<br>FO = 128 | | 6.7<br>6.7 | | 7.8<br>7.8 | | 8.8<br>8.8 | | 10.4<br>10.4 | | 14.5<br>14.5 | ns |
| $t_{PWH}$ | Minimum Pulse Width HIGH | FO = 16<br>FO = 128 | 3.1<br>3.3 | | 3.6<br>3.8 | | 4.1<br>4.3 | | 4.8<br>5.1 | | 6.7<br>7.1 | | ns |
| $t_{PWL}$ | Minimum Pulse Width LOW | FO = 16<br>FO = 128 | 3.1<br>3.3 | | 3.6<br>3.8 | | 4.1<br>4.3 | | 4.8<br>5.1 | | 6.7<br>7.1 | | ns |
| $t_{CKSW}$ | Maximum Skew | FO = 16<br>FO = 128 | | 0.6<br>0.8 | | 0.6<br>0.9 | | 0.7<br>1.0 | | 0.8<br>1.2 | | 1.2<br>1.6 | ns |

**Table 38 • A42MX09 Timing Characteristics (Nominal 5.0 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 4.75 V, $T_J$ = 70°C)**

| Parameter / Description | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{WASYN}$ | Flip-Flop (Latch) Asynchronous Pulse Width | 4.5 | | 4.9 | | 5.6 | | 6.6 | | 9.2 | | ns |
| $t_A$ | Flip-Flop Clock Input Period | 3.5 | | 3.8 | | 4.3 | | 5.1 | | 7.1 | | ns |
| $t_{INH}$ | Input Buffer Latch Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{INSU}$ | Input Buffer Latch Set-Up | 0.3 | | 0.3 | | 0.4 | | 0.4 | | 0.6 | | ns |
| $t_{OUTH}$ | Output Buffer Latch Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{OUTSU}$ | Output Buffer Latch Set-Up | 0.3 | | 0.3 | | 0.4 | | 0.4 | | 0.6 | | ns |
| $f_{MAX}$ | Flip-Flop (Latch) Clock Frequency | | 268 | | 244 | | 224 | | 195 | | 117 | MHz |

***Table 40 •*** **A42MX16 Timing Characteristics (Nominal 5.0 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 4.75 V, $T_J$ = 70°C)**

| Parameter / Description | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **CMOS Output Module Timing[5]** | | | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad HIGH | | 3.2 | | 3.6 | | 4.0 | | 4.7 | | 6.6 | ns |
| $t_{DHL}$ | Data-to-Pad LOW | | 2.5 | | 2.7 | | 3.1 | | 3.6 | | 5.1 | ns |
| $t_{ENZH}$ | Enable Pad Z to HIGH | | 2.7 | | 3.0 | | 3.4 | | 4.0 | | 5.6 | ns |
| $t_{ENZL}$ | Enable Pad Z to LOW | | 3.0 | | 3.3 | | 3.8 | | 4.4 | | 6.2 | ns |
| $t_{ENHZ}$ | Enable Pad HIGH to Z | | 5.4 | | 6.0 | | 6.8 | | 8.0 | | 11.2 | ns |
| $t_{ENLZ}$ | Enable Pad LOW to Z | | 5.0 | | 5.6 | | 6.3 | | 7.4 | | 10.4 | ns |
| $t_{GLH}$ | G-to-Pad HIGH | | 5.1 | | 5.6 | | 6.4 | | 7.5 | | 10.5 | ns |
| $t_{GHL}$ | G-to-Pad LOW | | 5.1 | | 5.6 | | 6.4 | | 7.5 | | 10.5 | ns |
| $t_{LCO}$ | I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading | | 5.7 | | 6.3 | | 7.1 | | 8.4 | | 11.9 | ns |
| $t_{ACO}$ | Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading | | 8.0 | | 8.9 | | 10.1 | | 11.9 | | 16.7 | ns |
| $d_{TLH}$ | Capacitive Loading, LOW to HIGH | | 0.03 | | 0.03 | | 0.03 | | 0.04 | | 0.06 | ns/pF |

1. For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, point and position whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.*
4. Set-up and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.
5. Delays based on 35 pF loading

***Table 41 •*** **A42MX16 Timing Characteristics (Nominal 3.3 V Operation) (Worst-Case Commercial Conditions, VCCA = 3.0 V, $T_J$ = 70°C)**

| Parameter / Description | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Logic Module Propagation Delays[1]** | | | | | | | | | | | | |
| $t_{PD1}$ | Single Module | | 1.9 | | 2.1 | | 2.4 | | 2.8 | | 4.0 | ns |
| $t_{CO}$ | Sequential Clock-to-Q | | 2.0 | | 2.2 | | 2.5 | | 3.0 | | 4.2 | ns |
| $t_{GO}$ | Latch G-to-Q | | 1.9 | | 2.1 | | 2.4 | | 2.8 | | 4.0 | ns |
| $t_{RS}$ | Flip-Flop (Latch) Reset-to-Q | | 2.2 | | 2.4 | | 2.8 | | 3.3 | | 4.6 | ns |
| **Logic Module Predicted Routing Delays[2]** | | | | | | | | | | | | |
| $t_{RD1}$ | FO = 1 Routing Delay | | 1.1 | | 1.2 | | 1.4 | | 1.6 | | 2.3 | ns |
| $t_{RD2}$ | FO = 2 Routing Delay | | 1.5 | | 1.6 | | 1.8 | | 2.1 | | 3.0 | ns |
| $t_{RD3}$ | FO = 3 Routing Delay | | 1.8 | | 2.0 | | 2.3 | | 2.7 | | 3.8 | ns |
| $t_{RD4}$ | FO = 4 Routing Delay | | 2.2 | | 2.4 | | 2.7 | | 3.2 | | 4.5 | ns |
| $t_{RD8}$ | FO = 8 Routing Delay | | 3.6 | | 4.0 | | 4.5 | | 5.3 | | 7.5 | ns |

***Table 43 •*** **A42MX24 Timing Characteristics (Nominal 3.3 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 3.0 V, $T_J$ = 70°C)**

| Parameter / Description | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Logic Module Sequential Timing[3, 4]** | | | | | | | | | | | | |
| $t_{CO}$ | Flip-Flop Clock-to-Output | | 2.1 | | 2.0 | | 2.3 | | 2.7 | | 3.7 | ns |
| $t_{GO}$ | Latch Gate-to-Output | | 3.4 | | 1.9 | | 2.1 | | 2.5 | | 3.4 | ns |
| $t_{SUD}$ | Flip-Flop (Latch) Set-Up Time | 0.4 | | 0.5 | | 0.6 | | 0.7 | | 0.9 | | ns |
| $t_{HD}$ | Flip-Flop (Latch) Hold Time | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{RO}$ | Flip-Flop (Latch) Reset-to-Output | | 2.0 | | 2.2 | | 2.5 | | 2.9 | | 4.1 | ns |
| $t_{SUENA}$ | Flip-Flop (Latch) Enable Set-Up | 0.6 | | 0.6 | | 0.7 | | 0.8 | | 1.2 | | ns |
| $t_{HENA}$ | Flip-Flop (Latch) Enable Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{WCLKA}$ | Flip-Flop (Latch) Clock Active Pulse Width | 4.6 | | 5.2 | | 5.8 | | 6.9 | | 9.6 | | ns |
| $t_{WASYN}$ | Flip-Flop (Latch) Asynchronous Pulse Width | 6.1 | | 6.8 | | 7.7 | | 9.0 | | 12.6 | | ns |
| **Input Module Propagation Delays** | | | | | | | | | | | | |
| $t_{INPY}$ | Input Data Pad-to-Y | | 1.4 | | 1.6 | | 1.8 | | 2.2 | | 3.0 | ns |
| $t_{INGO}$ | Input Latch Gate-to-Output | | 1.8 | | 1.9 | | 2.2 | | 2.6 | | 3.6 | ns |
| $t_{INH}$ | Input Latch Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{INSU}$ | Input Latch Set-Up | 0.7 | | 0.7 | | 0.8 | | 1.0 | | 1.4 | | ns |
| $t_{ILA}$ | Latch Active Pulse Width | 6.5 | | 7.3 | | 8.2 | | 9.7 | | 13.5 | | ns |

***Table 44 •*** **A42MX36 Timing Characteristics (Nominal 5.0 V Operation)(Worst-Case Commercial Conditions, VCCA = 4.75 V, $T_J$ = 70°C)**

| Parameter / Description | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Logic Module Combinatorial Functions[1]** | | | | | | | | | | | | |
| $t_{PD}$ | Internal Array Module Delay | | 1.3 | | 1.5 | | 1.7 | | 2.0 | | 2.7 | ns |
| $t_{PDD}$ | Internal Decode Module Delay | | 1.6 | | 1.8 | | 2.0 | | 2.4 | | 3.3 | ns |
| **Logic Module Predicted Routing Delays[2]** | | | | | | | | | | | | |
| $t_{RD1}$ | FO = 1 Routing Delay | | 0.9 | | 1.0 | | 1.2 | | 1.4 | | 2.0 | ns |
| $t_{RD2}$ | FO = 2 Routing Delay | | 1.3 | | 1.4 | | 1.6 | | 1.9 | | 2.7 | ns |
| $t_{RD3}$ | FO =3 Routing Delay | | 1.6 | | 1.8 | | 2.0 | | 2.4 | | 3.4 | ns |
| $t_{RD4}$ | FO = 4 Routing Delay | | 2.0 | | 2.2 | | 2.5 | | 2.9 | | 4.1 | ns |
| $t_{RD5}$ | FO = 8 Routing Delay | | 3.3 | | 3.7 | | 4.2 | | 4.9 | | 6.9 | ns |
| $t_{RDD}$ | Decode-to-Output Routing Delay | | 0.3 | | 0.4 | | 0.4 | | 0.5 | | 0.7 | ns |
| **Logic Module Sequential Timing[3, 4]** | | | | | | | | | | | | |
| $t_{CO}$ | Flip-Flop Clock-to-Output | | 1.3 | | 1.4 | | 1.6 | | 1.9 | | 2.7 | ns |
| $t_{GO}$ | Latch Gate-to-Output | | 1.3 | | 1.4 | | 1.6 | | 1.9 | | 2.7 | ns |
| $t_{SUD}$ | Flip-Flop (Latch) Set-Up Time | 0.3 | | 0.3 | | 0.4 | | 0.5 | | 0.7 | | ns |
| $t_{HD}$ | Flip-Flop (Latch) Hold Time | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{RO}$ | Flip-Flop (Latch) Reset-to-Output | | 1.6 | | 1.7 | | 2.0 | | 2.3 | | 3.2 | ns |
| $t_{SUENA}$ | Flip-Flop (Latch) Enable Set-Up | 0.7 | | 0.8 | | 0.9 | | 1.0 | | 1.4 | | ns |
| $t_{HENA}$ | Flip-Flop (Latch) Enable Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{WCLKA}$ | Flip-Flop (Latch) Clock Active Pulse Width | 3.3 | | 3.7 | | 4.2 | | 4.9 | | 6.9 | | ns |
| $t_{WASYN}$ | Flip-Flop (Latch) Asynchronous Pulse Width | 4.4 | | 4.8 | | 5.5 | | 6.4 | | 9.0 | | ns |
| **Synchronous SRAM Operations** | | | | | | | | | | | | |
| $t_{RC}$ | Read Cycle Time | 6.8 | | 7.5 | | 8.5 | | 10.0 | | 14.0 | | ns |
| $t_{WC}$ | Write Cycle Time | 6.8 | | 7.5 | | 8.5 | | 10.0 | | 14.0 | | ns |
| $t_{RCKHL}$ | Clock HIGH/LOW Time | 3.4 | | 3.8 | | 4.3 | | 5.0 | | 7.0 | | ns |
| $t_{RCO}$ | Data Valid After Clock HIGH/LOW | | 3.4 | | 3.8 | | 4.3 | | 5.0 | | 7.0 | ns |
| $t_{ADSU}$ | Address/Data Set-Up Time | 1.6 | | 1.8 | | 2.0 | | 2.4 | | 3.4 | | ns |
| **Synchronous SRAM Operations (continued)** | | | | | | | | | | | | |
| $t_{ADH}$ | Address/Data Hold Time | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{RENSU}$ | Read Enable Set-Up | 0.6 | | 0.7 | | 0.8 | | 0.9 | | 1.3 | | ns |
| $t_{RENH}$ | Read Enable Hold | 3.4 | | 3.8 | | 4.3 | | 5.0 | | 7.0 | | ns |
| $t_{WENSU}$ | Write Enable Set-Up | 2.7 | | 3.0 | | 3.4 | | 4.0 | | 5.6 | | ns |
| $t_{WENH}$ | Write Enable Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{BENS}$ | Block Enable Set-Up | 2.8 | | 3.1 | | 3.5 | | 4.1 | | 5.7 | | ns |
| $t_{BENH}$ | Block Enable Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |

***Table 49 •*** **PL84**

| **PL84** | | | | |
|---|---|---|---|---|
| **Pin Number** | **A40MX04 Function** | **A42MX09 Function** | **A42MX16 Function** | **A42MX24 Function** |
| 10 | I/O | DCLK, I/O | DCLK, I/O | DCLK, I/O |
| 11 | I/O | I/O | I/O | I/O |
| 12 | NC | MODE | MODE | MODE |
| 13 | I/O | I/O | I/O | I/O |
| 14 | I/O | I/O | I/O | I/O |
| 15 | I/O | I/O | I/O | I/O |
| 16 | I/O | I/O | I/O | I/O |
| 17 | I/O | I/O | I/O | I/O |
| 18 | GND | I/O | I/O | I/O |
| 19 | GND | I/O | I/O | I/O |
| 20 | I/O | I/O | I/O | I/O |
| 21 | I/O | I/O | I/O | I/O |
| 22 | I/O | VCCA | VCCI | VCCI |
| 23 | I/O | VCCI | VCCA | VCCA |
| 24 | I/O | I/O | I/O | I/O |
| 25 | VCC | I/O | I/O | I/O |
| 26 | VCC | I/O | I/O | I/O |
| 27 | I/O | I/O | I/O | I/O |
| 28 | I/O | GND | GND | GND |
| 29 | I/O | I/O | I/O | I/O |
| 30 | I/O | I/O | I/O | I/O |
| 31 | I/O | I/O | I/O | I/O |
| 32 | I/O | I/O | I/O | I/O |
| 33 | VCC | I/O | I/O | I/O |
| 34 | I/O | I/O | I/O | TMS, I/O |
| 35 | I/O | I/O | I/O | TDI, I/O |
| 36 | I/O | I/O | I/O | WD, I/O |
| 37 | I/O | I/O | I/O | I/O |
| 38 | I/O | I/O | I/O | WD, I/O |
| 39 | I/O | I/O | I/O | WD, I/O |
| 40 | GND | I/O | I/O | I/O |
| 41 | I/O | I/O | I/O | I/O |
| 42 | I/O | I/O | I/O | I/O |
| 43 | I/O | VCCA | VCCA | VCCA |
| 44 | I/O | I/O | I/O | WD, I/O |
| 45 | I/O | I/O | I/O | WD, I/O |
| 46 | VCC | I/O | I/O | WD, I/O |

***Table 53 •*** **PQ208**

| **PQ208** | | | |
|---|---|---|---|
| **Pin Number** | **A42MX16 Function** | **A42MX24 Function** | **A42MX36 Function** |
| 169 | I/O | WD, I/O | WD, I/O |
| 170 | I/O | I/O | I/O |
| 171 | NC | I/O | QCLKD, I/O |
| 172 | I/O | I/O | I/O |
| 173 | I/O | I/O | I/O |
| 174 | I/O | I/O | I/O |
| 175 | I/O | I/O | I/O |
| 176 | I/O | WD, I/O | WD, I/O |
| 177 | I/O | WD, I/O | WD, I/O |
| 178 | PRA, I/O | PRA, I/O | PRA, I/O |
| 179 | I/O | I/O | I/O |
| 180 | CLKA, I/O | CLKA, I/O | CLKA, I/O |
| 181 | NC | I/O | I/O |
| 182 | NC | VCCI | VCCI |
| 183 | VCCA | VCCA | VCCA |
| 184 | GND | GND | GND |
| 185 | I/O | I/O | I/O |
| 186 | CLKB, I/O | CLKB, I/O | CLKB, I/O |
| 187 | I/O | I/O | I/O |
| 188 | PRB, I/O | PRB, I/O | PRB, I/O |
| 189 | I/O | I/O | I/O |
| 190 | I/O | WD, I/O | WD, I/O |
| 191 | I/O | WD, I/O | WD, I/O |
| 192 | I/O | I/O | I/O |
| 193 | NC | I/O | I/O |
| 194 | NC | WD, I/O | WD, I/O |
| 195 | NC | WD, I/O | WD, I/O |
| 196 | I/O | I/O | QCLKC, I/O |
| 197 | NC | I/O | I/O |
| 198 | I/O | I/O | I/O |
| 199 | I/O | I/O | I/O |
| 200 | I/O | I/O | I/O |
| 201 | NC | I/O | I/O |
| 202 | VCCI | VCCI | VCCI |
| 203 | I/O | WD, I/O | WD, I/O |
| 204 | I/O | WD, I/O | WD, I/O |
| 205 | I/O | I/O | I/O |

***Table 54 •*** **PQ240**

| **PQ240** | |
|---|---|
| **Pin Number** | **A42MX36 Function** |
| 89 | VCCI |
| 90 | VCCA |
| 91 | LP |
| 92 | TCK, I/O |
| 93 | I/O |
| 94 | GND |
| 95 | I/O |
| 96 | I/O |
| 97 | I/O |
| 98 | I/O |
| 99 | I/O |
| 100 | I/O |
| 101 | I/O |
| 102 | I/O |
| 103 | I/O |
| 104 | I/O |
| 105 | I/O |
| 106 | I/O |
| 107 | I/O |
| 108 | VCCI |
| 109 | I/O |
| 110 | I/O |
| 111 | I/O |
| 112 | I/O |
| 113 | I/O |
| 114 | I/O |
| 115 | I/O |
| 116 | I/O |
| 117 | I/O |
| 118 | VCCA |
| 119 | GND |
| 120 | GND |
| 121 | GND |
| 122 | I/O |
| 123 | SDO, TDO, I/O |
| 124 | I/O |
| 125 | WD, I/O |

***Table 54 •*** **PQ240**

| **PQ240** | |
|---|---|
| **Pin Number** | **A42MX36 Function** |
| 163 | WD, I/O |
| 164 | WD, I/O |
| 165 | I/O |
| 166 | QCLKA, I/O |
| 167 | I/O |
| 168 | I/O |
| 169 | I/O |
| 170 | I/O |
| 171 | I/O |
| 172 | VCCI |
| 173 | I/O |
| 174 | WD, I/O |
| 175 | WD, I/O |
| 176 | I/O |
| 177 | I/O |
| 178 | TDI, I/O |
| 179 | TMS, I/O |
| 180 | GND |
| 181 | VCCA |
| 182 | GND |
| 183 | I/O |
| 184 | I/O |
| 185 | I/O |
| 186 | I/O |
| 187 | I/O |
| 188 | I/O |
| 189 | I/O |
| 190 | I/O |
| 191 | I/O |
| 192 | VCCI |
| 193 | I/O |
| 194 | I/O |
| 195 | I/O |
| 196 | I/O |
| 197 | I/O |
| 198 | I/O |
| 199 | I/O |

***Table 56 •*** **VQ100**

| **VQ100** | | |
|---|---|---|
| **Pin Number** | **A42MX09 Function** | **A42MX16 Function** |
| 21 | I/O | I/O |
| 22 | I/O | I/O |
| 23 | I/O | I/O |
| 24 | I/O | I/O |
| 25 | I/O | I/O |
| 26 | I/O | I/O |
| 27 | I/O | I/O |
| 28 | I/O | I/O |
| 29 | I/O | I/O |
| 30 | I/O | I/O |
| 31 | I/O | I/O |
| 32 | GND | GND |
| 33 | I/O | I/O |
| 34 | I/O | I/O |
| 35 | I/O | I/O |
| 36 | I/O | I/O |
| 37 | I/O | I/O |
| 38 | VCCA | VCCA |
| 39 | I/O | I/O |
| 40 | I/O | I/O |
| 41 | I/O | I/O |
| 42 | I/O | I/O |
| 43 | I/O | I/O |
| 44 | GND | GND |
| 45 | I/O | I/O |
| 46 | I/O | I/O |
| 47 | I/O | I/O |
| 48 | I/O | I/O |
| 49 | I/O | I/O |
| 50 | SDO, I/O | SDO, I/O |
| 51 | I/O | I/O |
| 52 | I/O | I/O |
| 53 | I/O | I/O |
| 54 | I/O | I/O |
| 55 | GND | GND |
| 56 | I/O | I/O |

***Table 60 •*** **BG272**

| **BG272** | |
|---|---|
| **Pin Number** | **A42MX36 Function** |
| C3 | GND |
| C4 | I/O |
| C5 | WD, I/O |
| C6 | I/O |
| C7 | QCLKC, I/O |
| C8 | I/O |
| C9 | I/O |
| C10 | CLKB |
| C11 | PRA, I/O |
| C12 | WD, I/O |
| C13 | I/O |
| C14 | QCLKD, I/O |
| C15 | I/O |
| C16 | WD, I/O |
| C17 | SDI, I/O |
| C18 | I/O |
| C19 | I/O |
| C20 | I/O |
| D1 | I/O |
| D2 | I/O |
| D3 | I/O |
| D4 | I/O |
| D5 | VCCI |
| D6 | I/O |
| D7 | I/O |
| D8 | VCCA |
| D9 | WD, I/O |
| D10 | VCCI |
| D11 | I/O |
| D12 | VCCI |
| D13 | I/O |
| D14 | VCCI |
| D15 | I/O |
| D16 | VCCA |
| D17 | GND |
| D18 | I/O |
| D19 | I/O |

***Table 60 •*** **BG272**

| **BG272** | |
|---|---|
| **Pin Number** | **A42MX36 Function** |
| M10 | GND |
| M11 | GND |
| M12 | GND |
| M17 | I/O |
| M18 | I/O |
| M19 | I/O |
| M20 | I/O |
| N1 | I/O |
| N2 | I/O |
| N3 | I/O |
| N4 | VCCI |
| N17 | VCCI |
| N18 | I/O |
| N19 | I/O |
| N20 | I/O |
| P1 | I/O |
| P2 | I/O |
| P3 | I/O |
| P4 | VCCA |
| P17 | I/O |
| P18 | I/O |
| P19 | I/O |
| P20 | I/O |
| R1 | I/O |
| R2 | I/O |
| R3 | I/O |
| R4 | VCCI |
| R17 | VCCI |
| R18 | I/O |
| R19 | I/O |
| R20 | I/O |
| T1 | I/O |
| T2 | I/O |
| T3 | I/O |
| T4 | I/O |
| T17 | VCCA |
| T18 | I/O |