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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

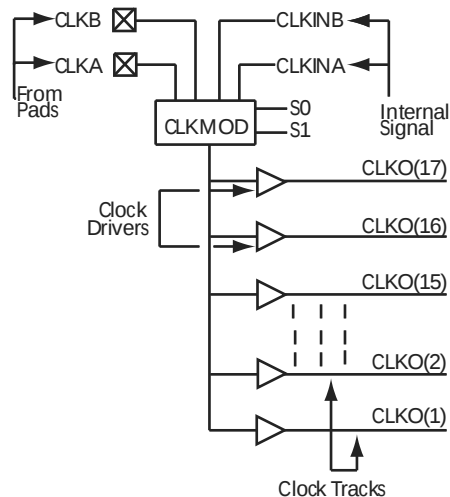
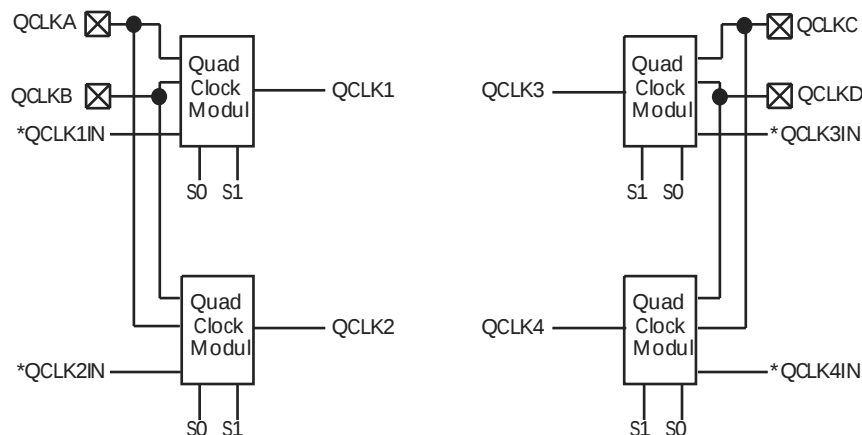
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	57
Number of Gates	3000
Voltage - Supply	3V ~ 3.6V, 4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	68-LCC (J-Lead)
Supplier Device Package	68-PLCC (24.23x24.23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a40mx02-pl68i

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Figure 8 • Clock Networks of 42MX Devices**Figure 9 • Quadrant Clock Network of A42MX36 Devices**

Note: *QCLK1IN, QCLK2IN, QCLK3IN, and QCLK4IN are internally-generated signals.

3.2.5 MultiPlex I/O Modules

42MX devices feature Multiplex I/Os and support 5.0 V, 3.3 V, and mixed 3.3 V/5.0 V operations.

The MultiPlex I/O modules provide the interface between the device pins and the logic array. Figure 10, page 12 is a block diagram of the 42MX I/O module. A variety of user functions, determined by a library macro selection, can be implemented in the module. (See the *Antifuse Macro Library Guide* for more information.) All 42MX I/O modules contain tristate buffers, with input and output latches that can be configured for input, output, or bidirectional operation.

All 42MX devices contain flexible I/O structures, where each output pin has a dedicated output-enable control (Figure 10, page 12). The I/O module can be used to latch input or output data, or both, providing fast set-up time. In addition, the Designer software tools can build a D-type flip-flop using a C-module combined with an I/O module to register input and output signals. See the *Antifuse Macro Library Guide* for more details.

A42MX24 and A42MX36 devices also offer selectable PCI output drives, enabling 100% compliance with version 2.1 of the PCI specification. For low-power systems, all inputs and outputs are turned off to reduce current consumption to below 500 μ A.

To achieve 5.0 V or 3.3 V PCI-compliant output drives on A42MX24 and A42MX36 devices, a chip-wide PCI fuse is programmed via the Device Selection Wizard in the Designer software (Figure 11, page 12). When the PCI fuse is not programmed, the output drive is standard.

Table 38 • A42MX09 Timing Characteristics (Nominal 5.0 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	4.5		4.9		5.6		6.6		9.2		ns
t _A	Flip-Flop Clock Input Period	3.5		3.8		4.3		5.1		7.1		ns
t _{INH}	Input Buffer Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{INSU}	Input Buffer Latch Set-Up	0.3		0.3		0.4		0.4		0.6		ns
t _{OUTH}	Output Buffer Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{OUTSU}	Output Buffer Latch Set-Up	0.3		0.3		0.4		0.4		0.6		ns
f _{MAX}	Flip-Flop (Latch) Clock Frequency		268		244		224		195		117	MHz

Table 42 • A42MX24 Timing Characteristics (Nominal 5.0 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description			–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Input Module Predicted Routing Delays ²													
t _{IRD1}	FO = 1 Routing Delay		1.8		2.0		2.3		2.7		3.8		ns
t _{IRD2}	FO = 2 Routing Delay		2.1		2.3		2.6		3.1		4.3		ns
t _{IRD3}	FO = 3 Routing Delay		2.3		2.5		2.9		3.4		4.8		ns
t _{IRD4}	FO = 4 Routing Delay		2.5		2.8		3.2		3.7		5.2		ns
t _{IRD8}	FO = 8 Routing Delay		3.4		3.8		4.3		5.1		7.1		ns
Global Clock Network													
t _{CKH}	Input LOW to HIGH	FO = 32	2.6		2.9		3.3		3.9		5.4		ns
		FO = 486	2.9		3.2		3.6		4.3		5.9		ns
t _{CKL}	Input HIGH to LOW	FO = 32	3.7		4.1		4.6		5.4		7.6		ns
		FO = 486	4.3		4.7		5.4		6.3		8.8		ns
t _{PWH}	Minimum Pulse Width HIGH	FO = 32	2.2	2.4	2.7		3.2		4.5				ns
		FO = 486	2.4	2.6	3.0		3.5		4.9				ns
t _{PWL}	Minimum Pulse Width LOW	FO = 32	2.2	2.4	2.7		3.2		4.5				ns
		FO = 486	2.4	2.6	3.0		3.5		4.9				ns
t _{CKSW}	Maximum Skew	FO = 32	0.5		0.6		0.7		0.8		1.1		ns
		FO = 486	0.5		0.6		0.7		0.8		1.1		ns
t _{SUEXT}	Input Latch External Set-Up	FO = 32	0.0	0.0	0.0		0.0		0.0				ns
		FO = 486	0.0	0.0	0.0		0.0		0.0				ns
t _{HEXT}	Input Latch External Hold	FO = 32	2.8	3.1	3.5		4.1		5.7				ns
		FO = 486	3.3	3.7	4.2		4.9		6.9				ns
t _P	Minimum Period (1/f _{MAX})	FO = 32	4.7	5.2	5.7		6.5		10.9				ns
		FO = 486	5.1	5.7	6.2		7.1		11.9				ns

Table 43 • A42MX24 Timing Characteristics (Nominal 3.3 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)

Parameter / Description			–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
TTL Output Module Timing ⁵ (continued)													
t _{LH}	I/O Latch Output Hold		0.0		0.0		0.0		0.0		0.0		ns
t _{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O			7.7		8.5		9.6		11.3		15.9	ns
t _{ACO}	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O			14.8		16.5		18.7		22.0		30.8	ns
d _{TLH}	Capacitive Loading, LOW to HIGH			0.05		0.05		0.06		0.07		0.10	ns/pF
d _{THL}	Capacitive Loading, HIGH to LOW			0.04		0.04		0.05		0.06		0.08	ns/pF
CMOS Output Module Timing ⁵													
t _{DLH}	Data-to-Pad HIGH			4.8		5.3		5.5		6.4		9.0	ns
t _{DHL}	Data-to-Pad LOW			3.5		3.9		4.1		4.9		6.8	ns
t _{ENZH}	Enable Pad Z to HIGH			3.6		4.0		4.5		5.3		7.4	ns
t _{ENZL}	Enable Pad Z to LOW			3.4		4.0		5.0		5.8		8.2	ns
t _{ENHZ}	Enable Pad HIGH to Z			7.2		8.0		9.0		10.7		14.9	ns
t _{ENLZ}	Enable Pad LOW to Z			6.7		7.5		8.5		9.9		13.9	ns
t _{GLH}	G-to-Pad HIGH			6.8		7.6		8.6		10.1		14.2	ns
t _{GHL}	G-to-Pad LOW			6.8		7.6		8.6		10.1		14.2	ns
t _{LSU}	I/O Latch Set-Up		0.7		0.7		0.8		1.0		1.4		ns
t _{LH}	I/O Latch Hold		0.0		0.0		0.0		0.0		0.0		ns
t _{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O			7.7		8.5		9.6		11.3		15.9	ns
t _{ACO}	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O			14.8		16.5		18.7		22.0		30.8	ns
d _{TLH}	Capacitive Loading, LOW to HIGH			0.05		0.05		0.06		0.07		0.10	ns/pF
d _{THL}	Capacitive Loading, HIGH to LOW			0.04		0.04		0.05		0.06		0.08	ns/pF
t _{HEXT}	Input Latch External Hold	FO = 32	3.9		4.3		4.9		5.7		8.1		ns
		FO = 486	4.6		5.2		5.8		6.9		9.6		ns
t _P	Minimum Period (1/f _{MAX})	FO = 32	7.8		8.7		9.5		10.8		18.2		ns
		FO = 486	8.6		9.5		10.4		11.9		19.9		ns

1. For dual-module macros, use t_{PD1} + t_{RD1} + t_{PDn}, t_{CO} + t_{RD1} + t_{PDn}, or t_{PD1} + t_{RD1} + t_{SUD}, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
4. Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.
5. Delays based on 35 pF loading.

Table 45 • A42MX36 Timing Characteristics (Nominal 3.3 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Synchronous SRAM Operations (continued)												
t _{ADH}	Address/Data Hold Time	0.0		0.0		0.0		0.0		0.0		ns
t _{RENSU}	Read Enable Set-Up	0.9		1.0		1.1		1.3		1.8		ns
t _{RENH}	Read Enable Hold	4.8		5.3		6.0		7.0		9.8		ns
t _{WENSU}	Write Enable Set-Up	3.8		4.2		4.8		5.6		7.8		ns
t _{WENH}	Write Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{BENS}	Block Enable Set-Up	3.9		4.3		4.9		5.7		8.0		ns
t _{BENH}	Block Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
Asynchronous SRAM Operations												
t _{RPD}	Asynchronous Access Time		11.3		12.6		14.3		16.8		23.5	ns
t _{RDADV}	Read Address Valid	12.3		13.7		15.5		18.2		25.5		ns
t _{ADSU}	Address/Data Set-Up Time	2.3		2.5		2.8		3.4		4.8		ns
t _{ADH}	Address/Data Hold Time	0.0		0.0		0.0		0.0		0.0		ns
t _{RENSUA}	Read Enable Set-Up to Address Valid	0.9		1.0		1.1		1.3		1.8		ns
t _{RENHA}	Read Enable Hold	4.8		5.3		6.0		7.0		9.8		ns
t _{WENSU}	Write Enable Set-Up	3.8		4.2		4.8		5.6		7.8		ns
t _{WENH}	Write Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{DOH}	Data Out Hold Time		1.8		2.0		2.1		2.5		3.5	ns
Input Module Propagation Delays												
t _{INPY}	Input Data Pad-to-Y		1.4		1.6		1.8		2.1		3.0	ns
t _{INGO}	Input Latch Gate-to-Output		2.0		2.2		2.5		2.9		4.1	ns
t _{INH}	Input Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{INSU}	Input Latch Set-Up	0.7		0.7		0.8		1.0		1.4		ns
t _{ILA}	Latch Active Pulse Width	6.5		7.3		8.2		9.7		13.5		ns

Table 45 • A42MX36 Timing Characteristics (Nominal 3.3 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)

Parameter / Description			–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Input Module Predicted Routing Delays ²													
t _{IRD1}	FO = 1 Routing Delay		2.8		3.1		3.5		4.1		5.7		ns
t _{IRD2}	FO = 2 Routing Delay		3.2		3.5		4.1		4.8		6.7		ns
t _{IRD3}	FO = 3 Routing Delay		3.7		4.1		4.7		5.5		7.7		ns
t _{IRD4}	FO = 4 Routing Delay		4.2		4.6		5.3		6.2		8.7		ns
t _{IRD8}	FO = 8 Routing Delay		6.1		6.8		7.7		9.0		12.6		ns
Global Clock Network													
t _{CKH}	Input LOW to HIGH	FO = 32	4.6		5.1		5.7		6.7		9.3		ns
		FO = 635	5.0		5.6		6.3		7.4		10.3		ns
t _{CKL}	Input HIGH to LOW	FO = 32	5.3		5.9		6.7		7.8		11.0		ns
		FO = 635	6.8		7.6		8.6		10.1		14.1		ns
t _{PWH}	Minimum Pulse Width HIGH	FO = 32	2.5		2.7		3.1		3.6		5.1		ns
		FO = 635	2.8		3.1		3.5		4.1		5.7		ns
t _{PWL}	Minimum Pulse Width LOW	FO = 32	2.5		2.7		3.1		3.6		5.1		ns
		FO = 635	2.8		3.1		3.5		4.1		5.7		ns
t _{CKSW}	Maximum Skew	FO = 32	1.0		1.2		1.3		1.5		2.2		ns
		FO = 635	1.0		1.2		1.3		1.5		2.2		ns
t _{SUEXT}	Input Latch External Set-Up	FO = 32	0.0		0.0		0.0		0.0		0.0		ns
		FO = 635	0.0		0.0		0.0		0.0		0.0		ns
t _{HEXT}	Input Latch External Hold	FO = 32	4.0		4.4		5.0		5.9		8.2		ns
		FO = 635	4.6		5.2		5.9		6.9		9.6		ns
t _P	Minimum Period (1/f _{MAX})	FO = 32	9.2		10.2		11.1		12.7		21.2		ns
		FO = 635	9.9		11.0		12.0		13.8		23.0		ns
f _{MAX}	Maximum Datapath Frequency	FO = 32	108		98		90		79		47		MHz
		FO = 635	100		91		83		73		44		MHz
TTL Output Module Timing ⁵													
t _{DLH}	Data-to-Pad HIGH		3.6		4.0		4.5		5.3		7.4		ns
t _{DHL}	Data-to-Pad LOW		4.2		4.6		5.2		6.2		8.6		ns
t _{ENZH}	Enable Pad Z to HIGH		3.7		4.2		4.7		5.5		7.7		ns
t _{ENZL}	Enable Pad Z to LOW		4.1		4.6		5.2		6.1		8.5		ns
t _{ENHZ}	Enable Pad HIGH to Z		7.34		8.2		9.3		10.9		15.3		ns
TTL Output Module Timing ⁵													
t _{ENLZ}	Enable Pad LOW to Z		6.9		7.6		8.7		10.2		14.3		ns
t _{GLH}	G-to-Pad HIGH		4.9		5.5		6.2		7.3		10.2		ns
t _{GHL}	G-to-Pad LOW		4.9		5.5		6.2		7.3		10.2		ns
t _{LSU}	I/O Latch Output Set-Up		0.7		0.7		0.8		1.0		1.4		ns
t _{LH}	I/O Latch Output Hold		0.0		0.0		0.0		0.0		0.0		ns
t _{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		7.9		8.8		10.0		11.8		16.5		ns

Table 45 • A42MX36 Timing Characteristics (Nominal 3.3 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)

Parameter / Description	–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{ACO} Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O		10.9		12.1		13.7		16.1		22.5	ns
d _{TLH} Capacitive Loading, LOW to HIGH		0.10		0.11		0.12		0.14		0.20	ns/pF
d _{THL} Capacitive Loading, HIGH to LOW		0.10		0.11		0.12		0.14		0.20	ns/pF
CMOS Output Module Timing⁵											
t _{DLH} Data-to-Pad HIGH		4.9		5.5		6.2		7.3		10.3	ns
t _{DHL} Data-to-Pad LOW		3.4		3.8		4.3		5.1		7.1	ns
t _{ENZH} Enable Pad Z to HIGH		3.7		4.1		4.7		5.5		7.7	ns
t _{ENZL} Enable Pad Z to LOW		4.1		4.6		5.2		6.1		8.5	ns
t _{ENHZ} Enable Pad HIGH to Z		7.4		8.2		9.3		10.9		15.3	ns
t _{ENLZ} Enable Pad LOW to Z		6.9		7.6		8.7		10.2		14.3	ns
t _{GLH} G-to-Pad HIGH		7.0		7.8		8.9		10.4		14.6	ns
t _{GHL} G-to-Pad LOW		7.0		7.8		8.9		10.4		14.6	ns
t _{LSU} I/O Latch Set-Up	0.7		0.7		0.8		1.0		1.4		ns
t _{LH} I/O Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{LCO} I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		7.9		8.8		10.0		11.8		16.5	ns

1. For dual-module macros, use t_{PD1} + t_{RD1} + t_{PDn}, t_{CO} + t_{RD1} + t_{PDn}, or t_{PD1} + t_{RD1} + t_{SUD}, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
4. Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.
5. Delays based on 35 pF loading.

3.12 Pin Descriptions

This section lists the pin descriptions for 40MX and 42MX series FPGAs.

CLK/A/B, I/O Global Clock

Clock inputs for clock distribution networks. CLK is for 40MX while CLKA and CLKB are for 42MX devices. The clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

DCLK, I/O Diagnostic Clock

Clock input for diagnostic probe and device programming. DCLK is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

GND, Ground

Input LOW supply voltage.

I/O, Input/Output

Table 48 • PL68

PL68		
Pin Number	A40MX02 Function	A40MX04 Function
24	I/O	I/O
25	VCC	VCC
26	I/O	I/O
27	I/O	I/O
28	I/O	I/O
29	I/O	I/O
30	I/O	I/O
31	I/O	I/O
32	GND	GND
33	I/O	I/O
34	I/O	I/O
35	I/O	I/O
36	I/O	I/O
37	I/O	I/O
38	VCC	VCC
39	I/O	I/O
40	I/O	I/O
41	I/O	I/O
42	I/O	I/O
43	I/O	I/O
44	I/O	I/O
45	I/O	I/O
46	I/O	I/O
47	I/O	I/O
48	I/O	I/O
49	GND	GND
50	I/O	I/O
51	I/O	I/O
52	CLK, I/O	CLK, I/O
53	I/O	I/O
54	MODE	MODE
55	VCC	VCC
56	SDI, I/O	SDI, I/O
57	DCLK, I/O	DCLK, I/O
58	PRA, I/O	PRA, I/O
59	PRB, I/O	PRB, I/O
60	I/O	I/O

Table 48 • PL68

PL68		
Pin Number	A40MX02 Function	A40MX04 Function
61	I/O	I/O
62	I/O	I/O
63	I/O	I/O
64	I/O	I/O
65	I/O	I/O
66	GND	GND
67	I/O	I/O
68	I/O	I/O

Figure 40 • PL84

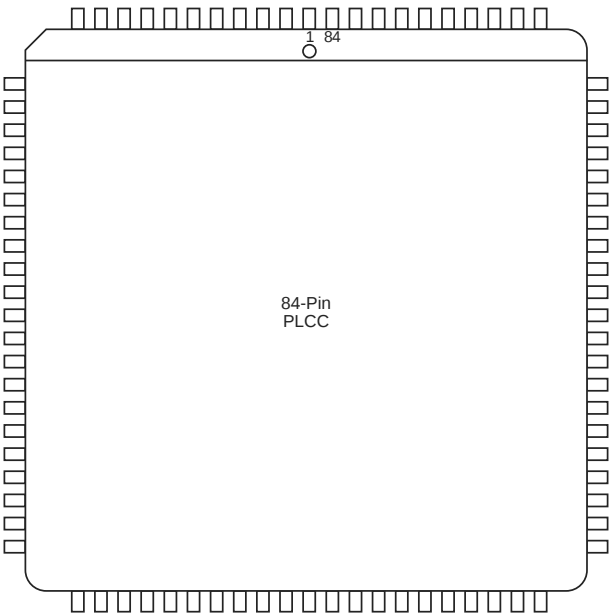


Table 49 • PL84

PL84				
Pin Number	A40MX04 Function	A42MX09 Function	A42MX16 Function	A42MX24 Function
1	I/O	I/O	I/O	I/O
2	I/O	CLKB, I/O	CLKB, I/O	CLKB, I/O
3	I/O	I/O	I/O	I/O
4	VCC	PRB, I/O	PRB, I/O	PRB, I/O
5	I/O	I/O	I/O	WD, I/O
6	I/O	GND	GND	GND
7	I/O	I/O	I/O	I/O
8	I/O	I/O	I/O	WD, I/O
9	I/O	I/O	I/O	WD, I/O

Table 52 • PQ160

PQ160			
Pin Number	A42MX09 Function	A42MX16 Function	A42MX24 Function
58	VCCI	VCCI	VCCI
59	GND	GND	GND
60	VCCA	VCCA	VCCA
61	LP	LP	LP
62	I/O	I/O	TCK, I/O
63	I/O	I/O	I/O
64	GND	GND	GND
65	I/O	I/O	I/O
66	I/O	I/O	I/O
67	I/O	I/O	I/O
68	I/O	I/O	I/O
69	GND	GND	GND
70	NC	I/O	I/O
71	I/O	I/O	I/O
72	I/O	I/O	I/O
73	I/O	I/O	I/O
74	I/O	I/O	I/O
75	NC	I/O	I/O
76	I/O	I/O	I/O
77	NC	I/O	I/O
78	I/O	I/O	I/O
79	NC	I/O	I/O
80	GND	GND	GND
81	I/O	I/O	I/O
82	SDO, I/O	SDO, I/O	SDO, TDO, I/O
83	I/O	I/O	WD, I/O
84	I/O	I/O	WD, I/O
85	I/O	I/O	I/O
86	NC	VCCI	VCCI
87	I/O	I/O	I/O
88	I/O	I/O	WD, I/O
89	GND	GND	GND
90	NC	I/O	I/O
91	I/O	I/O	I/O
92	I/O	I/O	I/O
93	I/O	I/O	I/O
94	I/O	I/O	I/O

Table 53 • PQ208

PQ208			
Pin Number	A42MX16 Function	A42MX24 Function	A42MX36 Function
21	I/O	I/O	I/O
22	GND	GND	GND
23	I/O	I/O	I/O
24	I/O	I/O	I/O
25	I/O	I/O	I/O
26	I/O	I/O	I/O
27	GND	GND	GND
28	VCCI	VCCI	VCCI
29	VCCA	VCCA	VCCA
30	I/O	I/O	I/O
31	I/O	I/O	I/O
32	VCCA	VCCA	VCCA
33	I/O	I/O	I/O
34	I/O	I/O	I/O
35	I/O	I/O	I/O
36	I/O	I/O	I/O
37	I/O	I/O	I/O
38	I/O	I/O	I/O
39	I/O	I/O	I/O
40	I/O	I/O	I/O
41	NC	I/O	I/O
42	NC	I/O	I/O
43	NC	I/O	I/O
44	I/O	I/O	I/O
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	I/O	I/O	I/O
48	I/O	I/O	I/O
49	I/O	I/O	I/O
50	NC	I/O	I/O
51	NC	I/O	I/O
52	GND	GND	GND
53	GND	GND	GND
54	I/O	TMS, I/O	TMS, I/O
55	I/O	TDI, I/O	TDI, I/O
56	I/O	I/O	I/O
57	I/O	WD, I/O	WD, I/O

Table 54 • PQ240

PQ240	
Pin Number	A42MX36 Function
15	QCLKC, I/O
16	I/O
17	WD, I/O
18	WD, I/O
19	I/O
20	I/O
21	WD, I/O
22	WD, I/O
23	I/O
24	PRB, I/O
25	I/O
26	CLKB, I/O
27	I/O
28	GND
29	VCCA
30	VCCI
31	I/O
32	CLKA, I/O
33	I/O
34	PRA, I/O
35	I/O
36	I/O
37	WD, I/O
38	WD, I/O
39	I/O
40	I/O
41	I/O
42	I/O
43	I/O
44	I/O
45	QCLKD, I/O
46	I/O
47	WD, I/O
48	WD, I/O
49	I/O
50	I/O
51	I/O

Table 55 • VQ80

VQ80		
Pin Number	A40MX02 Function	A40MX04 Function
13	VCC	VCC
14	I/O	I/O
15	I/O	I/O
16	I/O	I/O
17	NC	I/O
18	NC	I/O
19	NC	I/O
20	VCC	VCC
21	I/O	I/O
22	I/O	I/O
23	I/O	I/O
24	I/O	I/O
25	I/O	I/O
26	I/O	I/O
27	GND	GND
28	I/O	I/O
29	I/O	I/O
30	I/O	I/O
31	I/O	I/O
32	I/O	I/O
33	VCC	VCC
34	I/O	I/O
35	I/O	I/O
36	I/O	I/O
37	I/O	I/O
38	I/O	I/O
39	I/O	I/O
40	I/O	I/O
41	NC	I/O
42	NC	I/O
43	NC	I/O
44	I/O	I/O
45	I/O	I/O
46	I/O	I/O
47	GND	GND
48	I/O	I/O

Table 58 • CQ208

CQ208	
Pin Number	A42MX36 Function
185	I/O
186	CLKB, I/O
187	I/O
188	PRB, I/O
189	I/O
190	WD, I/O
191	WD, I/O
192	I/O
193	I/O
194	WD, I/O
195	WD, I/O
196	QCLKC, I/O
197	I/O
198	I/O
199	I/O
200	I/O
201	I/O
202	VCCI
203	WD, I/O
204	WD, I/O
205	I/O
206	I/O
207	DCLK, I/O
208	I/O

Table 59 • CQ256

CQ256	
Pin Number	A42MX36 Function
96	VCCA
97	GND
98	GND
99	I/O
100	I/O
101	I/O
102	I/O
103	I/O
104	I/O
105	WD, I/O
106	WD, I/O
107	I/O
108	I/O
109	WD, I/O
110	WD, I/O
111	I/O
112	QCLKA, I/O
113	I/O
114	GND
115	I/O
116	I/O
117	I/O
118	I/O
119	VCCI
120	I/O
121	WD, I/O
122	WD, I/O
123	I/O
124	I/O
125	I/O
126	I/O
127	GND
128	NC
129	NC
130	NC
131	GND
132	I/O

Table 61 • PG132

PG132	
Pin Number	A42MX09 Function
F2	I/O
F1	I/O
G1	I/O
G4	VSV
H1	I/O
H2	I/O
H3	I/O
H4	I/O
J1	I/O
K1	I/O
L1	I/O
K2	I/O
M1	I/O
K3	I/O
L2	I/O
N1	I/O
L3	BININ
M2	BINOUT
N2	I/O
M3	I/O
L4	I/O
N3	I/O
M4	I/O
N4	I/O
M5	I/O
K6	I/O
N5	I/O
N6	I/O
L6	I/O
M6	I/O
M7	I/O
N7	I/O
N8	I/O
M8	I/O
L8	I/O
K8	I/O
N9	I/O

Table 61 • PG132

PG132	
Pin Number	A42MX09 Function
N10	I/O
M10	I/O
N11	I/O
L10	I/O
M11	I/O
N12	SDO
M12	I/O
L11	I/O
N13	I/O
M13	I/O
K11	I/O
L12	I/O
L13	I/O
K13	I/O
H10	I/O
J12	I/O
J13	I/O
H11	I/O
H12	I/O
H13	VKS
G13	VPP

Figure 53 • CQ172

Table 62 • CQ172

CQ172	
Pin Number	A42MX16 Function
1	MODE
2	I/O
3	I/O
4	I/O
5	I/O
6	I/O
7	GND
8	I/O
9	I/O
10	I/O
11	I/O
12	VCC
13	I/O
14	I/O
15	I/O
16	I/O
17	GND
18	I/O
19	I/O
20	I/O

Table 62 • CQ172

60	I/O
61	I/O
62	I/O
63	I/O
64	I/O
65	GND
66	VCC
67	I/O
68	I/O
69	I/O
70	I/O
71	I/O
72	I/O
73	I/O
74	I/O
75	GND
76	I/O
77	I/O
78	I/O
79	I/O
80	VCCI
81	I/O
82	I/O
83	I/O
84	I/O
85	SDO
86	I/O
87	I/O
88	I/O
89	I/O
90	I/O
91	I/O
92	I/O
93	I/O
94	I/O
95	I/O
96	I/O
97	I/O
98	GND