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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	34
Number of Gates	3000
Voltage - Supply	3V ~ 3.6V, 4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a40mx02-plg44

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2.6 Temperature Grade Offerings

Table 4 • Temperature Grade Offerings

Package	A40MX02	A40MX04	A42MX09	A42MX16	A42MX24	A42MX36
PLCC 44	C, I, M	C, I, M				
PLCC 68	C, I, A, M	C, I, M				
PLCC 84		C, I, A, M	C, I, A, M	C, I, M	C, I, M	
PQFP 100	C, I, A, M	C, I, A, M	C, I, A, M	C, I, M		
PQFP 144			C			
PQFP 160			C, I, A, M	C, I, M	C, I, A, M	
PQFP 208				C, I, A, M	C, I, A, M	C, I, A, M
PQFP 240						C, I, A, M
VQFP 80	C, I, A, M	C, I, A, M				
VQFP 100			C, I, A, M	C, I, A, M		
TQFP 176			C, I, A, M	C, I, A, M	C, I, A, M	
PBGA 272						C, I, M
CQFP 172				C, M, B		
CQFP 208						C, M, B
CQFP 256						C, M, B
CPGA 132			C, M, B			

Note: C = Commercial
 I = Industrial
 A = Automotive
 M = Military
 B = MIL-STD-883 Class B

2.7 Speed Grade Offerings

Table 5 • Speed Grade Offerings

	- F	Std	-1	-2	-3
C	P	P	P	P	P
I		P	P	P	P
A		P			
M		P	P		
B		P	P		

Note: See the 40MX and 42MX Automotive Family FPGAs datasheet for details on automotive-grade MX offerings.

Contact your local *Microsemi Sales representative* for device availability.

reliability. Devices should not be operated outside the recommended operating conditions.

Table 21 • Recommended Operating Conditions

Parameter	Commercial	Industrial	Military	Units
Temperature Range*	0 to +70	−40 to +85	−55 to +125	°C
VCCA	4.75 to 5.25	4.5 to 5.5	4.5 to 5.5	V
VCCI	3.14 to 3.47	3.0 to 3.6	3.0 to 3.6	V

Note: *Ambient temperature (T_A) is used for commercial and industrial grades; case temperature (T_C) is used for military grades.

3.9.1 Mixed 5.0V/3.3V Electrical Specifications

Table 22 • Mixed 5.0V/3.3V Electrical Specifications

Symbol	Parameter	Commercial		Commercial –F		Industrial		Military		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
VOH ¹	IOH = –10 mA	2.4		2.4						V
	IOH = –4 mA					2.4		2.4		V
VOL ¹	IOL = 10 mA	0.5		0.5						V
	IOL = 6 mA					0.4		0.4		V
VIL		–0.3	0.8	–0.3	0.8	–0.3	0.8	–0.3	0.8	V
VIH ²		2.0	VCCA + 0.3	2.0	VCCA + 0.3	2.0	VCCA + 0.3	2.0	VCCA + 0.3	V
IL	VIN = 0.5 V	–10		–10		–10		–10		μA
IH	VIN = 2.7 V	–10		–10		–10		–10		μA
Input Transition Time, TR and TF		500		500		500		500		ns
C _{IO} I/O Capacitance		10		10		10		10		pF
Standby Current, ICC ³	A42MX09	5		25		25		25		mA
	A42MX16	6		25		25		25		mA
	A42MX24, A42MX36	20		25		25		25		mA
Low Power Mode Standby Current		0.5		ICC – 5.0		ICC – 5.0		ICC – 5.0		mA
I/O I/O source sink current	Can be derived from the <i>IBIS model</i> (http://www.microsemi.com/soc/techdocs/models/ibis.html)									

1. Only one output tested at a time. VCCI = min.
2. VIH(Min) is 2.4V for A42MX36 family. This applies only to VCCI of 5V and is not applicable to VCCI of 3.3V
3. All outputs unloaded. All inputs = VCCI or GND

3.9.2 Output Drive Characteristics for 5.0 V PCI Signaling

MX PCI device I/O drivers were designed specifically for high-performance PCI systems. Figure 16, page 28 shows the typical output drive characteristics of the MX devices. MX output drivers are compliant with the PCI Local Bus Specification.

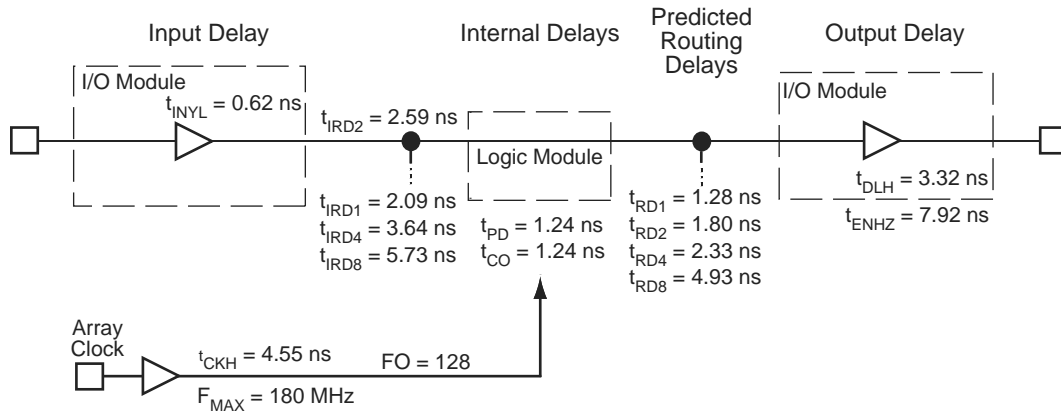
Table 23 • DC Specification (5.0 V PCI Signaling)¹

Symbol	Parameter	Condition	PCI		MX		Units
			Min.	Max.	Min.	Max.	
VCCI	Supply Voltage for I/Os		4.75	5.25	4.75	5.25 ²	V
VIH ³	Input High Voltage		2.0	VCC + 0.5	2.0	VCCI + 0.3	V
VIL	Input Low Voltage		–0.5	0.8	–0.3	0.8	V
I _{IH}	Input High Leakage Current	VIN = 2.7 V		70	—	10	μA
I _{IL}	Input Low Leakage Current	VIN=0.5 V		–70	—	–10	μA
VOH	Output High Voltage	I _O UT = –2 mA I _O UT = –6 mA	2.4		3.84		V
VOL	Output Low Voltage	I _O UT = 3 mA, 6 mA		0.55	—	0.33	V

3.10 Timing Models

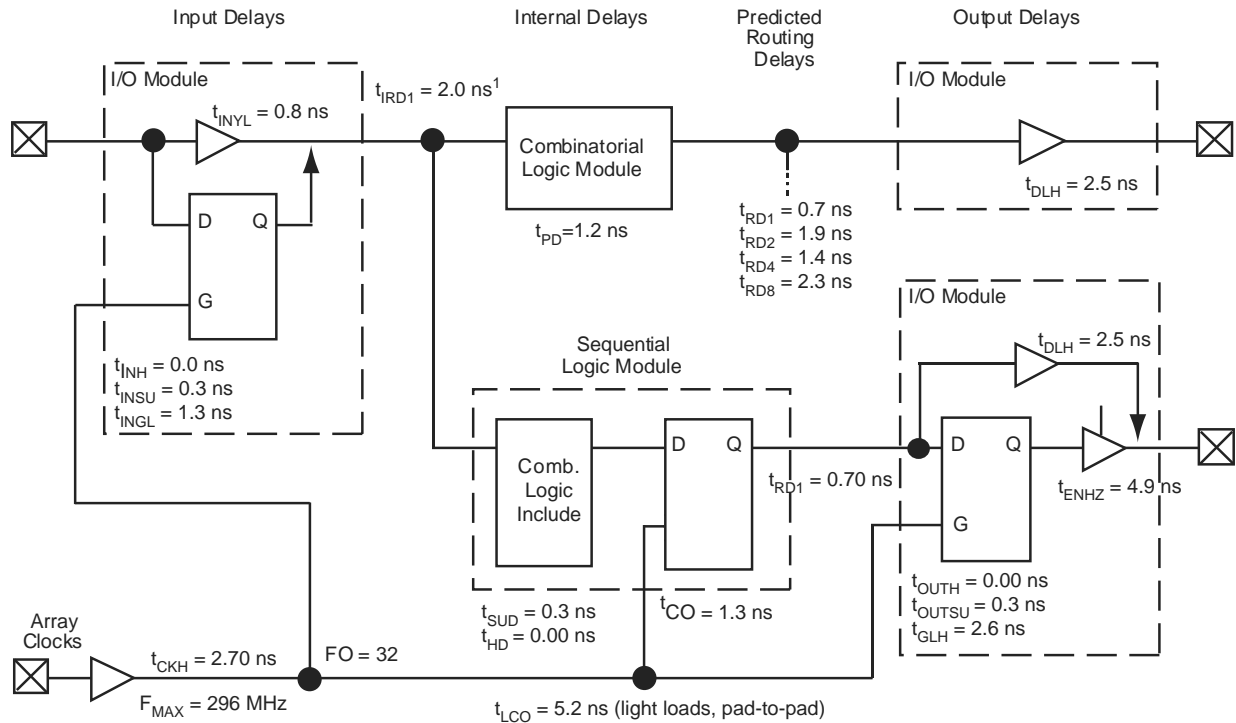
The following figures show various timing models.

Figure 17 • 40MX Timing Model*



Note: Values are shown for 40MX –3 speed devices at 5.0 V worst-case commercial conditions.

Figure 18 • 42MX Timing Model



Note: 1. Input module predicted routing delay

Note: 2. Values are shown for A42MX09 –3 at 5.0 V worst-case commercial conditions.

approximately a 3 ns to a 6 ns delay, which is represented statistically in higher fanout (FO=8) routing delays in the data sheet specifications section, shown in Table 34, page 41.

3.11.3 Timing Derating

MX devices are manufactured with a CMOS process. Therefore, device performance varies according to temperature, voltage, and process changes. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature and best-case processing. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature and worst-case processing.

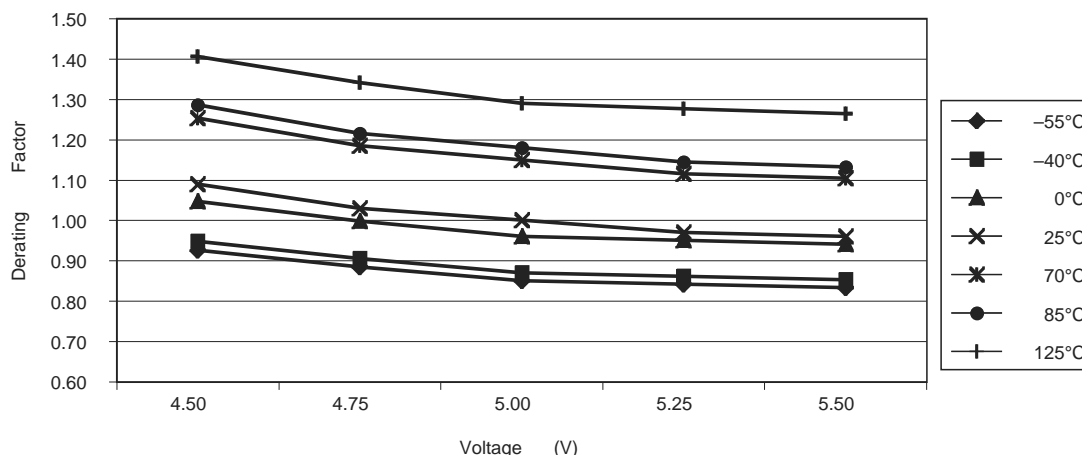
3.11.4 Temperature and Voltage Derating Factors

The following tables and figures show temperature and voltage derating factors for 40MX and 42MX FPGAs.

Table 28 • 42MX Temperature and Voltage Derating Factors (Normalized to $T_J = 25^\circ\text{C}$, $V_{CCA} = 5.0\text{ V}$)

42MX Voltage	Temperature						
	-55°C	-40°C	0°C	25°C	70°C	85°C	125°C
4.50	0.93	0.95	1.05	1.09	1.25	1.29	1.41
4.75	0.88	0.90	1.00	1.03	1.18	1.22	1.34
5.00	0.85	0.87	0.96	1.00	1.15	1.18	1.29
5.25	0.84	0.86	0.95	0.97	1.12	1.14	1.28
5.50	0.83	0.85	0.94	0.96	1.10	1.13	1.26

Figure 34 • 42MX Junction Temperature and Voltage Derating Curves (Normalized to $T_J = 25^\circ\text{C}$, $V_{CCA} = 5.0\text{ V}$)



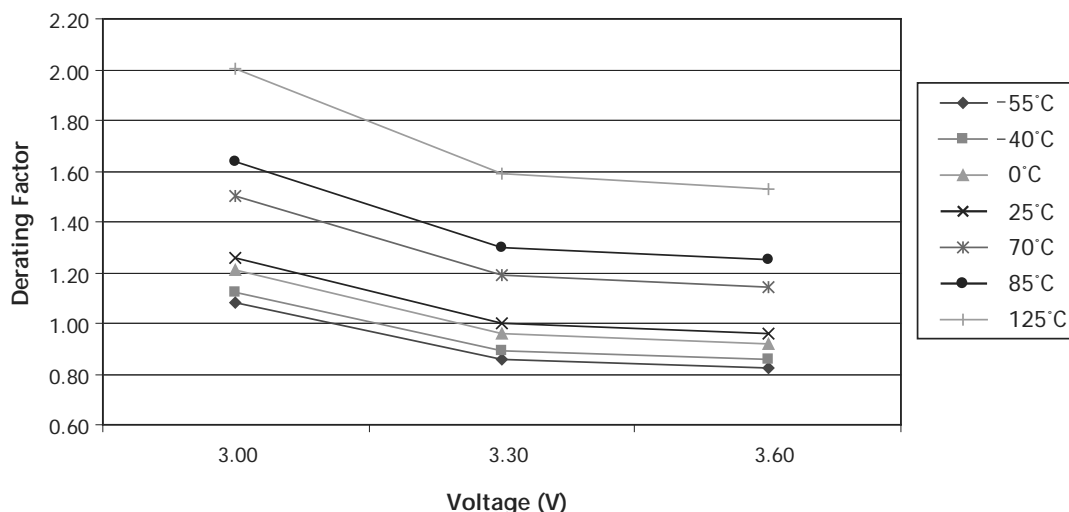
Note: This derating factor applies to all routing and propagation delays

Table 29 • 40MX Temperature and Voltage Derating Factors (Normalized to $T_J = 25^\circ\text{C}$, $V_{CC} = 5.0\text{ V}$)

40MX Voltage	Temperature						
	-55°C	-40°C	0°C	25°C	70°C	85°C	125°C
4.50	0.89	0.93	1.02	1.09	1.25	1.31	1.45
4.75	0.84	0.88	0.97	1.03	1.18	1.24	1.37
5.00	0.82	0.85	0.94	1.00	1.15	1.20	1.33
5.25	0.80	0.82	0.91	0.97	1.12	1.16	1.29
5.50	0.79	0.82	0.90	0.96	1.10	1.15	1.28

Table 31 • 40MX Temperature and Voltage Derating Factors (Normalized to $T_J = 25^\circ\text{C}$, $V_{CC} = 3.3\text{ V}$)

40MX Voltage	Temperature						
	-55°C	-40°C	0°C	25°C	70°C	85°C	125°C
3.60	0.83	0.85	0.92	0.96	1.14	1.25	1.53

Figure 37 • 40MX Junction Temperature and Voltage Derating Curves (Normalized to $T_J = 25^\circ\text{C}$, $V_{CC} = 3.3\text{ V}$)

Note: This derating factor applies to all routing and propagation delays

3.11.5 PCI System Timing Specification

The following tables list the critical PCI timing parameters and the corresponding timing parameters for the MX PCI-compliant devices.

3.11.6 PCI Models

Microsemi provides synthesizable VHDL and Verilog-HDL models for a PCI Target interface, a PCI Target and Target+DMA Master interface. Contact the Microsemi sales representative for more details.

Table 32 • Clock Specification for 33 MHz PCI

Symbol	Parameter	PCI		A42MX24		A42MX36		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYC}	CLK Cycle Time	30	–	4.0	–	4.0	–	ns
t_{HIGH}	CLK High Time	11	–	1.9	–	1.9	–	ns
t_{LOW}	CLK Low Time	11	–	1.9	–	1.9	–	ns

Table 33 • Timing Parameters for 33 MHz PCI

Symbol	Parameter	PCI		A42MX24		A42MX36		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{VAL}	CLK to Signal Valid—Bused Signals	2	11	2.0	9.0	2.0	9.0	ns
$t_{\text{VAL(PTP)}}$	CLK to Signal Valid—Point-to-Point	2 ²	12	2.0	9.0	2.0	9.0	ns
t_{ON}	Float to Active	2	–	2.0	4.0	2.0	4.0	ns
t_{OFF}	Active to Float	–	28	–	8.3 ¹	–	8.3 ¹	ns
t_{SU}	Input Set-Up Time to CLK—Bused Signals	7	–	1.5	–	1.5	–	ns

Table 34 • A40MX02 Timing Characteristics (Nominal 5.0 V Operation) (continued)
(Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C)

Parameter / Description	-3 Speed		-2 Speed		-1 Speed		Std Speed		-F Speed		Units
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
TTL Output Module Timing⁴											
t _{DLH}	Data-to-Pad HIGH	3.3		3.8		4.3		5.1		7.2	ns
t _{DHL}	Data-to-Pad LOW	4.0		4.6		5.2		6.1		8.6	ns
t _{ENZH}	Enable Pad Z to HIGH	3.7		4.3		4.9		5.8		8.0	ns
t _{ENZL}	Enable Pad Z to LOW	4.7		5.4		6.1		7.2		10.1	ns
t _{ENHZ}	Enable Pad HIGH to Z	7.9		9.1		10.4		12.2		17.1	ns
t _{ENLZ}	Enable Pad LOW to Z	5.9		6.8		7.7		9.0		12.6	ns
d _{TLH}	Delta LOW to HIGH	0.02		0.02		0.03		0.03		0.04	ns/pF
d _{THL}	Delta HIGH to LOW	0.03		0.03		0.03		0.04		0.06	ns/pF
CMOS Output Module Timing⁴											
t _{DLH}	Data-to-Pad HIGH	3.9		4.5		5.1		6.05		8.5	ns
t _{DHL}	Data-to-Pad LOW	3.4		3.9		4.4		5.2		7.3	ns
t _{ENZH}	Enable Pad Z to HIGH	3.4		3.9		4.4		5.2		7.3	ns
t _{ENZL}	Enable Pad Z to LOW	4.9		5.6		6.4		7.5		10.5	ns
t _{ENHZ}	Enable Pad HIGH to Z	7.9		9.1		10.4		12.2		17.0	ns
t _{ENLZ}	Enable Pad LOW to Z	5.9		6.8		7.7		9.0		12.6	ns
d _{TLH}	Delta LOW to HIGH	0.03		0.04		0.04		0.05		0.07	ns/pF
d _{THL}	Delta HIGH to LOW	0.02		0.02		0.03		0.03		0.04	ns/pF

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance
2. Set-up times assume fanout of 3. Further testing information can be obtained from the Timer utility
3. The hold time for the DFME1A macro may be greater than 0 ns. Use the Timer tool from the Designer software to check the hold time for this macro.
4. Delays based on 35pF loading

Table 35 • A40MX02 Timing Characteristics (Nominal 3.3 V Operation)
(Worst-Case Commercial Conditions, VCC = 3.0 V, T_J = 70°C)

Parameter / Description	-3 Speed		-2 Speed		-1 Speed		Std Speed		-F Speed		Units
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Logic Module Propagation Delays											
t _{PD1}	Single Module	1.7		2.0		2.3		2.7		3.7	ns
t _{PD2}	Dual-Module Macros	3.7		4.3		4.9		5.7		8.0	ns
t _{CO}	Sequential Clock-to-Q	1.7		2.0		2.3		2.7		3.7	ns
t _{GO}	Latch G-to-Q	1.7		2.0		2.3		2.7		3.7	ns
t _{RS}	Flip-Flop (Latch) Reset-to-Q	1.7		2.0		2.3		2.7		3.7	ns
Logic Module Predicted Routing Delays¹											

Table 37 • A40MX04 Timing Characteristics (Nominal 3.3 V Operation) (continued)(Worst-Case Commercial Conditions, VCC = 3.0 V, T_J = 70°C)

Parameter / Description	–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
CMOS Output Module Timing⁴											
t _{DLH}	Data-to-Pad HIGH	5.5	6.4	7.2	8.5	11.9	ns				
t _{DHL}	Data-to-Pad LOW	4.8	5.5	6.2	7.3	10.2	ns				
t _{ENZH}	Enable Pad Z to HIGH	4.7	5.5	6.2	7.3	10.2	ns				
t _{ENZL}	Enable Pad Z to LOW	6.8	7.9	8.9	10.5	14.7	ns				
t _{ENHZ}	Enable Pad HIGH to Z	11.1	12.8	14.5	17.1	23.9	ns				
t _{ENLZ}	Enable Pad LOW to Z	8.2	9.5	10.7	12.6	17.7	ns				
d _{TLH}	Delta LOW to HIGH	0.05	0.05	0.06	0.07	0.10	ns/pF				
d _{THL}	Delta HIGH to LOW	0.03	0.03	0.04	0.04	0.06	ns/pF				

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
2. Set-up times assume fanout of 3. Further testing information can be obtained from the Timer utility.
3. The hold time for the DFME1A macro may be greater than 0 ns. Use the Timer tool from the Designer software to check the hold time for this macro.
4. Delays based on 35 pF loading.

Table 38 • A42MX09 Timing Characteristics (Nominal 5.0 V Operation) (Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description	–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Logic Module Propagation Delays¹											
t _{PD1}	Single Module	1.2	1.3	1.5	1.8	2.5	ns				
t _{CO}	Sequential Clock-to-Q	1.3	1.4	1.6	1.9	2.7	ns				
t _{GO}	Latch G-to-Q	1.2	1.4	1.6	1.8	2.6	ns				
t _{RS}	Flip-Flop (Latch) Reset-to-Q	1.2	1.6	1.8	2.1	2.9	ns				
Logic Module Predicted Routing Delays²											
t _{RD1}	FO = 1 Routing Delay	0.7	0.8	0.9	1.0	1.4	ns				
t _{RD2}	FO = 2 Routing Delay	0.9	1.0	1.2	1.4	1.9	ns				
t _{RD3}	FO = 3 Routing Delay	1.2	1.3	1.5	1.7	2.4	ns				
t _{RD4}	FO = 4 Routing Delay	1.4	1.5	1.7	2.0	2.9	ns				
t _{RD8}	FO = 8 Routing Delay	2.3	2.6	2.9	3.4	4.8	ns				
Logic Module Sequential Timing^{3, 4}											
t _{SUD}	Flip-Flop (Latch) Data Input Set-Up	0.3	0.4	0.4	0.5	0.7	ns				
t _{HD}	Flip-Flop (Latch) Data Input Hold	0.0	0.0	0.0	0.0	0.0	ns				
t _{SUENA}	Flip-Flop (Latch) Enable Set-Up	0.4	0.5	0.5	0.6	0.8	ns				
t _{HENA}	Flip-Flop (Latch) Enable Hold	0.0	0.0	0.0	0.0	0.0	ns				
t _{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	3.4	3.8	4.3	5.0	7.0	ns				

Table 43 • A42MX24 Timing Characteristics (Nominal 3.3 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)

Parameter / Description	-3 Speed		-2 Speed		-1 Speed		Std Speed		-F Speed		Units
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
TTL Output Module Timing⁵ (continued)											
t _{LH}	I/O Latch Output Hold	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	ns
t _{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O	7.7	8.5	9.6	11.3	15.9					ns
t _{ACO}	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O	14.8	16.5	18.7	22.0	30.8					ns
d _{TLH}	Capacitive Loading, LOW to HIGH	0.05	0.05	0.06	0.07	0.10					ns/pF
d _{THL}	Capacitive Loading, HIGH to LOW	0.04	0.04	0.05	0.06	0.08					ns/pF
CMOS Output Module Timing⁵											
t _{DLH}	Data-to-Pad HIGH	4.8	5.3	5.5	6.4	9.0					ns
t _{DHL}	Data-to-Pad LOW	3.5	3.9	4.1	4.9	6.8					ns
t _{ENZH}	Enable Pad Z to HIGH	3.6	4.0	4.5	5.3	7.4					ns
t _{ENZL}	Enable Pad Z to LOW	3.4	4.0	5.0	5.8	8.2					ns
t _{ENHZ}	Enable Pad HIGH to Z	7.2	8.0	9.0	10.7	14.9					ns
t _{ENLZ}	Enable Pad LOW to Z	6.7	7.5	8.5	9.9	13.9					ns
t _{GLH}	G-to-Pad HIGH	6.8	7.6	8.6	10.1	14.2					ns
t _{GHL}	G-to-Pad LOW	6.8	7.6	8.6	10.1	14.2					ns
t _{LSU}	I/O Latch Set-Up	0.7	0.7	0.8	1.0	1.4					ns
t _{LH}	I/O Latch Hold	0.0	0.0	0.0	0.0	0.0					ns
t _{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O	7.7	8.5	9.6	11.3	15.9					ns
t _{ACO}	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O	14.8	16.5	18.7	22.0	30.8					ns
d _{TLH}	Capacitive Loading, LOW to HIGH	0.05	0.05	0.06	0.07	0.10					ns/pF
d _{THL}	Capacitive Loading, HIGH to LOW	0.04	0.04	0.05	0.06	0.08					ns/pF
t _{HEXT}	Input Latch External Hold	FO = 32 FO = 486	3.9 4.6	4.3 5.2	4.9 5.8	5.7 6.9	8.1 9.6				ns ns
t _P	Minimum Period (1/f _{MAX})	FO = 32 FO = 486	7.8 8.6	8.7 9.5	9.5 10.4	10.8 11.9	18.2 19.9				ns ns

1. For dual-module macros, use t_{PD1} + t_{RD1} + t_{PDn}, t_{CO} + t_{RD1} + t_{PDn}, or t_{PD1} + t_{RD1} + t_{SUD}, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
4. Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.
5. Delays based on 35 pF loading.

Table 44 • A42MX36 Timing Characteristics (Nominal 5.0 V Operation)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description		-3 Speed		-2 Speed		-1 Speed		Std Speed		-F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Asynchronous SRAM Operations												
t _{RPD}	Asynchronous Access Time		8.1		9.0		10.2		12.0		16.8	ns
t _{RDADV}	Read Address Valid		8.8		9.8		11.1		13.0		18.2	ns
t _{ADSU}	Address/Data Set-Up Time		1.6		1.8		2.0		2.4		3.4	ns
t _{ADH}	Address/Data Hold Time		0.0		0.0		0.0		0.0		0.0	ns
t _{RENSUA}	Read Enable Set-Up to Address Valid		0.6		0.7		0.8		0.9		1.3	ns
t _{RENHA}	Read Enable Hold		3.4		3.8		4.3		5.0		7.0	ns
t _{WENSU}	Write Enable Set-Up		2.7		3.0		3.4		4.0		5.6	ns
t _{WENH}	Write Enable Hold		0.0		0.0		0.0		0.0		0.0	ns
t _{DOH}	Data Out Hold Time		1.2		1.3		1.5		1.8		2.5	ns
Input Module Propagation Delays												
t _{INPY}	Input Data Pad-to-Y		1.0		1.1		1.3		1.5		2.1	ns
t _{INGO}	Input Latch Gate-to-Output		1.4		1.6		1.8		2.1		2.9	ns
t _{INH}	Input Latch Hold		0.0		0.0		0.0		0.0		0.0	ns
t _{INSU}	Input Latch Set-Up		0.5		0.5		0.6		0.7		1.0	ns
t _{ILA}	Latch Active Pulse Width		4.7		5.2		5.9		6.9		9.7	ns
Input Module Predicted Routing Delays²												
t _{IRD1}	FO = 1 Routing Delay		2.0		2.2		2.5		2.9		4.1	ns
t _{IRD2}	FO = 2 Routing Delay		2.3		2.6		2.9		3.4		4.8	ns
t _{IRD3}	FO = 3 Routing Delay		2.6		2.9		3.3		3.9		5.5	ns
t _{IRD4}	FO = 4 Routing Delay		3.0		3.3		3.8		4.4		6.2	ns
t _{IRD8}	FO = 8 Routing Delay		4.3		4.8		5.5		6.4		9.0	ns
Global Clock Network												
t _{CKH}	Input LOW to HIGH	FO = 32	2.7		3.0		3.4		4.0		5.6	ns
		FO = 635	3.0		3.3		3.8		4.4		6.2	ns
t _{CKL}	Input HIGH to LOW	FO = 32	3.8		4.2		4.8		5.6		7.8	ns
		FO = 635	4.9		5.4		6.1		7.2		10.1	ns
t _{PWH}	Minimum Pulse Width HIGH	FO = 32	1.8		2.0		2.2		2.6		3.6	ns
		FO = 635	2.0		2.2		2.5		2.9		4.1	ns
t _{PWL}	Minimum Pulse Width LOW	FO = 32	1.8		2.0		2.2		2.6		3.6	ns
		FO = 635	2.0		2.2		2.5		2.9		4.1	ns
t _{CKSW}	Maximum Skew	FO = 32	0.8		0.8		0.9		1.0		1.4	ns
		FO = 635	0.8		0.8		0.9		1.0		1.4	ns

Table 44 • A42MX36 Timing Characteristics (Nominal 5.0 V Operation)(Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)

Parameter / Description	-3 Speed		-2 Speed		-1 Speed		Std Speed		-F Speed		Units
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
TTL Output Module Timing⁵ (Continued)											
t _{ENLZ}	Enable Pad LOW to Z		4.9	5.5	6.2	7.3	10.2	ns			
t _{GLH}	G-to-Pad HIGH		2.9	3.3	3.7	4.4	6.1	ns			
t _{GHL}	G-to-Pad LOW		2.9	3.3	3.7	4.4	6.1	ns			
t _{LSU}	I/O Latch Output Set-Up		0.5	0.5	0.6	0.7	1.0	ns			
t _{LH}	I/O Latch Output Hold		0.0	0.0	0.0	0.0	0.0	ns			
t _{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		5.7	6.3	7.1	8.4	11.8	ns			
t _{ACO}	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O		7.8	8.6	9.8	11.5	16.1	ns			
d _{TLH}	Capacitive Loading, LOW to HIGH		0.07	0.08	0.09	0.10	0.14	ns/pF			
d _{THL}	Capacitive Loading, HIGH to LOW		0.07	0.08	0.09	0.10	0.14	ns/pF			

Table 47 • PL44

PL44		
Pin Number	A40MX02 Function	A40MX04 Function
21	GND	GND
22	I/O	I/O
23	I/O	I/O
24	I/O	I/O
25	VCC	VCC
26	I/O	I/O
27	I/O	I/O
28	I/O	I/O
29	I/O	I/O
30	I/O	I/O
31	I/O	I/O
32	GND	GND
33	CLK, I/O	CLK, I/O
34	MODE	MODE
35	VCC	VCC
36	SDI, I/O	SDI, I/O
37	DCLK, I/O	DCLK, I/O
38	PRA, I/O	PRA, I/O
39	PRB, I/O	PRB, I/O
40	I/O	I/O
41	I/O	I/O
42	I/O	I/O
43	GND	GND
44	I/O	I/O

Table 48 • PL68

PL68		
Pin Number	A40MX02 Function	A40MX04 Function
24	I/O	I/O
25	VCC	VCC
26	I/O	I/O
27	I/O	I/O
28	I/O	I/O
29	I/O	I/O
30	I/O	I/O
31	I/O	I/O
32	GND	GND
33	I/O	I/O
34	I/O	I/O
35	I/O	I/O
36	I/O	I/O
37	I/O	I/O
38	VCC	VCC
39	I/O	I/O
40	I/O	I/O
41	I/O	I/O
42	I/O	I/O
43	I/O	I/O
44	I/O	I/O
45	I/O	I/O
46	I/O	I/O
47	I/O	I/O
48	I/O	I/O
49	GND	GND
50	I/O	I/O
51	I/O	I/O
52	CLK, I/O	CLK, I/O
53	I/O	I/O
54	MODE	MODE
55	VCC	VCC
56	SDI, I/O	SDI, I/O
57	DCLK, I/O	DCLK, I/O
58	PRA, I/O	PRA, I/O
59	PRB, I/O	PRB, I/O
60	I/O	I/O

Table 51 • PQ144

PQ144	
Pin Number	A42MX09 Function
6	I/O
7	I/O
8	I/O
9	GNDQ
10	GNDI
11	NC
12	I/O
13	I/O
14	I/O
15	I/O
16	I/O
17	I/O
18	VSV
19	VCC
20	VCCI
21	NC
22	I/O
23	I/O
24	I/O
25	I/O
26	I/O
27	I/O
28	GND
29	GNDI
30	NC
31	I/O
32	I/O
33	I/O
34	I/O
35	I/O
36	I/O
37	BININ
38	BINOUT
39	I/O
40	I/O
41	I/O
42	I/O

Table 52 • PQ160

PQ160			
Pin Number	A42MX09 Function	A42MX16 Function	A42MX24 Function
58	VCCI	VCCI	VCCI
59	GND	GND	GND
60	VCCA	VCCA	VCCA
61	LP	LP	LP
62	I/O	I/O	TCK, I/O
63	I/O	I/O	I/O
64	GND	GND	GND
65	I/O	I/O	I/O
66	I/O	I/O	I/O
67	I/O	I/O	I/O
68	I/O	I/O	I/O
69	GND	GND	GND
70	NC	I/O	I/O
71	I/O	I/O	I/O
72	I/O	I/O	I/O
73	I/O	I/O	I/O
74	I/O	I/O	I/O
75	NC	I/O	I/O
76	I/O	I/O	I/O
77	NC	I/O	I/O
78	I/O	I/O	I/O
79	NC	I/O	I/O
80	GND	GND	GND
81	I/O	I/O	I/O
82	SDO, I/O	SDO, I/O	SDO, TDO, I/O
83	I/O	I/O	WD, I/O
84	I/O	I/O	WD, I/O
85	I/O	I/O	I/O
86	NC	VCCI	VCCI
87	I/O	I/O	I/O
88	I/O	I/O	WD, I/O
89	GND	GND	GND
90	NC	I/O	I/O
91	I/O	I/O	I/O
92	I/O	I/O	I/O
93	I/O	I/O	I/O
94	I/O	I/O	I/O

Table 57 • TQ176

TQ176			
Pin Number	A42MX09 Function	A42MX16 Function	A42MX24 Function
47	I/O	I/O	TDI, I/O
48	I/O	I/O	I/O
49	I/O	I/O	WD, I/O
50	I/O	I/O	WD, I/O
51	I/O	I/O	I/O
52	NC	VCCI	VCCI
53	I/O	I/O	I/O
54	NC	I/O	I/O
55	NC	I/O	WD, I/O
56	I/O	I/O	WD, I/O
57	NC	NC	I/O
58	I/O	I/O	I/O
59	I/O	I/O	WD, I/O
60	I/O	I/O	WD, I/O
61	NC	I/O	I/O
62	I/O	I/O	I/O
63	I/O	I/O	I/O
64	NC	I/O	I/O
65	I/O	I/O	I/O
66	NC	I/O	I/O
67	GND	GND	GND
68	VCCA	VCCA	VCCA
69	I/O	I/O	WD, I/O
70	I/O	I/O	WD, I/O
71	I/O	I/O	I/O
72	I/O	I/O	I/O
73	I/O	I/O	I/O
74	NC	I/O	I/O
75	I/O	I/O	I/O
76	I/O	I/O	I/O
77	NC	NC	WD, I/O
78	NC	I/O	WD, I/O
79	I/O	I/O	I/O
80	NC	I/O	I/O
81	I/O	I/O	I/O
82	NC	VCCI	VCCI
83	I/O	I/O	I/O

Table 58 • CQ208

CQ208	
Pin Number	A42MX36 Function
185	I/O
186	CLKB, I/O
187	I/O
188	PRB, I/O
189	I/O
190	WD, I/O
191	WD, I/O
192	I/O
193	I/O
194	WD, I/O
195	WD, I/O
196	QCLKC, I/O
197	I/O
198	I/O
199	I/O
200	I/O
201	I/O
202	VCCI
203	WD, I/O
204	WD, I/O
205	I/O
206	I/O
207	DCLK, I/O
208	I/O

Table 62 • CQ172

21	I/O
22	GND
23	VCCI
24	VSV
25	I/O
26	I/O
27	VCC
28	I/O
29	I/O
30	I/O
31	I/O
32	GND
33	I/O
34	I/O
35	I/O
36	I/O
37	GND
38	I/O
39	I/O
40	I/O
41	I/O
42	I/O
43	I/O
44	BININ
45	BINOUT
46	I/O
47	I/O
48	I/O
49	I/O
50	VCCI
51	I/O
52	I/O
53	I/O
54	I/O
55	GND
56	I/O
57	I/O
58	I/O
59	I/O

Table 62 • CQ172

138	I/O
139	I/O
140	I/O
141	GND
142	I/O
143	I/O
144	I/O
145	I/O
146	I/O
147	I/O
148	PROBA
149	I/O
150	CLKA
151	VCC
152	GND
153	I/O
154	CLKB
155	I/O
156	PROBB
157	I/O
158	I/O
159	I/O
160	I/O
161	GND
162	I/O
163	I/O
164	I/O
165	I/O
166	VCCI
167	I/O
168	I/O
169	I/O
170	I/O
171	DCLK