Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	57
Number of Gates	3000
Voltage - Supply	3V ~ 3.6V, 4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 125°C (TA)
Package / Case	80-TQFP
Supplier Device Package	80-VQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a40mx02-vq80a

3.2.3.3   Antifuse Structures

An antifuse is a "normally open" structure. The use of antifuses to implement a programmable logic device results in highly testable structures as well as efficient programming algorithms. There are no pre-existing connections; temporary connections can be made using pass transistors. These temporary connections can isolate individual antifuses to be programmed and individual circuit structures to be tested, which can be done before and after programming. For instance, all metal tracks can be tested for continuity and shorts between adjacent tracks, and the functionality of all logic modules can be verified.

Figure 7 •   **MX Routing Structure**
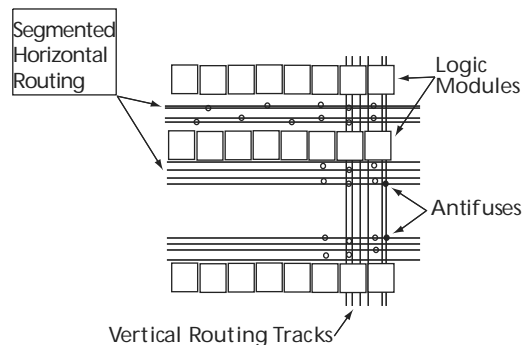
3.2.4   Clock Networks

The 40MX devices have one global clock distribution network (CLK). A signal can be put on the CLK network by being routed through the CLKBUF buffer.

In 42MX devices, there are two low-skew, high-fanout clock distribution networks, referred to as CLKA and CLKB. Each network has a clock module (CLKMOD) that can select the source of the clock signal from any of the following (Figure 8, page 11):

*   Externally from the CLKA pad, using CLKBUF buffer
*   Externally from the CLKB pad, using CLKBUF buffer
*   Internally from the CLKINTA input, using CLKINT buffer
*   Internally from the CLKINTB input, using CLKINT buffer

The clock modules are located in the top row of I/O modules. Clock drivers and a dedicated horizontal clock track are located in each horizontal routing channel.

Clock input pads in both 40MX and 42MX devices can also be used as normal I/Os, bypassing the clock networks.

The A42MX36 device has four additional register control resources, called quadrant clock networks (Figure 9, page 11). Each quadrant clock provides a local, high-fanout resource to the contiguous logic modules within its quadrant of the device. Quadrant clock signals can originate from specific I/O pins or from the internal array and can be used as a secondary register clock, register clear, or output enable.
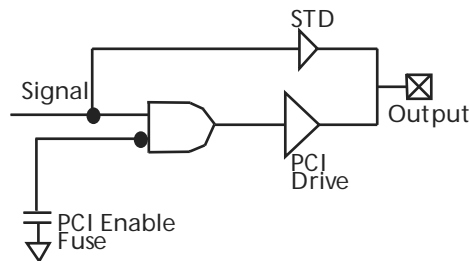
Designer software development tools provide a design library of I/O macro functions that can implement all I/O configurations supported by the MX FPGAs.

Figure 10 • **42MX I/O Module**
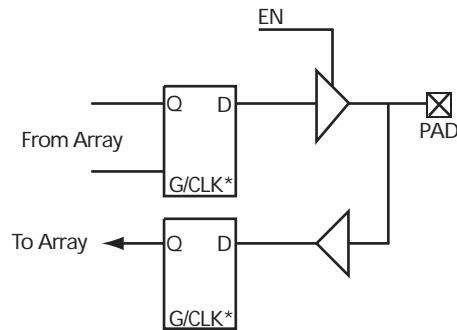
Note: *Can be configured as a Latch or D Flip-Flop (Using C-Module)*

Figure 11 • **PCI Output Structure of A42MX24 and A42MX36 Devices**

3.3 Other Architectural Features

The following sections cover other architectural features of 40MX and 42MX FPGAs.

3.3.1 Performance

MX devices can operate with internal clock frequencies of 250 MHz, enabling fast execution of complex logic functions. MX devices are live on power-up and do not require auxiliary configuration devices and thus are an optimal platform to integrate the functionality contained in multiple programmable logic devices. In addition, designs that previously would have required a gate array to meet performance can be integrated into an MX device with improvements in cost and time-to-market. Using timing-driven place-and-route (TDPR) tools, designers can achieve highly deterministic device performance.

3.3.2 User Security

Microsemi FuseLock provides robust security against design theft. Special security fuses are hidden in the fabric of the device and protect against unauthorized users attempting to access the programming and/or probe interfaces. It is virtually impossible to identify or bypass these fuses without damaging the device, making Microsemi antifuse FPGAs protected with the highest level of security available from both invasive and noninvasive attacks.

Special security fuses in 40MX devices include the Probe Fuse and Program Fuse. The former disables the probing circuitry while the latter prohibits further programming of all fuses, including the Probe Fuse. In 42MX devices, there is the Security Fuse which, when programmed, both disables the probing circuitry and prohibits further programming of the device.

3.3.3 Programming

Device programming is supported through the Silicon Sculptor series of programmers. Silicon Sculptor is a compact, robust, single-site and multi-site device programmer for the PC. With standalone software, Silicon Sculptor is designed to allow concurrent programming of multiple units from the same PC.

- VCCA = Power supply in volts (V)
- F = Switching frequency in megahertz (MHz)

3.4.4 Equivalent Capacitance

Equivalent capacitance is calculated by measuring ICCactive at a specified frequency and voltage for each circuit component of interest. Measurements have been made over a range of frequencies at a fixed value of VCC. Equivalent capacitance is frequency-independent, so the results can be used over a wide range of operating conditions. Equivalent capacitance values are shown below.

3.4.5 C$_{EQ}$ Values for Microsemi MX FPGAs

Modules (C$_{EQM}$)3.5

Input Buffers (C$_{EQI}$)6.9

Output Buffers (C$_{EQO}$)18.2

Routed Array Clock Buffer Loads (C$_{EQCR}$)1.4

To calculate the active power dissipated from the complete design, the switching frequency of each part of the logic must be known. The equation below shows a piece-wise linear summation over all components.

$$\text{Power} = \text{VCCA}^2 *[(m \times C_{EQM}*f_m)_{modules} + (n*C_{EQI}*f_n)_{inputs} + \overline{}(p*(C_{EQO} + C_L)*f_p)_{outputs} +$$

$$0.5*(q_1*C_{EQCR}*f_{q1})_{routed\_Clk1} + (r_{1*}f_{q1})_{routed\_Clk1} +$$

$$0.5*(q_2*C_{EQCR}*f_{q2})_{routed\_Clk2} + (r_{2*}f_{q2})_{routed\_Clk2}(2)]$$

EQ 3

where:

m = Number of logic modules switching at frequency f$_m$

n = Number of input buffers switching at frequency f$_n$

p = Number of output buffers switching at frequency f$_p$

q$_1$ = Number of clock loads on the first routed array clock

q$_2$ = Number of clock loads on the second routed array clock

r$_1$ = Fixed capacitance due to first routed array clock

r$_2$ = Fixed capacitance due to second routed array clock

C$_{EQM}$ = Equivalent capacitance of logic modules in pF

C$_{EQI}$ = Equivalent capacitance of input buffers in pF

C$_{EQO}$ = Equivalent capacitance of output buffers in pF

C$_{EQCR}$ = Equivalent capacitance of routed array clock in pF

C$_L$ = Output load capacitance in pF

f$_m$ = Average logic module switching rate in MHz

f$_n$ = Average input buffer switching rate in MHz

f$_p$ = Average output buffer switching rate in MHz

f$_{q1}$ = Average first routed array clock rate in MHz

Additionally, the back-annotation flow is compatible with all the major simulators and the simulation results can be cross-probed with Silicon Explorer II, Microsemi's integrated verification and logic analysis tool. Another tool included in the Libero software is the SmartGen macro builder, which easily creates popular and commonly used logic functions for implementation into your schematic or HDL design.

Microsemi's Libero software is compatible with the most popular FPGA design entry and verification tools from companies such as Mentor Graphics, Synopsys, and Cadence design systems.

See the Libero IDE web content at www.microsemi.com/soc/products/software/libero/default.aspx for further information on licensing and current operating system support.

3.6 Related Documents

The following sections give the list of related documents which can be refered for this datasheet.

3.6.1 Application Notes

- *AC278: BSDL Files Format Description*
- *AC225: Programming Antifuse Devices*
- *AC168: Implementation of Security in Microsemi Antifuse FPGAs*

3.6.2 User Guides and Manuals

- *Antifuse Macro Library Guide*
- *Silicon Sculptor Programmers User Guide*

3.6.3 Miscellaneous

Libero IDE Flow Diagram

3.7 5.0 V Operating Conditions

The following tables show 5.0 V operating conditions.

Table 12 •   **Absolute Maximum Ratings for 40MX Devices***

Symbol	Parameter	Limits	Units
VCC	DC Supply Voltage	−0.5 to +7.0	V
VI	Input Voltage	−0.5 to VCC+0.5	V
VO	Output Voltage	−0.5 to VCC+0.5	V
t_{STG}	Storage Temperature	−65 to +150	°C

Note: *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the recommended operating conditions.

Table 13 •   **Absolute Maximum Ratings for 42MX Devices***

Symbol	Parameter	Limits	Units
VCCI	DC Supply Voltage for I/Os	−0.5 to +7.0	V
VCCA	DC Supply Voltage for Array	−0.5 to +7.0	V
VI	Input Voltage	−0.5 to VCCI+0.5	V
VO	Output Voltage	−0.5 to VCCI+0.5	V
t_{STG}	Storage Temperature	−65 to +150	°C

reliability. Devices should not be operated outside the recommended operating conditions.

Table 21 • **Recommended Operating Conditions**

Parameter	Commercial	Industrial	Military	Units
Temperature Range*	0 to +70	–40 to +85	–55 to +125	°C
VCCA	4.75 to 5.25	4.5 to 5.5	4.5 to 5.5	V
VCCI	3.14 to 3.47	3.0 to 3.6	3.0 to 3.6	V

Note: *Ambient temperature (T_A) is used for commercial and industrial grades; case temperature (T_C) is used for military grades.

Figure 16 • **Typical Output Drive Characteristics (Based Upon Measured Data)**
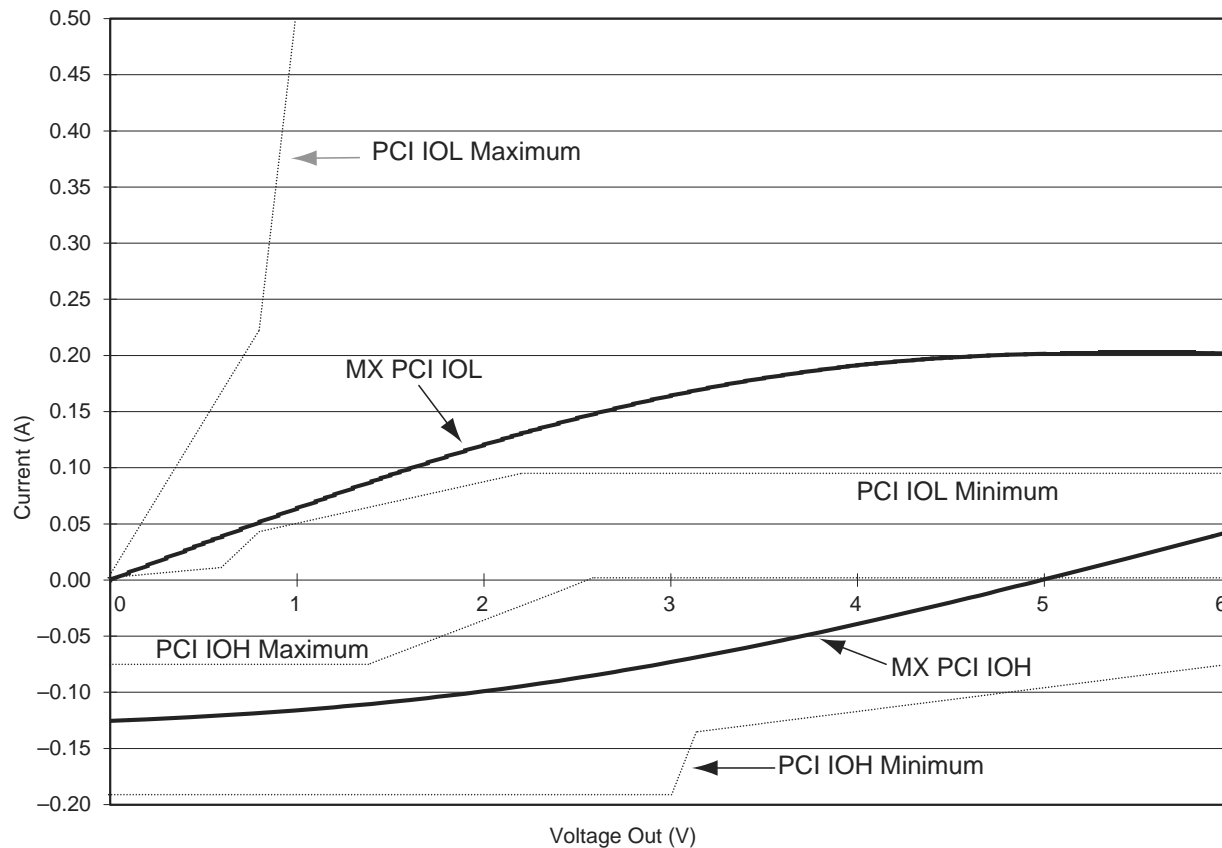
3.9.4 Junction Temperature (T$_J$)

The temperature variable in the Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because the heat generated from dynamic power consumption is usually hotter than the ambient temperature. The following equation can be used to calculate junction temperature.

$$\text{Junction Temperature} = \Delta T + T_a (1)$$

EQ 4

where:

- T_a = Ambient Temperature
- ΔT = Temperature gradient between junction (silicon) and ambient
- $\Delta T = \theta_{ja} * P$ (2)
- P = Power
- θ_{ja} = Junction to ambient of package. θ_{ja} numbers are located in Table 27, page 29.

3.9.5 Package Thermal Characteristics

The device junction-to-case thermal characteristic is θ_{jc}, and the junction-to-ambient air characteristic is θ_{ja}. The thermal characteristics for θ_{ja} are shown with two different air flow rates.

The maximum junction temperature is 150°C.

Maximum power dissipation for commercial- and industrial-grade devices is a function of θ_{ja}.

Figure 19 • **42MX Timing Model (Logic Functions Using Quadrant Clocks)**
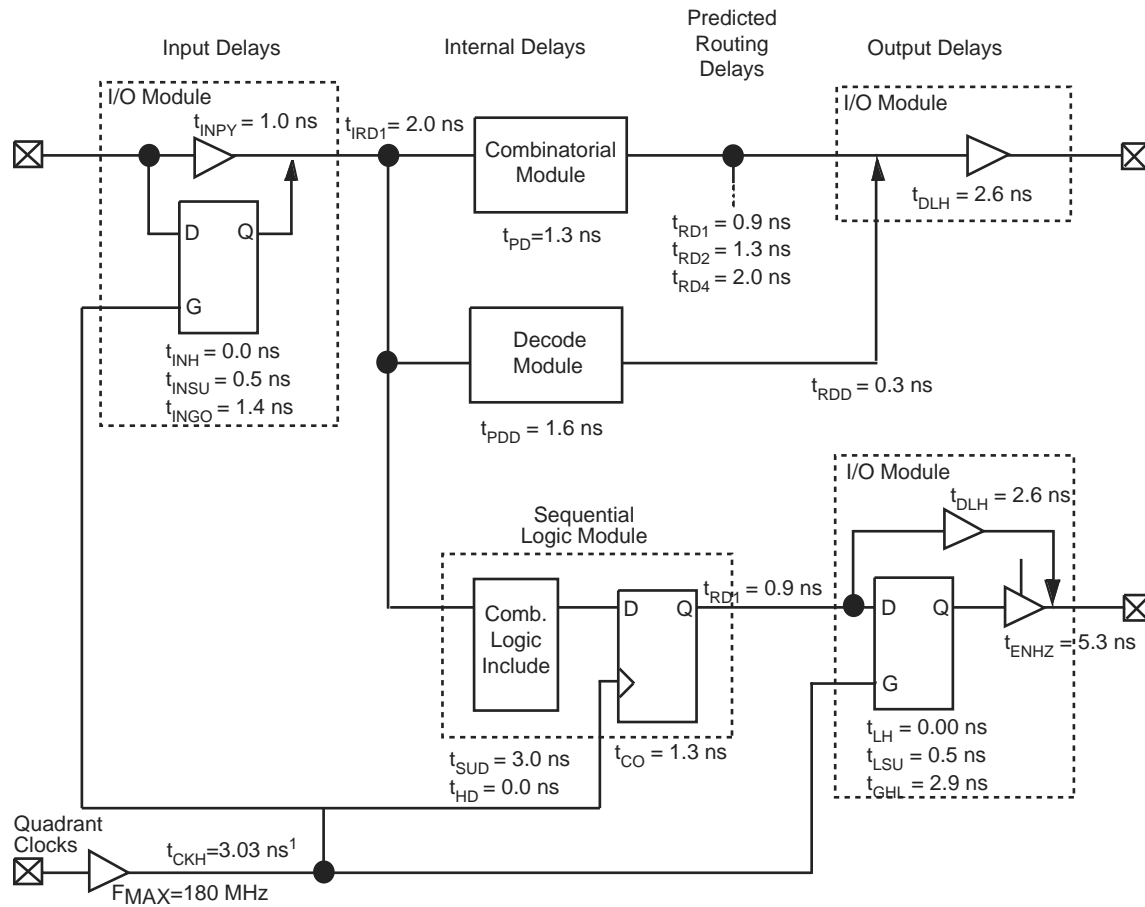
Note: 1. Load-dependent

Note: 2. Values are shown for A42MX36 –3 at 5.0 V worst-case commercial conditions

Figure 33 • **42MX SRAM Asynchronous Read Operation—Type 2 (Write Address Controlled)**

3.10.7 Predictable Performance: Tight Delay Distributions

Propagation delay between logic modules depends on the resistive and capacitive loading of the routing tracks, the interconnect elements, and the module inputs being driven. Propagation delay increases as the length of routing tracks, the number of interconnect elements, or the number of inputs increases.

From a design perspective, the propagation delay can be statistically correlated or modeled by the fanout (number of loads) driven by a module. Higher fanout usually requires some paths to have longer routing tracks.
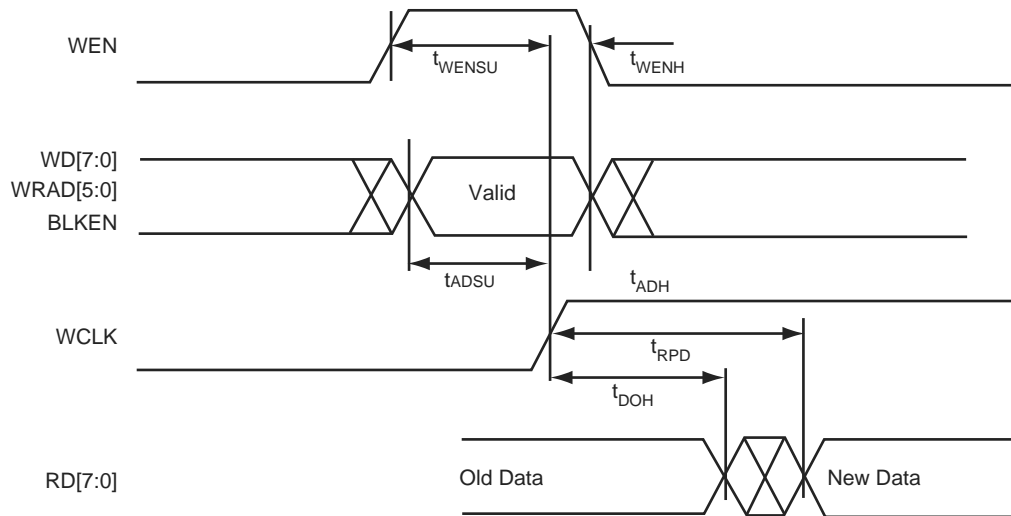
The MX FPGAs deliver a tight fanout delay distribution, which is achieved in two ways: by decreasing the delay of the interconnect elements and by decreasing the number of interconnect elements per path.

Microsemi's patented antifuse offers a very low resistive/capacitive interconnect. The antifuses, fabricated in 0.45 µm lithography, offer nominal levels of 100 Ω resistance and 7.0 fF capacitance per antifuse.

MX fanout distribution is also tight due to the low number of antifuses required for each interconnect path. The proprietary architecture limits the number of antifuses per path to a maximum of four, with 90 percent of interconnects using only two antifuses.

3.11 Timing Characteristics

Device timing characteristics fall into three categories: family-dependent, device-dependent, and design-dependent. The input and output buffer characteristics are common to all MX devices. Internal routing delays are device-dependent; actual delays are not determined until after place-and-route of the user's design is complete. Delay values may then be determined by using the Designer software utility or by performing simulation with post-layout delays.

3.11.1 Critical Nets and Typical Nets

Propagation delays are expressed only for typical nets, which are used for initial design performance evaluation. Critical net delays can then be applied to the most timing critical paths. Critical nets are determined by net property assignment in Microsemi's Designer software prior to placement and routing. Up to 6% of the nets in a design may be designated as critical.

3.11.2 Long Tracks

Some nets in the design use long tracks, which are special routing resources that span multiple rows, columns, or modules. Long tracks employ three and sometimes four antifuse connections, which increase capacitance and resistance, resulting in longer net delays for macros connected to long tracks. Typically, up to 6 percent of nets in a fully utilized device require long tracks. Long tracks add

Table 38 • **A42MX09 Timing Characteristics (Nominal 5.0 V Operation)** *(continued)***(Worst-Case Commercial Conditions, VCCA = 4.75 V, T$_J$ = 70°C)**

Parameter / Description		–3 Speed Min.	Max.	–2 Speed Min.	Max.	–1 Speed Min.	Max.	Std Speed Min.	Max.	–F Speed Min.	Max.	Units
t$_{WASYN}$	Flip-Flop (Latch) Asynchronous Pulse Width	4.5		4.9		5.6		6.6		9.2		ns
t$_A$	Flip-Flop Clock Input Period	3.5		3.8		4.3		5.1		7.1		ns
t$_{INH}$	Input Buffer Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t$_{INSU}$	Input Buffer Latch Set-Up	0.3		0.3		0.4		0.4		0.6		ns
t$_{OUTH}$	Output Buffer Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t$_{OUTSU}$	Output Buffer Latch Set-Up	0.3		0.3		0.4		0.4		0.6		ns
f$_{MAX}$	Flip-Flop (Latch) Clock Frequency		268		244		224		195		117	MHz

Table 39 • **A42MX09 Timing Characteristics (Nominal 3.3 V Operation)** *(continued)***(Worst-Case Commercial Conditions, VCCA = 3.0 V, T$_J$ = 70°C)**

Parameter / Description		–3 Speed Min.	–3 Speed Max.	–2 Speed Min.	–2 Speed Max.	–1 Speed Min.	–1 Speed Max.	Std Speed Min.	Std Speed Max.	–F Speed Min.	–F Speed Max.	Units
TTL Output Module Timing[5]												
t_{DLH}	Data-to-Pad HIGH		3.4		3.8		4.3		5.1		7.1	ns
t_{DHL}	Data-to-Pad LOW		4.0		4.5		5.1		6.1		8.3	ns
t_{ENZH}	Enable Pad Z to HIGH		3.7		4.1		4.6		5.5		7.6	ns
t_{ENZL}	Enable Pad Z to LOW		4.1		4.5		5.1		6.1		8.5	ns
t_{ENHZ}	Enable Pad HIGH to Z		6.9		7.6		8.6		10.2		14.2	ns
t_{ENLZ}	Enable Pad LOW to Z		7.5		8.3		9.4		11.1		15.5	ns
t_{GLH}	G-to-Pad HIGH		5.8		6.5		7.3		8.6		12.0	ns
t_{GHL}	G-to-Pad LOW		5.8		6.5		7.3		8.6		12.0	ns
t_{LSU}	I/O Latch Set-Up	0.7		0.8		0.9		1.0		1.4		ns
t_{LH}	I/O Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading		8.7		9.7		10.9		12.9		18.0	ns
t_{ACO}	Array Clock-to-Out (Pad-to-Pad),64 Clock Loading		12.2		13.5		15.4		18.1		25.3	ns
d_{TLH}	Capacity Loading, LOW to HIGH		0.00		0.00		0.00		0.10		0.01	ns/pF
d_{THL}	Capacity Loading, HIGH to LOW		0.09		0.10		0.10		0.10		0.10	ns/pF

Table 39 • **A42MX09 Timing Characteristics (Nominal 3.3 V Operation)** *(continued)***(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)**

Parameter / Description		–3 Speed Min.	–3 Speed Max.	–2 Speed Min.	–2 Speed Max.	–1 Speed Min.	–1 Speed Max.	Std Speed Min.	Std Speed Max.	–F Speed Min.	–F Speed Max.	Units
CMOS Output Module Timing[5]												
t_{DLH}	Data-to-Pad HIGH		3.4		3.8		5.5		6.4		9.0	ns
t_{DHL}	Data-to-Pad LOW		4.1		4.5		4.2		5.0		7.0	ns
t_{ENZH}	Enable Pad Z to HIGH		3.7		4.1		4.6		5.5		7.6	ns
t_{ENZL}	Enable Pad Z to LOW		4.1		4.5		5.1		6.1		8.5	ns
t_{ENHZ}	Enable Pad HIGH to Z		6.9		7.6		8.6		10.2		14.2	ns
t_{ENLZ}	Enable Pad LOW to Z		7.5		8.3		9.4		11.1		15.5	ns
t_{GLH}	G-to-Pad HIGH		5.8		6.5		7.3		8.6		12.0	ns
t_{GHL}	G-to-Pad LOW		5.8		6.5		7.3		8.6		12.0	ns
t_{LSU}	I/O Latch Set-Up	0.7		0.8		0.9		1.0		1.4		ns
t_{LH}	I/O Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading		8.7		9.7		10.9		12.9		18.0	ns
t_{ACO}	Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading		12.2		13.5		15.4		18.1		25.3	ns
d_{TLH}	Capacity Loading, LOW to HIGH		0.04		0.04		0.05		0.06		0.08	ns/pF
d_{THL}	Capacity Loading, HIGH to LOW		0.05		0.05		0.06		0.07		0.10	ns/pF

1. For dual-module macros, use t_{PD1} + t_{RD1} + t_{PDn}, t_{CO} + t_{RD1} + t_{PDn}, or t_{PD1} + t_{RD1} + t_{SUD}, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
4. Set-up and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.
5. Delays based on 35 pF loading.

Table 40 • **A42MX16 Timing Characteristics (Nominal 5.0 V Operation) (Worst-Case Commercial Conditions, VCCA = 4.75 V, T_J = 70°C)**

Parameter / Description		–3 Speed Min.	–3 Speed Max.	–2 Speed Min.	–2 Speed Max.	–1 Speed Min.	–1 Speed Max.	Std Speed Min.	Std Speed Max.	–F Speed Min.	–F Speed Max.	Units
Logic Module Propagation Delays[1]												
t_{PD1}	Single Module		1.4		1.5		1.7		2.0		2.8	ns
t_{CO}	Sequential Clock-to-Q		1.4		1.6		1.8		2.1		3.0	ns
t_{GO}	Latch G-to-Q		1.4		1.5		1.7		2.0		2.8	ns
t_{RS}	Flip-Flop (Latch) Reset-to-Q		1.6		1.7		2.0		2.3		3.3	ns
Logic Module Predicted Routing Delays[2]												
t_{RD1}	FO = 1 Routing Delay		0.8		0.9		1.0		1.2		1.6	ns
t_{RD2}	FO = 2 Routing Delay		1.0		1.2		1.3		1.5		2.1	ns

Figure 42 •   **PQ144**
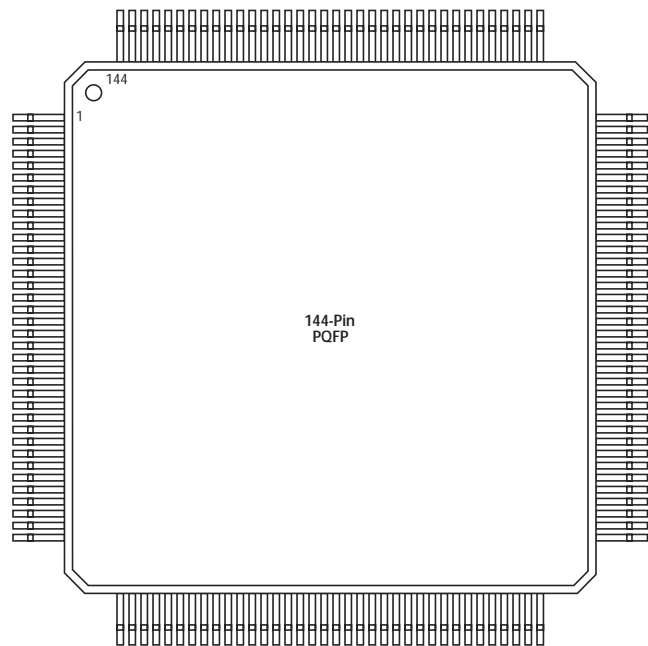
Table 51 •   **PQ144**

PQ144	
Pin Number	**A42MX09 Function**
1	I/O
2	MODE
3	I/O
4	I/O
5	I/O

Table 51 • **PQ144**

PQ144	
Pin Number	**A42MX09 Function**
43	I/O
44	GNDQ
45	GNDI
46	NC
47	I/O
48	I/O
49	I/O
50	I/O
51	I/O
52	I/O
53	I/O
54	VCC
55	VCCI
56	NC
57	I/O
58	I/O
59	I/O
60	I/O
61	I/O
62	I/O
63	I/O
64	GND
65	GNDI
66	I/O
67	I/O
68	I/O
69	I/O
70	I/O
71	SDO
72	I/O
73	I/O
74	I/O
75	I/O
76	I/O
77	I/O
78	I/O
79	GNDQ

Table 52 • **PQ160**

PQ160

Pin Number	A42MX09 Function	A42MX16 Function	A42MX24 Function
95	I/O	I/O	I/O
96	I/O	I/O	WD, I/O
97	I/O	I/O	I/O
98	VCCA	VCCA	VCCA
99	GND	GND	GND
100	NC	I/O	I/O
101	I/O	I/O	I/O
102	I/O	I/O	I/O
103	NC	I/O	I/O
104	I/O	I/O	I/O
105	I/O	I/O	I/O
106	I/O	I/O	WD, I/O
107	I/O	I/O	WD, I/O
108	I/O	I/O	I/O
109	GND	GND	GND
110	NC	I/O	I/O
111	I/O	I/O	WD, I/O
112	I/O	I/O	WD, I/O
113	I/O	I/O	I/O
114	NC	VCCI	VCCI
115	I/O	I/O	WD, I/O
116	NC	I/O	WD, I/O
117	I/O	I/O	I/O
118	I/O	I/O	TDI, I/O
119	I/O	I/O	TMS, I/O
120	GND	GND	GND
121	I/O	I/O	I/O
122	I/O	I/O	I/O
123	I/O	I/O	I/O
124	NC	I/O	I/O
125	GND	GND	GND
126	I/O	I/O	I/O
127	I/O	I/O	I/O
128	I/O	I/O	I/O
129	NC	I/O	I/O
130	GND	GND	GND
131	I/O	I/O	I/O

Table 54 • **PQ240**

PQ240

Pin Number	A42MX36 Function
237	GND
238	MODE
239	VCCA
240	GND

Figure 46 • **VQ80**
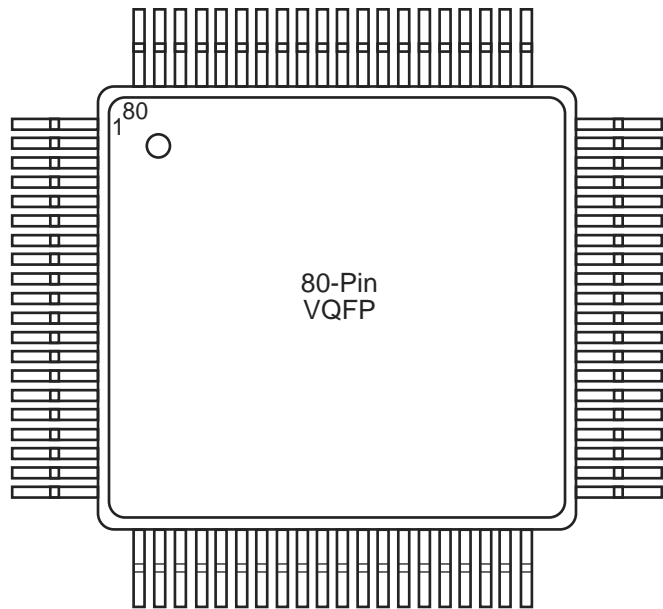
80-Pin
VQFP

Table 55 • **VQ80**

VQ80

Pin Number	A40MX02 Function	A40MX04 Function
1	I/O	I/O
2	NC	I/O
3	NC	I/O
4	NC	I/O
5	I/O	I/O
6	I/O	I/O
7	GND	GND
8	I/O	I/O
9	I/O	I/O
10	I/O	I/O
11	I/O	I/O
12	I/O	I/O

Table 55 • **VQ80**

VQ80

Pin Number	A40MX02 Function	A40MX04 Function
49	I/O	I/O
50	CLK, I/O	CLK, I/O
51	I/O	I/O
52	MODE	MODE
53	VCC	VCC
54	NC	I/O
55	NC	I/O
56	NC	I/O
57	SDI, I/O	SDI, I/O
58	DCLK, I/O	DCLK, I/O
59	PRA, I/O	PRA, I/O
60	NC	NC
61	PRB, I/O	PRB, I/O
62	I/O	I/O
63	I/O	I/O
64	I/O	I/O
65	I/O	I/O
66	I/O	I/O
67	I/O	I/O
68	GND	GND
69	I/O	I/O
70	I/O	I/O
71	I/O	I/O
72	I/O	I/O
73	I/O	I/O
74	VCC	**VCC**
75	I/O	I/O
76	I/O	I/O
77	I/O	I/O
78	I/O	I/O
79	I/O	I/O
80	I/O	I/O

Table 58 • **CQ208**

CQ208	
Pin Number	**A42MX36 Function**
1	GND
2	VCCA
3	MODE
4	I/O
5	I/O
6	I/O
7	I/O
8	I/O
9	I/O
10	I/O
11	I/O
12	I/O
13	I/O
14	I/O
15	I/O
16	I/O
17	VCCA
18	I/O
19	I/O
20	I/O
21	I/O
22	GND
23	I/O
24	I/O
25	I/O
26	I/O
27	GND
28	VCCI
29	VCCA
30	I/O
31	I/O
32	VCCA
33	I/O
34	I/O
35	I/O
36	I/O

Table 59 • **CQ256**

CQ256	
Pin Number	**A42MX36 Function**
96	VCCA
97	GND
98	GND
99	I/O
100	I/O
101	I/O
102	I/O
103	I/O
104	I/O
105	WD, I/O
106	WD, I/O
107	I/O
108	I/O
109	WD, I/O
110	WD, I/O
111	I/O
112	QCLKA, I/O
113	I/O
114	GND
115	I/O
116	I/O
117	I/O
118	I/O
119	VCCI
120	I/O
121	WD, I/O
122	WD, I/O
123	I/O
124	I/O
125	I/O
126	I/O
127	GND
128	NC
129	NC
130	NC
131	GND
132	I/O

Table 59 • **CQ256**

CQ256	
Pin Number	**A42MX36 Function**
244	WD, I/O
245	I/O
246	I/O
247	I/O
248	VCCI
249	I/O
250	WD, I/O
251	WD, I/O
252	I/O
253	SDI, I/O
254	I/O
255	GND
256	NC

Figure 51 • **BG272**
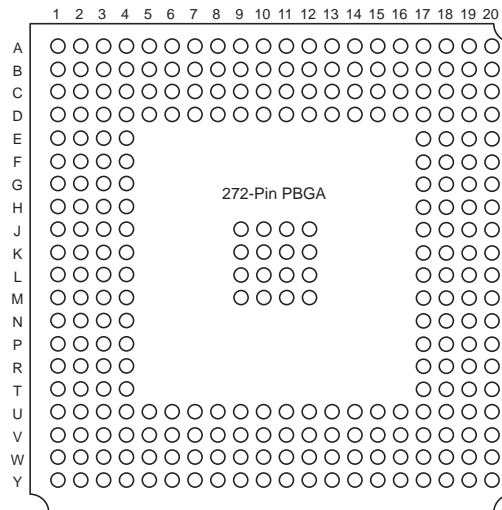
Table 60 • **BG272**

BG272	
Pin Number	**A42MX36 Function**
A1	GND
A2	GND
A3	I/O
A4	WD, I/O
A5	I/O

Table 60 •   **BG272**

BG272	
Pin Number	**A42MX36 Function**
Y13	I/O
Y14	I/O
Y15	I/O
Y16	I/O
Y17	I/O
Y18	WD, I/O
Y19	GND
Y20	GND

Figure 52 •   **PG132**

● Orientation Pin
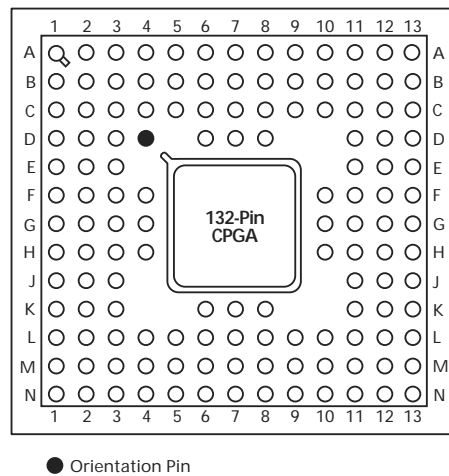
Table 61 •   **PG132**

PG132	
Pin Number	**A42MX09 Function**
–	PMPOUT
B2	I/O
A1	MODE
B1	I/O
D3	I/O
C2	I/O
C1	I/O
D2	I/O
D1	I/O
E2	I/O
E1	I/O
F3	I/O