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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | - |
| Number of I/O | 57 |
| Number of Gates | 3000 |
| Voltage - Supply | 3V ~ 3.6V, 4.5V ~ 5.5V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Package / Case | 80-TQFP |
| Supplier Device Package | 80-VQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/a40mx02-vq80i |

**Microsemi Corporate Headquarters**
One Enterprise, Aliso Viejo,
CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Fax: +1 (949) 215-4996
Email: sales.support@microsemi.com
www.microsemi.com





## About Microsemi

Microsemi Corporation (Nasdaq: MSCC) offers a comprehensive portfolio of semiconductor and system solutions for aerospace & defense, communications, data center and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; enterprise storage and communication solutions, security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, California, and has approximately 4,800 employees globally. Learn more at www.microsemi.com.

5172136. 15.0 12/16

# 1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

## 1.1 Revision 15.0

The following is a summary of the changes in revision 15.0 of this document.

- Table 15, page 21 is edited to add the footnote, VIH(Min) is 2.4V for A42MX36 family. This applies only to VCCI of 5V and is not applicable to VCCI of 3.3V
- Table 22, page 25 is edited to add the footnote, VIH(Min) is 2.4V for A42MX36 family. This applies only to VCCI of 5V and is not applicable to VCCI of 3.3V
- Table 23, page 25 is edited to add the footnote, VIH(Min) is 2.4V for A42MX36 family. This applies only to VCCI of 5V and is not applicable to VCCI of 3.3V

## 1.2 Revision 14.0

The following is a summary of the changes in revision 14.0 of this document.

- Added CQFP package information for A42MX16 device in Product Profile, page 1 and Ceramic Device Resources, page 4 (SAR 79522).
- Added Military (M) and MIL-STD-883 Class B (B) grades for CPGA 132 Package and added Commercial (C), Military (M), and MIL-STD-883 Class B (B) grades for CQFP 172 Package in Temperature Grade Offerings, page 5 (SAR 79519)
- Changed Silicon Sculptor II to Silicon Sculptor in Programming, page 12 (SAR 38754)
- Added Figure 53, page 158 CQ172 package (SAR 79522).

## 1.3 Revision 13.0

The following is a summary of the changes in revision 13.0 of this document.

- Added Figure 42, page 97 PQ144 Package for A42MX09 device (SAR 69776)
- Added Figure 52, page 153 PQ132 Package for A42MX09 device (SAR 69776)

## 1.4 Revision 12.0

The following is a summary of the changes in revision 12.0 of this document.

- Added information on power-up behavior for A42MX24 and A42MX36 devices to the Power Supply, page 13 (SAR 42096
- Corrected the inadvertent mistake in the naming of the PL68 pin assignment table (SARs 48999, 49793)

## 1.5 Revision 11.0

The following is a summary of the changes in revision 11.0 of this document.

- The FuseLock logo and accompanying text was removed from the User Security, page 12. This marking is no longer used on Microsemi devices (PCN 0915)
- The Development Tool Support, page 19 was updated (SAR 38512)

## 1.6 Revision 10.0

The following is a summary of the changes in revision 10.0 of this document.

- Ordering Information, page 3 was updated to include lead-free package ordering codes (SAR 21968)
- The User Security, page 12 was revised to clarify that although no existing security measures can give an absolute guarantee, Microsemi FPGAs implement the best security available in the industry (SAR 34673)

### 3.8.1 3.3 V LVTTL Electrical Specifications

***Table 19 •*** **3.3V LVTTL Electrical Specifications**

| | | Commercial | | Commercial -F | | Industrial | | Military | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| VOH[1] | IOH = –4 mA | 2.15 | | 2.15 | | 2.4 | | 2.4 | | V |
| VOL[1] | IOL = 6 mA | | 0.4 | | 0.4 | | 0.48 | | 0.48 | V |
| VIL | | –0.3 | 0.8 | –0.3 | 0.8 | –0.3 | 0.8 | –0.3 | 0.8 | V |
| VIH (40MX) | | 2.0 | VCC + 0.3 | 2.0 | VCC + 0.3 | 2.0 | VCC + 0.3 | 2.0 | VCC + 0.3 | V |
| VIH (42MX) | | 2.0 | VCCI + 0.3 | 2.0 | VCCI + 0.3 | 2.0 | VCCI + 0.3 | 2.0 | VCCI + 0.3 | V |
| IIL | | | –10 | | –10 | | –10 | | –10 | µA |
| IIH | | | –10 | | –10 | | –10 | | –10 | µA |
| Input Transition Time, $T_R$ and $T_F$ | | | 500 | | 500 | | 500 | | 500 | ns |
| $C_{IO}$ I/O Capacitance | | | 10 | | 10 | | 10 | | 10 | pF |
| Standby Current, ICC[2] | A40MX02, A40MX04 | | 3 | | 25 | | 10 | | 25 | mA |
| | A42MX09 | | 5 | | 25 | | 25 | | 25 | mA |
| | A42MX16 | | 6 | | 25 | | 25 | | 25 | mA |
| | A42MX24, A42MX36 | | 15 | | 25 | | 25 | | 25 | mA |
| Low-Power Mode Standby Current | 42MX devices only | | 0.5 | | ICC - 5.0 | | ICC - 5.0 | | ICC - 5.0 | mA |
| IIO, I/O source sink current | Can be derived from the *IBIS model* (http://www.microsemi.com/soc/techdocs/models/ibis.html) | | | | | | | | | |

1. Only one output tested at a time. VCC/VCCI = min.
2. All outputs unloaded. All inputs = VCC/VCCI or GND.

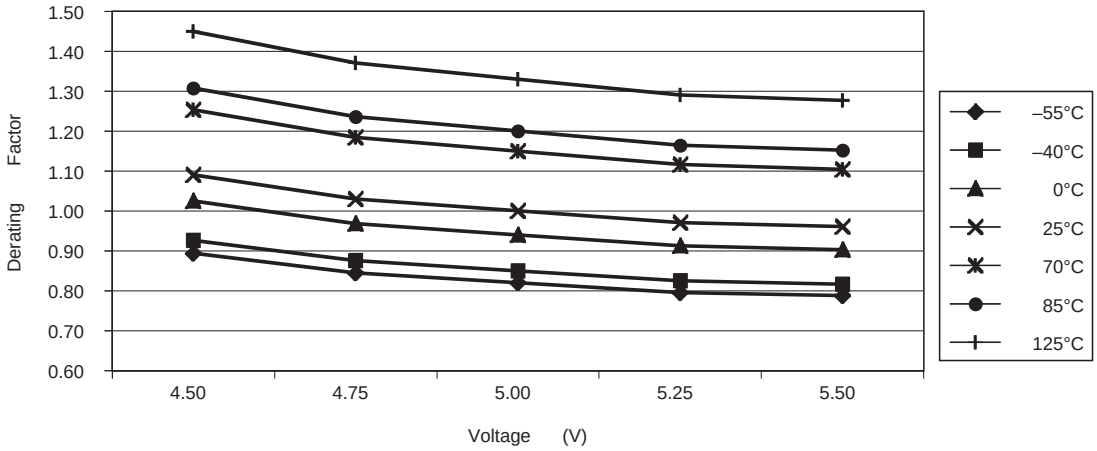
## 3.9 Mixed 5.0 V / 3.3 V Operating Conditions (for 42MX Devices Only)

***Table 20 •*** **Absolute Maximum Ratings***

| **Symbol** | **Parameter** | **Limits** | **Units** |
|---|---|---|---|
| VCCI | DC Supply Voltage for I/Os | –0.5 to +7.0 | V |
| VCCA | DC Supply Voltage for Array | –0.5 to +7.0 | V |
| VI | Input Voltage | –0.5 to VCCA +0.5 | V |
| VO | Output Voltage | –0.5 to VCCI + 0.5 | V |
| $t_{STG}$ | Storage Temperature | –65 to +150 | °C |

**Note:** *Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device

***Figure 35 •*** **40MX Junction Temperature and Voltage Derating Curves (Normalized to TJ = 25°C, VCC = 5.0 V)**

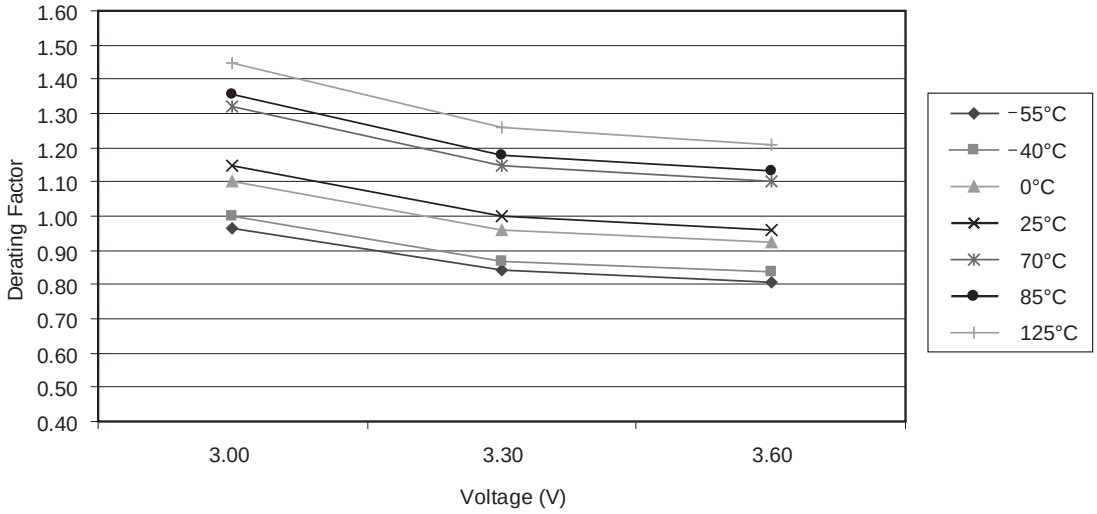



**Note:** This derating factor applies to all routing and propagation delays

***Table 30 •*** **42MX Temperature and Voltage Derating Factors(Normalized to TJ = 25°C, VCCA = 3.3 V)**

| | Temperature | | | | | | |
|---|---|---|---|---|---|---|---|
| **42MX Voltage** | **–55°C** | **–40°C** | **0°C** | **25°C** | **70°C** | **85°C** | **125°C** |
| 3.00 | 0.97 | 1.00 | 1.10 | 1.15 | 1.32 | 1.36 | 1.45 |
| 3.30 | 0.84 | 0.87 | 0.96 | 1.00 | 1.15 | 1.18 | 1.26 |
| 3.60 | 0.81 | 0.84 | 0.92 | 0.96 | 1.10 | 1.13 | 1.21 |

***Figure 36 •*** **42MX Junction Temperature and Voltage Derating Curves (Normalized to TJ = 25°C, VCCA = 3.3 V)**




**Note:** This derating factor applies to all routing and propagation delays

***Table 31 •*** **40MX Temperature and Voltage Derating Factors (Normalized to TJ = 25°C, VCC = 3.3 V)**

| | Temperature | | | | | | |
|---|---|---|---|---|---|---|---|
| **40MX Voltage** | **–55°C** | **–40°C** | **0°C** | **25°C** | **70°C** | **85°C** | **125°C** |
| 3.00 | 1.08 | 1.12 | 1.21 | 1.26 | 1.50 | 1.64 | 2.00 |
| 3.30 | 0.86 | 0.89 | 0.96 | 1.00 | 1.19 | 1.30 | 1.59 |

**Table 39 • A42MX09 Timing Characteristics (Nominal 3.3 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 3.0 V, $T_J$ = 70°C)**

| Parameter / Description | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **TTL Output Module Timing[5]** | | | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad HIGH | | 3.4 | | 3.8 | | 4.3 | | 5.1 | | 7.1 | ns |
| $t_{DHL}$ | Data-to-Pad LOW | | 4.0 | | 4.5 | | 5.1 | | 6.1 | | 8.3 | ns |
| $t_{ENZH}$ | Enable Pad Z to HIGH | | 3.7 | | 4.1 | | 4.6 | | 5.5 | | 7.6 | ns |
| $t_{ENZL}$ | Enable Pad Z to LOW | | 4.1 | | 4.5 | | 5.1 | | 6.1 | | 8.5 | ns |
| $t_{ENHZ}$ | Enable Pad HIGH to Z | | 6.9 | | 7.6 | | 8.6 | | 10.2 | | 14.2 | ns |
| $t_{ENLZ}$ | Enable Pad LOW to Z | | 7.5 | | 8.3 | | 9.4 | | 11.1 | | 15.5 | ns |
| $t_{GLH}$ | G-to-Pad HIGH | | 5.8 | | 6.5 | | 7.3 | | 8.6 | | 12.0 | ns |
| $t_{GHL}$ | G-to-Pad LOW | | 5.8 | | 6.5 | | 7.3 | | 8.6 | | 12.0 | ns |
| $t_{LSU}$ | I/O Latch Set-Up | 0.7 | | 0.8 | | 0.9 | | 1.0 | | 1.4 | | ns |
| $t_{LH}$ | I/O Latch Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{LCO}$ | I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading | | 8.7 | | 9.7 | | 10.9 | | 12.9 | | 18.0 | ns |
| $t_{ACO}$ | Array Clock-to-Out (Pad-to-Pad),64 Clock Loading | | 12.2 | | 13.5 | | 15.4 | | 18.1 | | 25.3 | ns |
| $d_{TLH}$ | Capacity Loading, LOW to HIGH | | 0.00 | | 0.00 | | 0.00 | | 0.10 | | 0.01 | ns/pF |
| $d_{THL}$ | Capacity Loading, HIGH to LOW | | 0.09 | | 0.10 | | 0.10 | | 0.10 | | 0.10 | ns/pF |

**Table 40 • A42MX16 Timing Characteristics (Nominal 5.0 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 4.75 V, $T_J$ = 70°C)**

| Parameter / Description | | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{PWL}$ | Minimum Pulse Width LOW | FO = 32 | 3.2 | | 3.5 | | 4.0 | | 4.7 | | 6.6 | | ns |
| | | FO = 384 | 3.7 | | 4.1 | | 4.6 | | 5.4 | | 7.6 | | ns |
| $t_{CKSW}$ | Maximum Skew | FO = 32 | | 0.3 | | 0.4 | | 0.4 | | 0.5 | | 0.7 | ns |
| | | FO = 384 | | 0.3 | | 0.4 | | 0.4 | | 0.5 | | 0.7 | ns |
| $t_{SUEXT}$ | Input Latch External Set-Up | FO = 32 | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| | | FO = 384 | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{HEXT}$ | Input Latch External Hold | FO = 32 | 2.8 | | 3.1 | | 5.5 | | 4.1 | | 5.7 | | ns |
| | | FO = 384 | 3.2 | | 3.5 | | 4.0 | | 4.7 | | 6.6 | | ns |
| $t_P$ | Minimum Period | FO = 32 | 4.2 | | 4.67 | | 5.1 | | 5.8 | | 9.7 | | ns |
| | | FO = 384 | 4.6 | | 5.1 | | 5.6 | | 6.4 | | 10.7 | | ns |
| $f_{MAX}$ | Maximum Frequency | FO = 32 | | 237 | | 215 | | 198 | | 172 | | 103 | MHz |
| | | FO = 384 | | 215 | | 195 | | 179 | | 156 | | 94 | MHz |

***Table 42 •*** **A42MX24 Timing Characteristics (Nominal 5.0 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 4.75 V, $T_J$ = 70°C)**

| | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter / Description** | | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| **TTL Output Module Timing[5]** | | | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad HIGH | | 2.4 | | 2.7 | | 3.1 | | 3.6 | | 5.1 | ns |
| $t_{DHL}$ | Data-to-Pad LOW | | 2.8 | | 3.2 | | 3.6 | | 4.2 | | 5.9 | ns |
| $t_{ENZH}$ | Enable Pad Z to HIGH | | 2.5 | | 2.8 | | 3.2 | | 3.8 | | 5.3 | ns |
| $t_{ENZL}$ | Enable Pad Z to LOW | | 2.8 | | 3.1 | | 3.5 | | 4.2 | | 5.9 | ns |
| $t_{ENHZ}$ | Enable Pad HIGH to Z | | 5.2 | | 5.7 | | 6.5 | | 7.6 | | 10.7 | ns |
| $t_{ENLZ}$ | Enable Pad LOW to Z | | 4.8 | | 5.3 | | 6.0 | | 7.1 | | 9.9 | ns |
| $t_{GLH}$ | G-to-Pad HIGH | | 2.9 | | 3.2 | | 3.6 | | 4.3 | | 6.0 | ns |
| $t_{GHL}$ | G-to-Pad LOW | | 2.9 | | 3.2 | | 3.6 | | 4.3 | | 6.0 | ns |
| $t_{LSU}$ | I/O Latch Output Set-Up | 0.5 | | 0.5 | | 0.6 | | 0.7 | | 1.0 | | ns |
| $t_{LH}$ | I/O Latch Output Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{LCO}$ | I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O | | 5.6 | | 6.1 | | 6.9 | | 8.1 | | 11.4 | ns |
| $t_{ACO}$ | Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O | | 10.6 | | 11.8 | | 13.4 | | 15.7 | | 22.0 | ns |
| $d_{TLH}$ | Capacitive Loading, LOW to HIGH | | 0.04 | | 0.04 | | 0.04 | | 0.05 | | 0.07 | ns/pF |
| $d_{THL}$ | Capacitive Loading, HIGH to LOW | | 0.03 | | 0.03 | | 0.03 | | 0.04 | | 0.06 | ns/pF |

**Table 43 • A42MX24 Timing Characteristics (Nominal 3.3 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 3.0 V, $T_J$ = 70°C)**

| Parameter / Description | | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Input Module Predicted Routing Delays[2]** | | | | | | | | | | | | | |
| $t_{IRD1}$ | FO = 1 Routing Delay | | | 2.6 | | 2.9 | | 3.2 | | 3.8 | | 5.3 | ns |
| $t_{IRD2}$ | FO = 2 Routing Delay | | | 2.9 | | 3.2 | | 3.6 | | 4.3 | | 6.0 | ns |
| $t_{IRD3}$ | FO = 3 Routing Delay | | | 3.2 | | 3.6 | | 4.0 | | 4.8 | | 6.6 | ns |
| $t_{IRD4}$ | FO = 4 Routing Delay | | | 3.5 | | 3.9 | | 4.4 | | 5.2 | | 7.3 | ns |
| $t_{IRD8}$ | FO = 8 Routing Delay | | | 4.8 | | 5.3 | | 6.1 | | 7.1 | | 10.0 | ns |
| **Global Clock Network** | | | | | | | | | | | | | |
| $t_{CKH}$ | Input LOW to HIGH | FO = 32 | | 4.4 | | 4.8 | | 5.5 | | 6.5 | | 9.1 | ns |
| | | FO = 486 | | 4.8 | | 5.3 | | 6.0 | | 7.1 | | 10.0 | ns |
| $t_{CKL}$ | Input HIGH to LOW | FO = 32 | | 5.1 | | 5.7 | | 6.4 | | 7.6 | | 10.6 | ns |
| | | FO = 486 | | 6.0 | | 6.6 | | 7.5 | | 8.8 | | 12.4 | ns |
| $t_{PWH}$ | Minimum Pulse Width HIGH | FO = 32 | 3.0 | | 3.3 | | 3.8 | | 4.5 | | 6.3 | | ns |
| | | FO = 486 | 3.3 | | 3.7 | | 4.2 | | 4.9 | | 6.9 | | ns |
| $t_{PWL}$ | Minimum Pulse Width LOW | FO = 32 | 3.0 | | 3.4 | | 3.8 | | 4.5 | | 6.3 | | ns |
| | | FO = 486 | 3.3 | | 3.7 | | 4.2 | | 4.9 | | 6.9 | | ns |
| $t_{CKSW}$ | Maximum Skew | FO = 32 | | 0.8 | | 0.8 | | 1.0 | | 1.1 | | 1.6 | ns |
| | | FO = 486 | | 0.8 | | 0.8 | | 1.0 | | 1.1 | | 1.6 | ns |
| $t_{SUEXT}$ | Input Latch External Set-Up | FO = 32 | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| | | FO = 486 | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| **TTL Output Module Timing[5]** | | | | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad HIGH | | | 3.4 | | 3.8 | | 4.3 | | 5.0 | | 7.1 | ns |
| $t_{DHL}$ | Data-to-Pad LOW | | | 4.0 | | 4.4 | | 5.0 | | 5.9 | | 8.3 | ns |
| $t_{ENZH}$ | Enable Pad Z to HIGH | | | 3.6 | | 4.0 | | 4.5 | | 5.3 | | 7.4 | ns |
| $t_{ENZL}$ | Enable Pad Z to LOW | | | 3.9 | | 4.4 | | 5.0 | | 5.8 | | 8.2 | ns |
| $t_{ENHZ}$ | Enable Pad HIGH to Z | | | 7.2 | | 8.0 | | 9.1 | | 10.7 | | 14.9 | ns |
| $t_{ENLZ}$ | Enable Pad LOW to Z | | | 6.7 | | 7.5 | | 8.5 | | 9.9 | | 13.9 | ns |
| $t_{GLH}$ | G-to-Pad HIGH | | | 4.8 | | 5.3 | | 6.0 | | 7.2 | | 10.0 | ns |
| $t_{GHL}$ | G-to-Pad LOW | | | 4.8 | | 5.3 | | 6.0 | | 7.2 | | 10.0 | ns |
| $t_{LSU}$ | I/O Latch Output Set-Up | | 0.7 | | 0.7 | | 0.8 | | 1.0 | | 1.4 | | ns |

**Table 43 • A42MX24 Timing Characteristics (Nominal 3.3 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 3.0 V, $T_J$ = 70°C)**

| Parameter / Description | | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **TTL Output Module Timing[5] (continued)** | | | | | | | | | | | | | |
| $t_{LH}$ | I/O Latch Output Hold | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{LCO}$ | I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O | | | 7.7 | | 8.5 | | 9.6 | | 11.3 | | 15.9 | ns |
| $t_{ACO}$ | Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O | | | 14.8 | | 16.5 | | 18.7 | | 22.0 | | 30.8 | ns |
| $d_{TLH}$ | Capacitive Loading, LOW to HIGH | | | 0.05 | | 0.05 | | 0.06 | | 0.07 | | 0.10 | ns/pF |
| $d_{THL}$ | Capacitive Loading, HIGH to LOW | | | 0.04 | | 0.04 | | 0.05 | | 0.06 | | 0.08 | ns/pF |
| **CMOS Output Module Timing[5]** | | | | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad HIGH | | | 4.8 | | 5.3 | | 5.5 | | 6.4 | | 9.0 | ns |
| $t_{DHL}$ | Data-to-Pad LOW | | | 3.5 | | 3.9 | | 4.1 | | 4.9 | | 6.8 | ns |
| $t_{ENZH}$ | Enable Pad Z to HIGH | | | 3.6 | | 4.0 | | 4.5 | | 5.3 | | 7.4 | ns |
| $t_{ENZL}$ | Enable Pad Z to LOW | | | 3.4 | | 4.0 | | 5.0 | | 5.8 | | 8.2 | ns |
| $t_{ENHZ}$ | Enable Pad HIGH to Z | | | 7.2 | | 8.0 | | 9.0 | | 10.7 | | 14.9 | ns |
| $t_{ENLZ}$ | Enable Pad LOW to Z | | | 6.7 | | 7.5 | | 8.5 | | 9.9 | | 13.9 | ns |
| $t_{GLH}$ | G-to-Pad HIGH | | | 6.8 | | 7.6 | | 8.6 | | 10.1 | | 14.2 | ns |
| $t_{GHL}$ | G-to-Pad LOW | | | 6.8 | | 7.6 | | 8.6 | | 10.1 | | 14.2 | ns |
| $t_{LSU}$ | I/O Latch Set-Up | | 0.7 | | 0.7 | | 0.8 | | 1.0 | | 1.4 | | ns |
| $t_{LH}$ | I/O Latch Hold | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{LCO}$ | I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O | | | 7.7 | | 8.5 | | 9.6 | | 11.3 | | 15.9 | ns |
| $t_{ACO}$ | Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O | | | 14.8 | | 16.5 | | 18.7 | | 22.0 | | 30.8 | ns |
| $d_{TLH}$ | Capacitive Loading, LOW to HIGH | | | 0.05 | | 0.05 | | 0.06 | | 0.07 | | 0.10 | ns/pF |
| $d_{THL}$ | Capacitive Loading, HIGH to LOW | | | 0.04 | | 0.04 | | 0.05 | | 0.06 | | 0.08 | ns/pF |
| $t_{HEXT}$ | Input Latch External Hold | FO = 32 | 3.9 | | 4.3 | | 4.9 | | 5.7 | | 8.1 | | ns |
| | | FO = 486 | 4.6 | | 5.2 | | 5.8 | | 6.9 | | 9.6 | | ns |
| $t_P$ | Minimum Period ($1/f_{MAX}$) | FO = 32 | 7.8 | | 8.7 | | 9.5 | | 10.8 | | 18.2 | | ns |
| | | FO = 486 | 8.6 | | 9.5 | | 10.4 | | 11.9 | | 19.9 | | ns |

1. For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
4. Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.
5. Delays based on 35 pF loading.

***Table 44 •*** **A42MX36 Timing Characteristics (Nominal 5.0 V Operation)(Worst-Case Commercial Conditions, VCCA = 4.75 V, $T_J$ = 70°C)**

| Parameter / Description | | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{SUEXT}$ | Input Latch External Set-Up | FO = 32 | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| | | FO = 635 | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{HEXT}$ | Input Latch External Hold | FO = 32 | 2.8 | | 3.2 | | 3.6 | | 4.2 | | 5.9 | | ns |
| | | FO = 635 | 3.3 | | 3.7 | | 4.2 | | 4.9 | | 6.9 | | ns |
| $t_P$ | Minimum Period ($1/f_{MAX}$) | FO = 32 | 5.5 | | 6.1 | | 6.6 | | 7.6 | | 12.7 | | ns |
| | | FO = 635 | 6.0 | | 6.6 | | 7.2 | | 8.3 | | 13.8 | | ns |
| $f_{MAX}$ | Maximum Datapath Frequency | FO = 32 | | 180 | | 164 | | 151 | | 131 | | 79 | MHz |
| | | FO = 635 | | 166 | | 151 | | 139 | | 121 | | 73 | MHz |
| **TTL Output Module Timing[5]** | | | | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad HIGH | | | 2.6 | | 2.8 | | 3.2 | | 3.8 | | 5.3 | ns |
| $t_{DHL}$ | Data-to-Pad LOW | | | 3.0 | | 3.3 | | 3.7 | | 4.4 | | 6.2 | ns |
| $t_{ENZH}$ | Enable Pad Z to HIGH | | | 2.7 | | 3.0 | | 3.3 | | 3.9 | | 5.5 | ns |
| $t_{ENZL}$ | Enable Pad Z to LOW | | | 3.0 | | 3.3 | | 3.7 | | 4.3 | | 6.1 | ns |
| $t_{ENHZ}$ | Enable Pad HIGH to Z | | | 5.3 | | 5.8 | | 6.6 | | 7.8 | | 10.9 | ns |

***Table 45 •*** **A42MX36 Timing Characteristics (Nominal 3.3 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 3.0 V, $T_J$ = 70°C)**

| Parameter / Description | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Units |
| $t_{ACO}$ | Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O | | 10.9 | | 12.1 | | 13.7 | | 16.1 | | 22.5 | ns |
| $d_{TLH}$ | Capacitive Loading, LOW to HIGH | | 0.10 | | 0.11 | | 0.12 | | 0.14 | | 0.20 | ns/pF |
| $d_{THL}$ | Capacitive Loading, HIGH to LOW | | 0.10 | | 0.11 | | 0.12 | | 0.14 | | 0.20 | ns/pF |
| **CMOS Output Module Timing[5]** | | | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad HIGH | | 4.9 | | 5.5 | | 6.2 | | 7.3 | | 10.3 | ns |
| $t_{DHL}$ | Data-to-Pad LOW | | 3.4 | | 3.8 | | 4.3 | | 5.1 | | 7.1 | ns |
| $t_{ENZH}$ | Enable Pad Z to HIGH | | 3.7 | | 4.1 | | 4.7 | | 5.5 | | 7.7 | ns |
| $t_{ENZL}$ | Enable Pad Z to LOW | | 4.1 | | 4.6 | | 5.2 | | 6.1 | | 8.5 | ns |
| $t_{ENHZ}$ | Enable Pad HIGH to Z | | 7.4 | | 8.2 | | 9.3 | | 10.9 | | 15.3 | ns |
| $t_{ENLZ}$ | Enable Pad LOW to Z | | 6.9 | | 7.6 | | 8.7 | | 10.2 | | 14.3 | ns |
| $t_{GLH}$ | G-to-Pad HIGH | | 7.0 | | 7.8 | | 8.9 | | 10.4 | | 14.6 | ns |
| $t_{GHL}$ | G-to-Pad LOW | | 7.0 | | 7.8 | | 8.9 | | 10.4 | | 14.6 | ns |
| $t_{LSU}$ | I/O Latch Set-Up | 0.7 | | 0.7 | | 0.8 | | 1.0 | | 1.4 | | ns |
| $t_{LH}$ | I/O Latch Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{LCO}$ | I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O | | 7.9 | | 8.8 | | 10.0 | | 11.8 | | 16.5 | ns |

1. For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
4. *Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*
5. Delays based on 35 pF loading.

## 3.12 Pin Descriptions

This section lists the pin descriptions for 40MX and 42MX series FPGAs.

**CLK/A/B, I/O Global Clock**

Clock inputs for clock distribution networks. CLK is for 40MX while CLKA and CLKB are for 42MX devices. The clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

**DCLK, I/ODiagnostic Clock**

Clock input for diagnostic probe and device programming. DCLK is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

**GND, Ground**

Input LOW supply voltage.

**I/O, Input/Output**

Input, output, tristate or bidirectional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. Unused I/Os pins are configured by the Designer software as shown in Table 46, page 84.

***Table 46 •*** **Configuration of Unused I/Os**

| Device | Configuration |
|---|---|
| A40MX02, A40MX04 | Pulled LOW |
| A42MX09, A42MX16 | Pulled LOW |
| A42MX24, A42MX36 | Tristated |

In all cases, it is recommended to tie all unused MX I/O pins to LOW on the board. This applies to all dual-purpose pins when configured as I/Os as well.

**LP, Low Power Mode**

Controls the low power mode of all 42MX devices. The device is placed in the low power mode by connecting the LP pin to logic HIGH. In low power mode, all I/Os are tristated, all input buffers are turned OFF, and the core of the device is turned OFF. To exit the low power mode, the LP pin must be set LOW. The device enters the low power mode 800 ns after the LP pin is driven to a logic HIGH. It will resume normal operation in 200 µs after the LP pin is driven to a logic LOW.

**MODE, Mode**

Controls the use of multifunction pins (DCLK, PRA, PRB, SDI, TDO). The MODE pin is held HIGH to provide verification capability. The MODE pin should be terminated to GND through a 10kΩ resistor so that the MODE pin can be pulled HIGH when required.

**NC, No Connection**

This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

**PRA, I/O**

**PRB, I/OProbe A/B**

The Probe pin is used to output data from any user-defined design node within the device. Each diagnostic pin can be used in conjunction with the other probe pin to allow real-time diagnostic output of any signal path within the device. The Probe pin can be used as a user-defined I/O when verification has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. The Probe pin is accessible when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

**QCLKA/B/C/D, I/O Quadrant Clock**

Quadrant clock inputs for A42MX36 devices. When not used as a register control signal, these pins can function as user I/Os.

**SDI, I/OSerial Data Input**

Serial data input for diagnostic probe and device programming. SDI is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

**SDO, I/OSerial Data Output**

Serial data output for diagnostic probe and device programming. SDO is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW. SDO is available for 42MX devices only.

When Silicon Explorer II is being used, SDO will act as an output while the "checksum" command is run. It will return to user I/O when "checksum" is complete.

**TCK, I/O Test Clock**

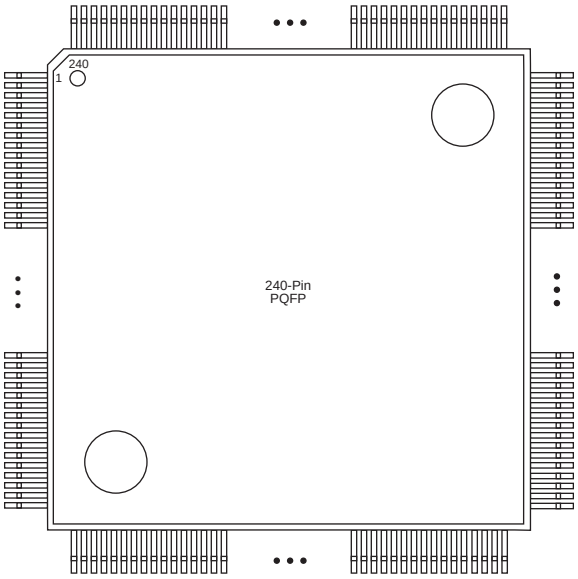
***Table 50 •*** **PQ 100**

| **PQ100** | | | | |
|---|---|---|---|---|
| **Pin Number** | **A40MX02 Function** | **A40MX04 Function** | **A42MX09 Function** | **A42MX16 Function** |
| 56 | VCC | VCC | I/O | I/O |
| 57 | I/O | I/O | GND | GND |
| 58 | I/O | I/O | I/O | I/O |
| 59 | I/O | I/O | I/O | I/O |
| 60 | I/O | I/O | I/O | I/O |
| 61 | I/O | I/O | I/O | I/O |
| 62 | I/O | I/O | I/O | I/O |
| 63 | GND | GND | I/O | I/O |
| 64 | I/O | I/O | LP | LP |
| 65 | I/O | I/O | VCCA | VCCA |
| 66 | I/O | I/O | VCCI | VCCI |
| 67 | I/O | I/O | VCCA | VCCA |
| 68 | I/O | I/O | I/O | I/O |
| 69 | VCC | VCC | I/O | I/O |
| 70 | I/O | I/O | I/O | I/O |
| 71 | I/O | I/O | I/O | I/O |
| 72 | I/O | I/O | GND | GND |
| 73 | I/O | I/O | I/O | I/O |
| 74 | I/O | I/O | I/O | I/O |
| 75 | I/O | I/O | I/O | I/O |
| 76 | I/O | I/O | I/O | I/O |
| 77 | NC | NC | I/O | I/O |
| 78 | NC | NC | I/O | I/O |
| 79 | NC | NC | SDI, I/O | SDI, I/O |
| 80 | NC | I/O | I/O | I/O |
| 81 | NC | I/O | I/O | I/O |
| 82 | NC | I/O | I/O | I/O |
| 83 | I/O | I/O | I/O | I/O |
| 84 | I/O | I/O | GND | GND |
| 85 | I/O | I/O | I/O | I/O |
| 86 | GND | GND | I/O | I/O |
| 87 | GND | GND | PRA, I/O | PRA, I/O |
| 88 | I/O | I/O | I/O | I/O |
| 89 | I/O | I/O | CLKA, I/O | CLKA, I/O |
| 90 | CLK, I/O | CLK, I/O | VCCA | VCCA |
| 91 | I/O | I/O | I/O | I/O |
| 92 | MODE | MODE | CLKB, I/O | CLKB, I/O |

***Table 53 •*** **PQ208**

| PQ208 | | | |
|---|---|---|---|
| **Pin Number** | **A42MX16 Function** | **A42MX24 Function** | **A42MX36 Function** |
| 206 | I/O | I/O | I/O |
| 207 | DCLK, I/O | DCLK, I/O | DCLK, I/O |
| 208 | I/O | I/O | I/O |

***Figure 45 •*** **PQ240**




**Note:** This figure shows the 240-Pin PQFP Package top view.

***Table 54 •*** **PQ240**

| PQ240 | |
|---|---|
| **Pin Number** | **A42MX36 Function** |
| 1 | I/O |
| 2 | DCLK, I/O |
| 3 | I/O |
| 4 | I/O |
| 5 | I/O |
| 6 | WD, I/O |
| 7 | WD, I/O |
| 8 | VCCI |
| 9 | I/O |
| 10 | I/O |
| 11 | I/O |
| 12 | I/O |
| 13 | I/O |
| 14 | I/O |

***Table 55 •*** **VQ80**

| **VQ80** | | |
|---|---|---|
| **Pin Number** | **A40MX02 Function** | **A40MX04 Function** |
| 13 | VCC | VCC |
| 14 | I/O | I/O |
| 15 | I/O | I/O |
| 16 | I/O | I/O |
| 17 | NC | I/O |
| 18 | NC | I/O |
| 19 | NC | I/O |
| 20 | VCC | VCC |
| 21 | I/O | I/O |
| 22 | I/O | I/O |
| 23 | I/O | I/O |
| 24 | I/O | I/O |
| 25 | I/O | I/O |
| 26 | I/O | I/O |
| 27 | GND | GND |
| 28 | I/O | I/O |
| 29 | I/O | I/O |
| 30 | I/O | I/O |
| 31 | I/O | I/O |
| 32 | I/O | I/O |
| 33 | VCC | VCC |
| 34 | I/O | I/O |
| 35 | I/O | I/O |
| 36 | I/O | I/O |
| 37 | I/O | I/O |
| 38 | I/O | I/O |
| 39 | I/O | I/O |
| 40 | I/O | I/O |
| 41 | NC | I/O |
| 42 | NC | I/O |
| 43 | NC | I/O |
| 44 | I/O | I/O |
| 45 | I/O | I/O |
| 46 | I/O | I/O |
| 47 | GND | GND |
| 48 | I/O | I/O |

***Table 56 •*** **VQ100**

| **VQ100** | | |
|---|---|---|
| **Pin Number** | **A42MX09 Function** | **A42MX16 Function** |
| 21 | I/O | I/O |
| 22 | I/O | I/O |
| 23 | I/O | I/O |
| 24 | I/O | I/O |
| 25 | I/O | I/O |
| 26 | I/O | I/O |
| 27 | I/O | I/O |
| 28 | I/O | I/O |
| 29 | I/O | I/O |
| 30 | I/O | I/O |
| 31 | I/O | I/O |
| 32 | GND | GND |
| 33 | I/O | I/O |
| 34 | I/O | I/O |
| 35 | I/O | I/O |
| 36 | I/O | I/O |
| 37 | I/O | I/O |
| 38 | VCCA | VCCA |
| 39 | I/O | I/O |
| 40 | I/O | I/O |
| 41 | I/O | I/O |
| 42 | I/O | I/O |
| 43 | I/O | I/O |
| 44 | GND | GND |
| 45 | I/O | I/O |
| 46 | I/O | I/O |
| 47 | I/O | I/O |
| 48 | I/O | I/O |
| 49 | I/O | I/O |
| 50 | SDO, I/O | SDO, I/O |
| 51 | I/O | I/O |
| 52 | I/O | I/O |
| 53 | I/O | I/O |
| 54 | I/O | I/O |
| 55 | GND | GND |
| 56 | I/O | I/O |

***Table 57 •*** **TQ176**

| **TQ176** | | | |
|---|---|---|---|
| **Pin Number** | **A42MX09 Function** | **A42MX16 Function** | **A42MX24 Function** |
| 47 | I/O | I/O | TDI, I/O |
| 48 | I/O | I/O | I/O |
| 49 | I/O | I/O | WD, I/O |
| 50 | I/O | I/O | WD, I/O |
| 51 | I/O | I/O | I/O |
| 52 | NC | VCCI | VCCI |
| 53 | I/O | I/O | I/O |
| 54 | NC | I/O | I/O |
| 55 | NC | I/O | WD, I/O |
| 56 | I/O | I/O | WD, I/O |
| 57 | NC | NC | I/O |
| 58 | I/O | I/O | I/O |
| 59 | I/O | I/O | WD, I/O |
| 60 | I/O | I/O | WD, I/O |
| 61 | NC | I/O | I/O |
| 62 | I/O | I/O | I/O |
| 63 | I/O | I/O | I/O |
| 64 | NC | I/O | I/O |
| 65 | I/O | I/O | I/O |
| 66 | NC | I/O | I/O |
| 67 | GND | GND | GND |
| 68 | VCCA | VCCA | VCCA |
| 69 | I/O | I/O | WD, I/O |
| 70 | I/O | I/O | WD, I/O |
| 71 | I/O | I/O | I/O |
| 72 | I/O | I/O | I/O |
| 73 | I/O | I/O | I/O |
| 74 | NC | I/O | I/O |
| 75 | I/O | I/O | I/O |
| 76 | I/O | I/O | I/O |
| 77 | NC | NC | WD, I/O |
| 78 | NC | I/O | WD, I/O |
| 79 | I/O | I/O | I/O |
| 80 | NC | I/O | I/O |
| 81 | I/O | I/O | I/O |
| 82 | NC | VCCI | VCCI |
| 83 | I/O | I/O | I/O |

***Table 59 •*** **CQ256**

| **CQ256** | |
|---|---|
| **Pin Number** | **A42MX36 Function** |
| 59 | I/O |
| 60 | VCCA |
| 61 | GND |
| 62 | GND |
| 63 | NC |
| 64 | NC |
| 65 | NC |
| 66 | I/O |
| 67 | SDO, TDO, I/O |
| 68 | I/O |
| 69 | WD, I/O |
| 70 | WD, I/O |
| 71 | I/O |
| 72 | VCCI |
| 73 | I/O |
| 74 | I/O |
| 75 | I/O |
| 76 | WD, I/O |
| 77 | GND |
| 78 | WD, I/O |
| 79 | I/O |
| 80 | QCLKB, I/O |
| 81 | I/O |
| 82 | I/O |
| 83 | I/O |
| 84 | I/O |
| 85 | I/O |
| 86 | I/O |
| 87 | WD, I/O |
| 88 | WD, I/O |
| 89 | I/O |
| 90 | I/O |
| 91 | I/O |
| 92 | I/O |
| 93 | I/O |
| 94 | I/O |
| 95 | VCCI |

***Table 59 •*** **CQ256**

| **CQ256** | |
|---|---|
| **Pin Number** | **A42MX36 Function** |
| 133 | I/O |
| 134 | I/O |
| 135 | I/O |
| 136 | I/O |
| 137 | I/O |
| 138 | I/O |
| 139 | GND |
| 140 | I/O |
| 141 | I/O |
| 142 | I/O |
| 143 | I/O |
| 144 | I/O |
| 145 | I/O |
| 146 | I/O |
| 147 | I/O |
| 148 | I/O |
| 149 | I/O |
| 150 | I/O |
| 151 | I/O |
| 152 | I/O |
| 153 | I/O |
| 154 | I/O |
| 155 | VCCA |
| 156 | I/O |
| 157 | I/O |
| 158 | VCCA |
| 159 | VCCI |
| 160 | GND |
| 161 | I/O |
| 162 | I/O |
| 163 | I/O |
| 164 | I/O |
| 165 | GND |
| 166 | I/O |
| 167 | I/O |
| 168 | I/O |
| 169 | I/O |

***Table 61 •*** **PG132**

| **PG132** | |
|---|---|
| **Pin Number** | **A42MX09 Function** |
| N10 | I/O |
| M10 | I/O |
| N11 | I/O |
| L10 | I/O |
| M11 | I/O |
| N12 | SDO |
| M12 | I/O |
| L11 | I/O |
| N13 | I/O |
| M13 | I/O |
| K11 | I/O |
| L12 | I/O |
| L13 | I/O |
| K13 | I/O |
| H10 | I/O |
| J12 | I/O |
| J13 | I/O |
| H11 | I/O |
| H12 | I/O |
| H13 | VKS |
| G13 | VPP |